PTFA072401EL
PTFA072401FL

green Product

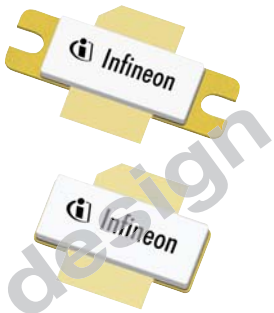
Thermally-Enhanced High Power RF LDMOS FETs
240 W, 30 V, 725 – 770 MHz

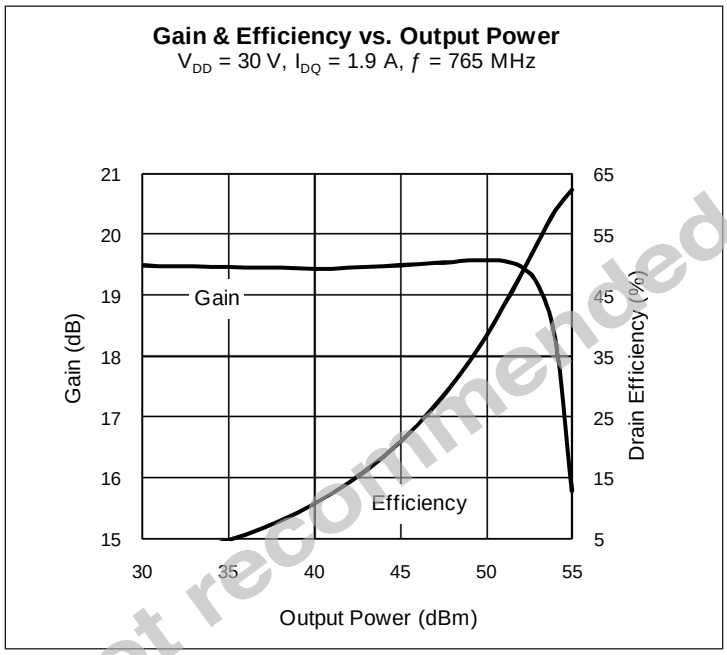
Description

The PTFA072401EL and PTFA072401FL are 240-watt LDMOS FETs designed for use in cellular power amplifier applications in the 725 to 770 MHz frequency band. These devices feature internal I/O matching and thermally-enhanced, open-cavity ceramic packages. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA072401EL
Package H-33288-2

PTFA072401FL
Package H-34288-2





Features

- Broadband internal matching
- Typical two-carrier WCDMA performance at 770 MHz, 30 V
  - Average output power = 40 W
  - Linear gain = 19 dB
  - Efficiency = 25%
  - Intermodulation distortion = –39 dBc
- Typical CW performance, 770 MHz, 30 V
  - Output power at P_{1dB} = 240 W
  - Efficiency = 58%
- Integrated ESD protection
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 30 V, 240 W (CW) output power
- Thermally-enhanced packages, Pb-free and RoHS compliant with low gold (<0.25 micron) plating

not recommended for new design

RF Characteristics

Two-carrier WCDMA Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
V_{DD} = 30 V, I_{DQ} = 1800 mA, P_{OUT} = 40 W average, f_1 = 760 MHz, f_2 = 770 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8.1 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	19	—	dB
Drain Efficiency	η_D	—	25	—	%
Intermodulation Distortion	IMD	—	–39	—	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)
V_{DD} = 30 V, I_{DQ} = 1800 mA, P_{OUT} = 220 W PEP, f = 765 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	18	19	—	dB
Drain Efficiency	η_D	43	45	—	%
Intermodulation Distortion	IMD	—	–29	–28	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	1.82	—	Ω
Operating Gate Voltage	V_{DS} = 30 V, I_{DQ} = 1800 mA	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	700	W
Above 25°C derate by		4.0	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 240 W CW)	$R_{\theta JC}$	0.28	°C/W

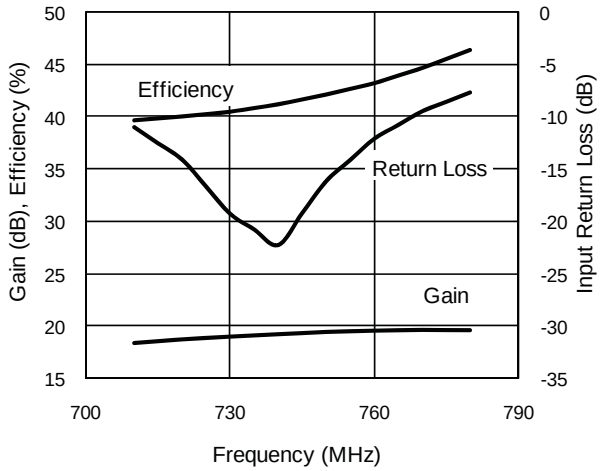
Ordering Information

Type and Version	Order Code	Package	Package Description	Shipping
PTFA072401EL V5	PTFA072401ELV5XWSA1	H-33288-2	Slotted flange	Tray
PTFA072401FL V5	PTFA072401FLV5XWSA1	H-34288-2	Earless flange	Tray

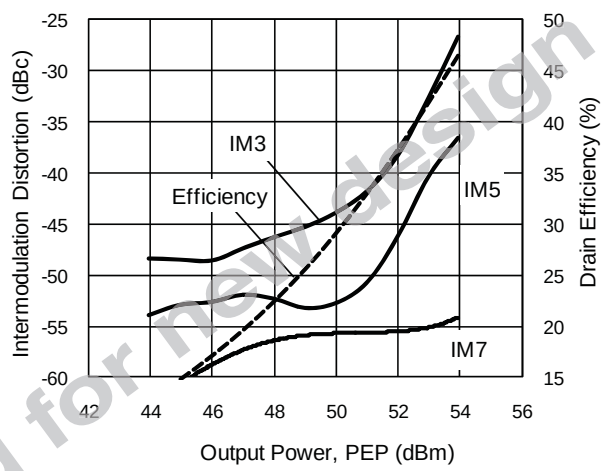
not recommended for new design

Typical Performance (data taken in a production test fixture)

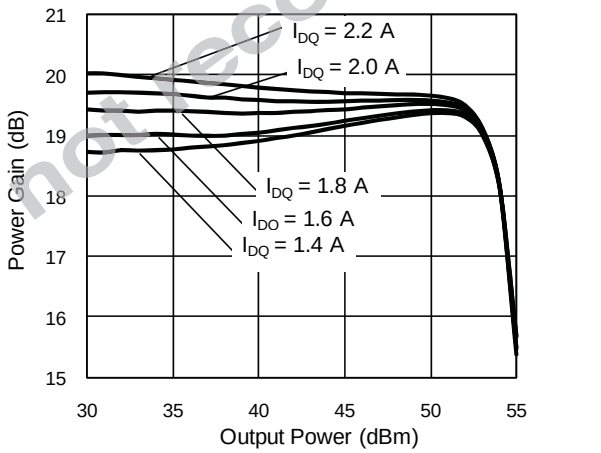
Broadband Performance
V_{DD} = 30 V, I_{DQ} = 1800 mA, P_{OUT} = 126 W



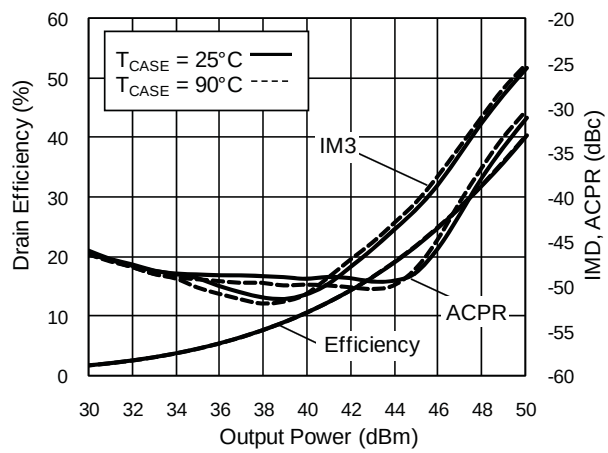
Two-tone Drive-up
V_{DD} = 30 V, I_{DQ} = 1800 mA,
f = 765 MHz, tone spacing = 1 MHz



Power Sweep
V_{DD} = 30 V, f = 770 MHz

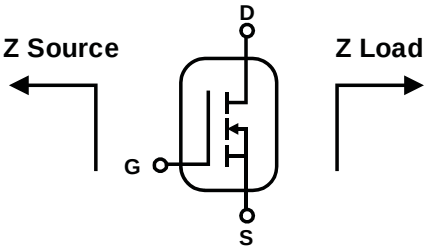


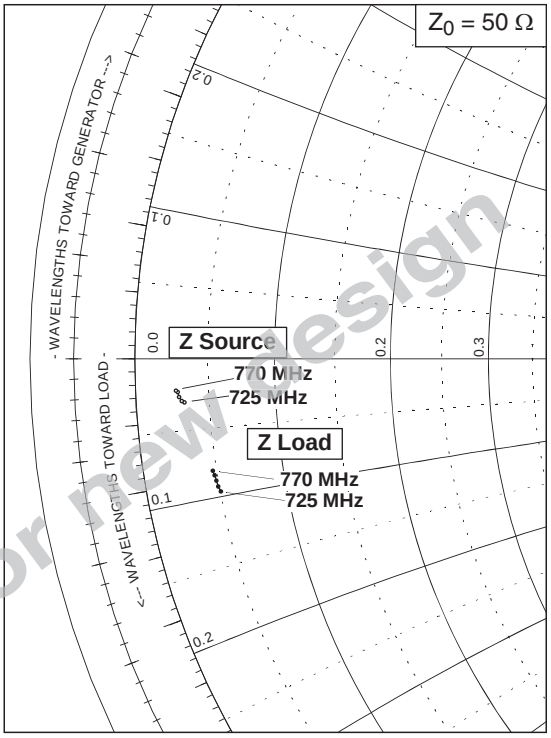
Two-carrier WCDMA Performance
V_{DD} = 30 V, I_{DQ} = 1.9 A, f = 765 MHz



not recommended for new design

Broadband Circuit Impedance



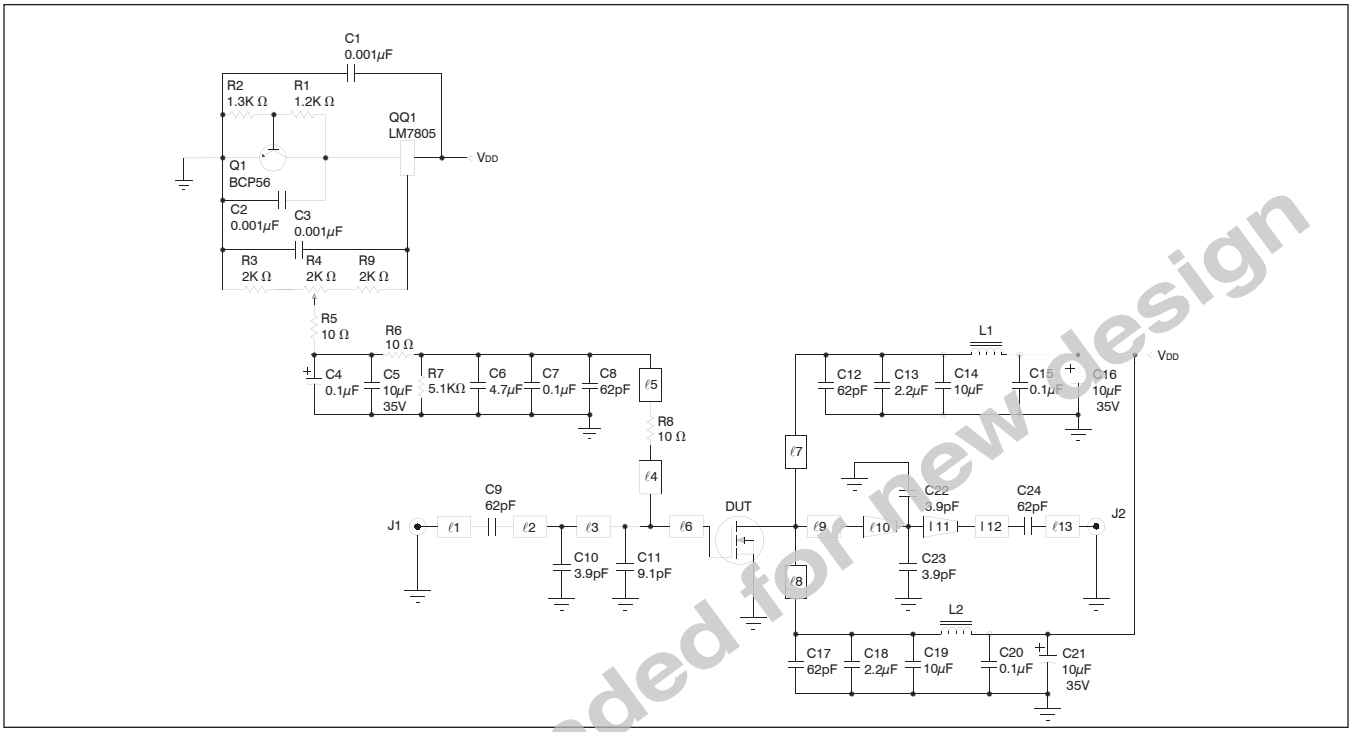


Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
725	2.53	–4.83	1.64	–1.54
736	2.48	–4.64	1.55	–1.48
748	2.44	–4.41	1.46	–1.33
759	2.41	–4.22	1.42	–1.17
770	2.37	–4.04	1.36	–1.11

See next page for reference circuit information

not recommended for new design

Reference Circuit



Reference circuit schematic for ƒ = 770 MHz

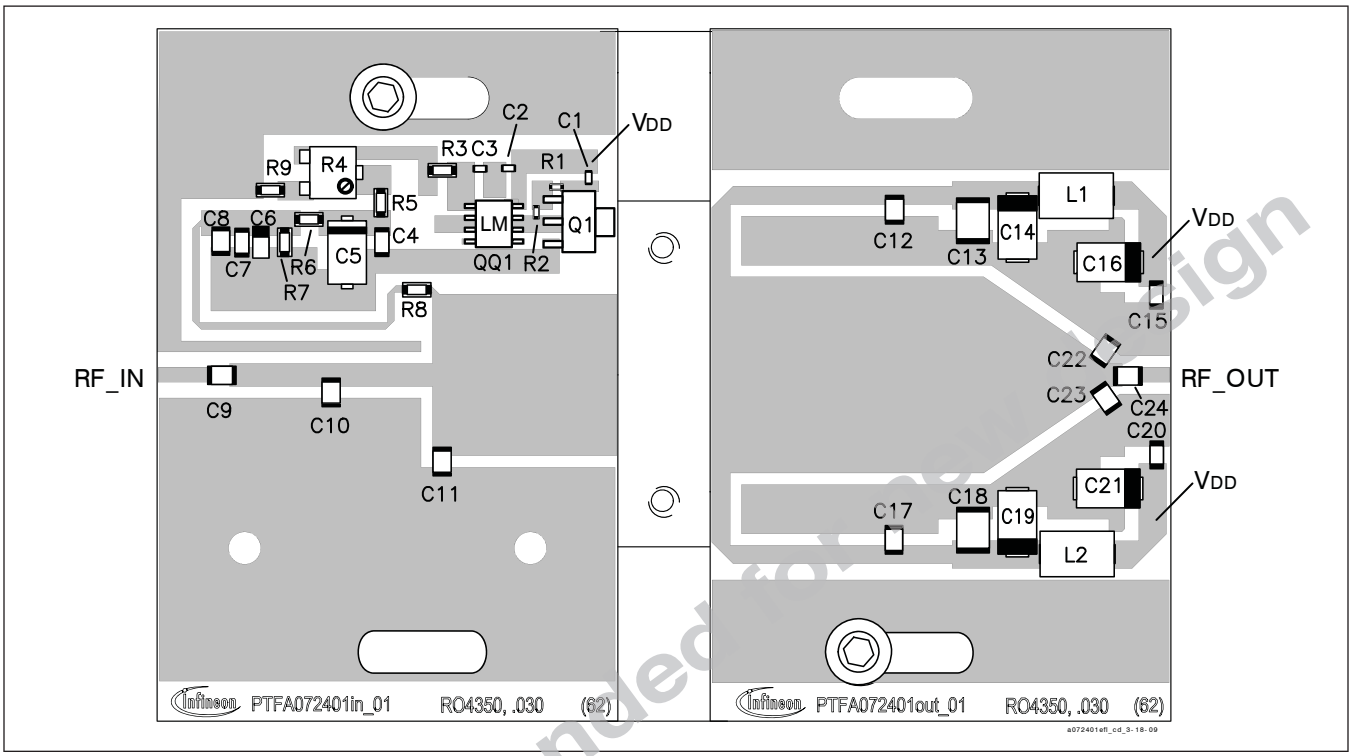
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Circuit Assembly Information

DUT	PTFA072401EL or PTFA072401FL	LDMOS Transistor
PCB	LTN/PTFA072401E or LTN/PTFA072401F	Rogers RO4350: 0.76 mm [.030"] thick, εr = 3.48, 1 oz. copper

Microstrip	Electrical Characteristics at 770 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.025 λ, 50.7 Ω	5.84 x 1.65	0.230 x 0.065
ℓ2, ℓ3	0.048 λ, 38.4 Ω	11.18 x 2.54	0.440 x 0.100
ℓ4	0.002 λ, 76.8 Ω	0.51 x 0.76	0.020 x 0.030
ℓ5	0.145 λ, 76.8 Ω	35.43 x 0.76	1.395 x 0.030
ℓ6	0.094 λ, 7.8 Ω	20.32 x 17.78	0.800 x 0.700
ℓ7, ℓ8	0.108 λ, 44.5 Ω	25.40 x 2.03	1.000 x 0.080
ℓ9	0.140 λ, 6.5 Ω	29.97 x 21.59	1.180 x 0.850
ℓ10 (taper)	0.058 λ, 6.5 Ω / 29.4 Ω	13.13 x 21.59 / 3.68	0.517 x 0.850 / 0.145
ℓ11 (taper)	0.004 λ, 29.4 Ω / 38.4 Ω	0.84 x 3.68 / 2.54	0.033 x 0.145 / 0.100
ℓ12	0.005 λ, 38.4 Ω	1.27 x 2.54	0.050 x 0.100
ℓ13	0.016 λ, 50.7 Ω	3.76 x 1.65	0.148 x 0.065

Reference Circuit (cont.)



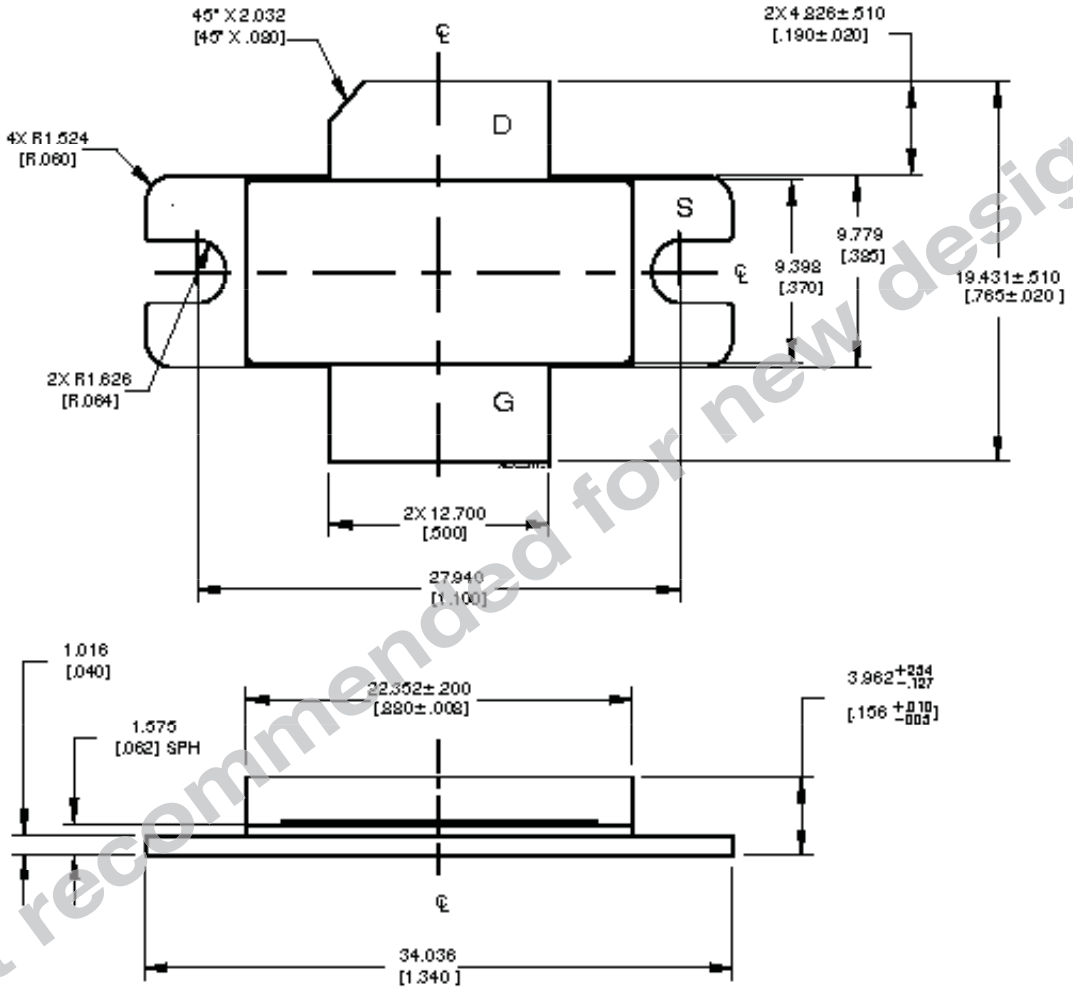
Reference circuit assembly diagram (not to scale)

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4, C7, C15, C20	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C5,	Tantalum Capacitor, 10 µF, 35 V	Digi-Key	399-1655-2-ND
C6	Capacitor, 4.7 µF, 16 V	Digi-Key	PCS3475CT-ND
C8, C9, C12, C17, C24	Ceramic capacitor, 62 pF	ATC	100B 620
C10, C22, C23	Ceramic capacitor, 3.9 pF	ATC	100B 3R9
C11	Ceramic capacitor, 9.1 pF	ATC	100B 9R1
C13, C18	Capacitor, 2.2 µF	Digi-Key	445-1447-2-ND
C14, C16, C19, C21	Tantalum Capacitor, 10 µF, 35 V	Digi-Key	PCS6106TR-ND
L1, L2	Ferrite, 8.9 mm	Digi-Key	240-2511-2-ND
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage Regulator	National Semiconductor	LM7805
R1	Chip resistor, 1.2k Ω	Digi-Key	P1.2KGCT-ND
R2	Chip resistor, 1.3k Ω	Digi-Key	P1.3KGCT-ND
R3, R9	Chip resistor, 2k Ω	Digi-Key	P2KECT-ND
R4	Variable Resistor 2k Ω	Digi-Key	3224W-202ETR-ND
R5, R6, R8	Chip resistor, 10 Ω	Digi-Key	P10ECT-ND
R7	Chip resistor 5.1k Ω	Digi-Key	P5.1KECT-ND

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Package Outline Specifications

Package H-33288-2



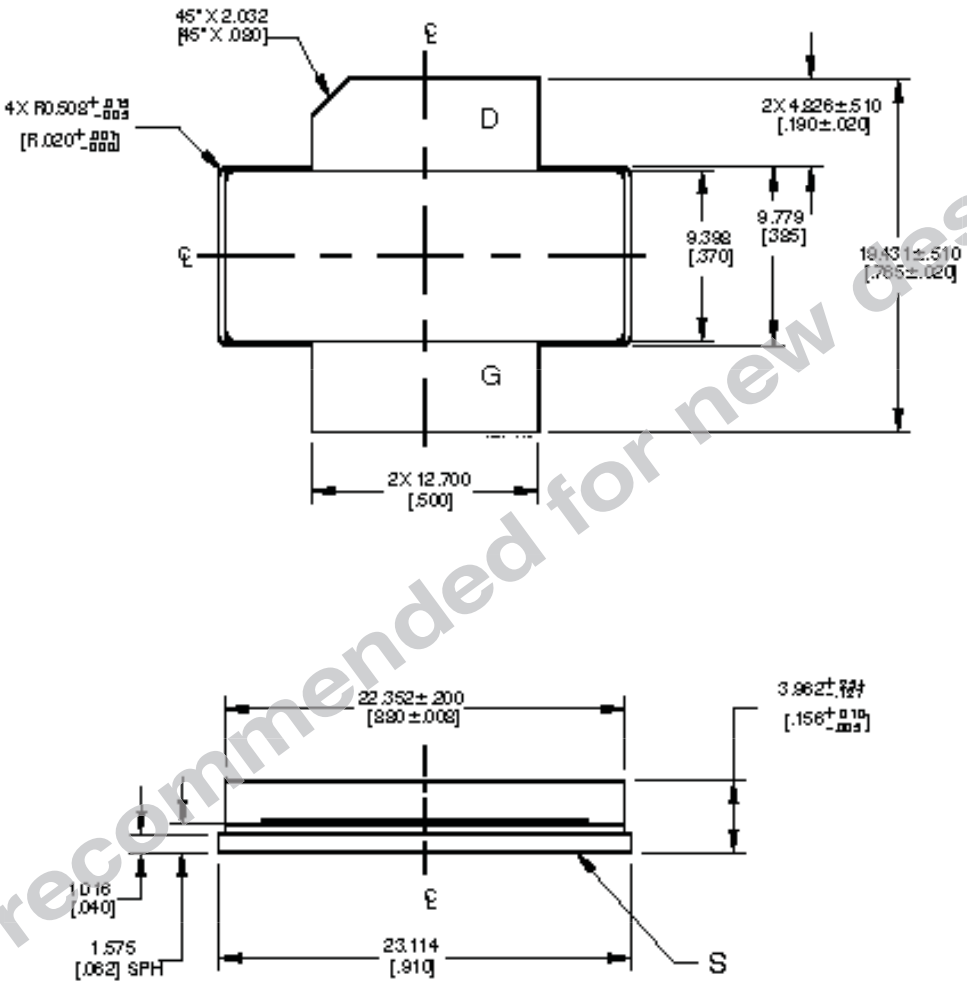
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Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D – drain; S – source; G – gate.
5. Lead thickness: 0.10 + 0.051/–0.025 mm [.004 +0.002/–0.001 inch].
6. Gold plating thickness: 0.25 micron [10 microinch] max.

Package Outline Specifications (cont.)

Package H-34288-2



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Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D – drain; S – source; G – gate.
5. Lead thickness: 0.10 + 0.051/–0.025 mm [.004 +0.002/–0.001 inch].
6. Gold plating thickness: 0.25 micron [10 microinch] max.

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Revision History:	2015-02-24	Data Sheet
Previous Version:	2012-02-16, Data Sheet	
Page	Subjects (major changes since last revision)	
All	Not recommended for new design	

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