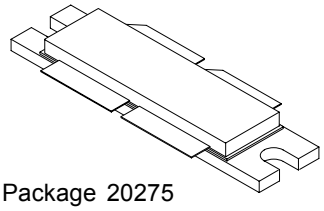
PEAK DEVICES



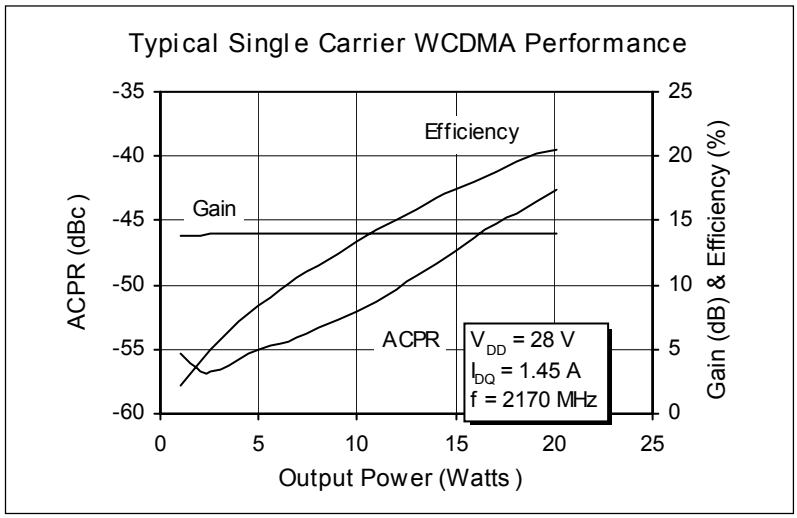
Package 20275

120 Watts, 2110-2170 MHz PUSH/PULL LATERAL MOSFET

PTF102003

Description

The PTF102003 is a 120–watt, internally matched LDMOS FET intended for WCDMA applications from 2110 to 2170 MHz. This device typically operates at 48% efficiency (P-1dB) and 14 dB linear gain. Full gold metallization ensures excellent device lifetime and reliability.



Key Features

- INTERNALLY MATCHED
- Typical WCDMA Performance at 28 V
  - Average Output Power = 20 W atts
  - Gain = 14 dB
  - Efficiency = 22%
    (channel bandwidth 3.84 MHz, adjacent channels ±5 MHz, peak/avg 8.5:1 at 0.01% CCD)
- Typical CW Performance at 28 V
  - Output Power at P1-dB = 120 W atts
  - Gain = 13 dB
  - Efficiency = 48%
- Full Gold Metallization
- Integrated ESD Protection; Class 1 (minimum) Human Body Model
- Excellent Thermal Stability
- Broadband Internal Matching
- Low HCI Drift
- Capable of Handling 10:1 VSWR @ 28 V , 120 Watts (CW) Output Power

Guaranteed Performance

WCDMA Measurements (in test fixture)

V_{DD} = 28 V, I_{DQ} = 1.45 A, P_{OUT} = 20 W AVG
f = 2170 MHz, Single Carrier 3GPP Channel Bandwidth 3.84 MHz, Adj Channels ± 5 MHz, Peak to Avg 8.5:1

Characteristic	Symbol	Min	Typ	Max	Units
Adjacent Channel Power Ratio	ACPR	—	-45	-40	dB
Gain	G_{ps}	13	14.5	—	dB
Drain Efficiency	η_D	19	22	—	%

Two-Tone Measurements (in test fixture)

V_{DD} = 28 V, I_{DQ} = 1.20 A, P_{OUT} = 120 W PEP, f = 2170 MHz, Tone Spacing = 100 kHz

Characteristic	Symbol	Min	Typ	Max	Units
Gain	G_{ps}	12.5	14	—	dB
Drain Efficiency	η_D	31	36	—	%
Intermodulation Distortion	IMD	-27	-30	—	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated.

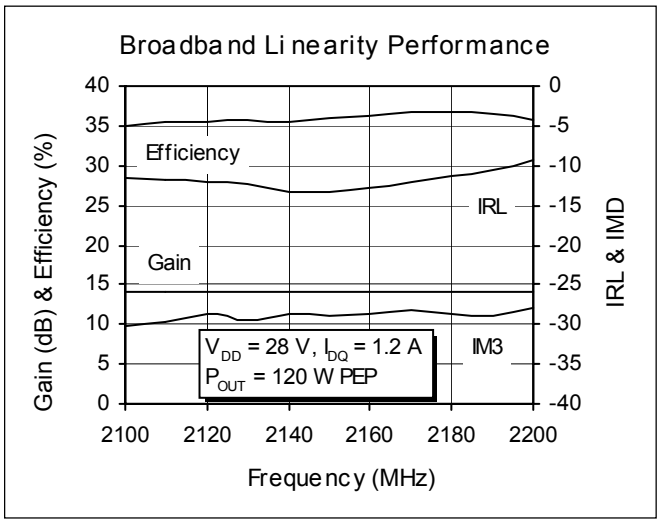
Electrical Characteristics (Guaranteed)

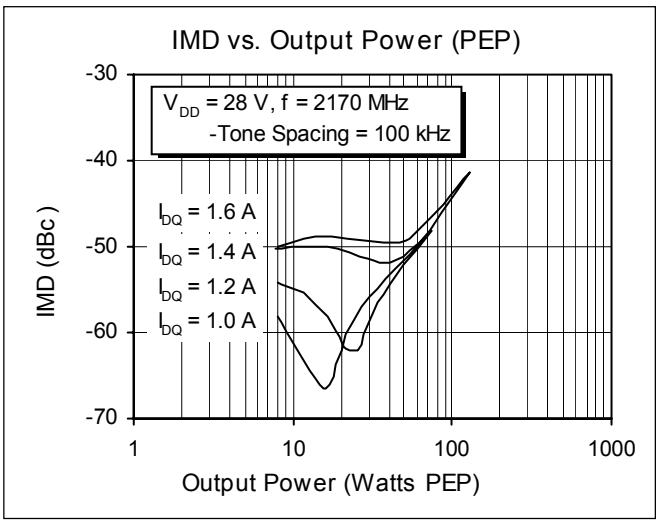
Characteristic	Conditions	Symbol	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 1 µA/Side	$V_{(BR)DSS}$	65	—	—	Volts
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V/Side	I_{DSS}	—	—	1.0	µA
On-State Resistance	V_{GS} = 10 V, I_{DS} = 1 A/Side	$R_{DS(on)}$	—	0.13	—	Ohms
Quiescent Current Gate Voltage	V_{DS} = 28 V, I_D = 700 mA/Side	$V_{GS(Q)}$	2.5	3.4	4	Volts
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V/Side	I_{GSS}	—	—	100	nA

Maximum Ratings

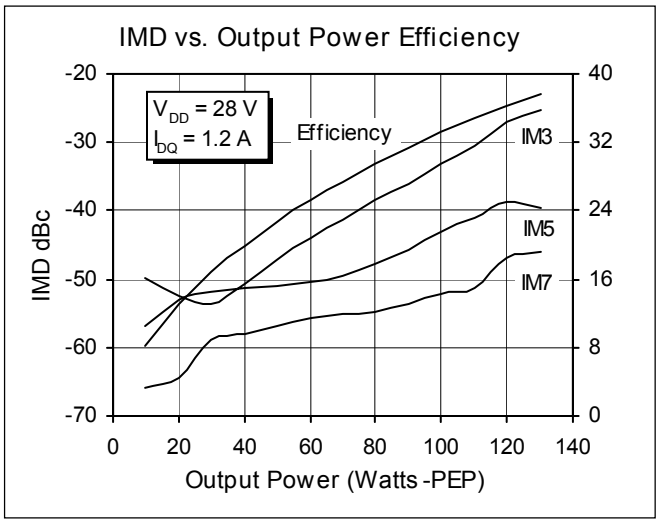
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Volts
Gate-Source Voltage	V_{GS}	+15, -0.5	Volts
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	330	Watts
Above 25°C derate by		1.88	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C)	$R_{\theta JC}$	0.55	°C/W

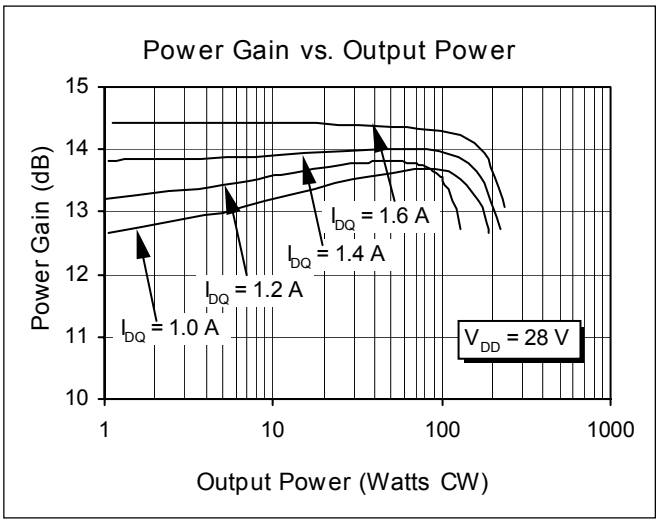
Typical Performance

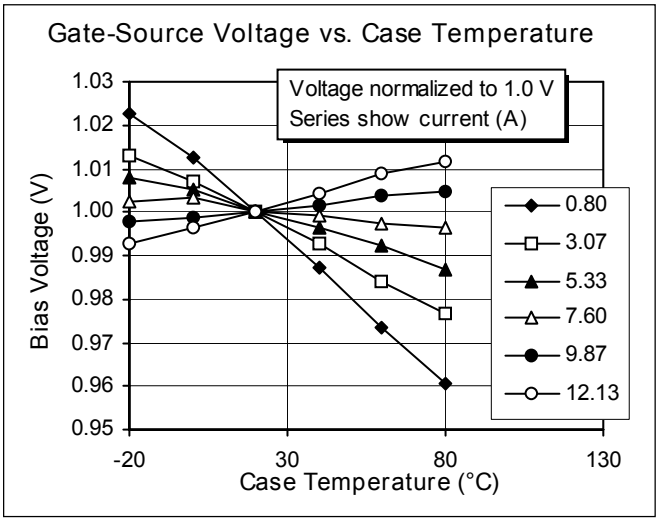


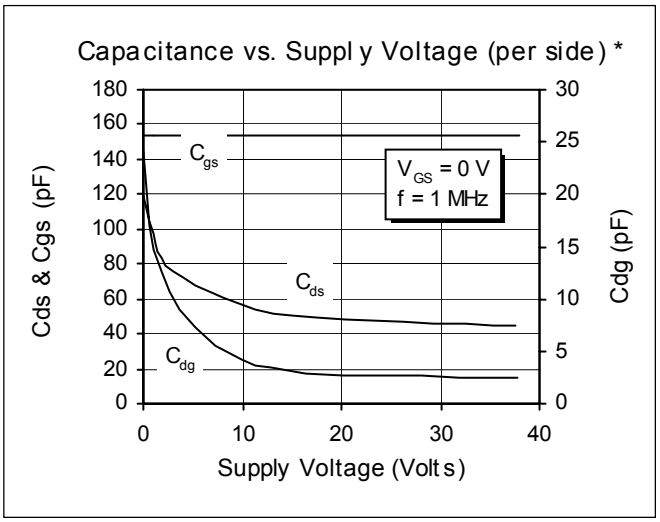


Typical Performance (cont.)





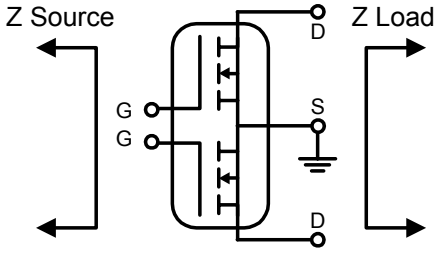


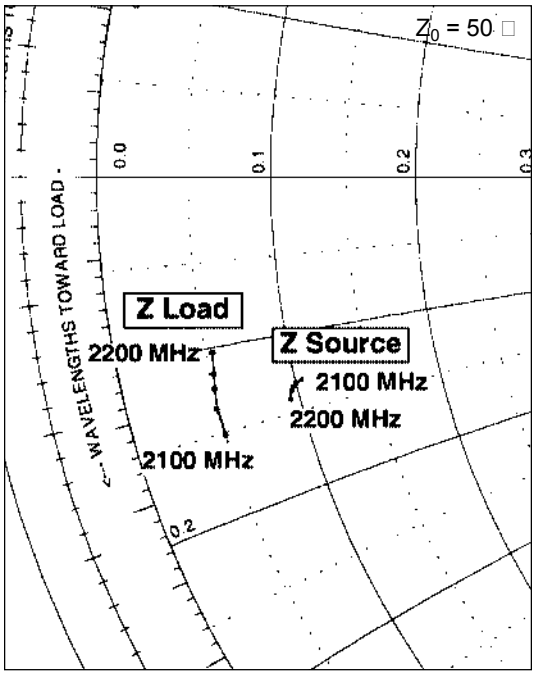


* This part is internally matched. Measurements of the finished product will not yield these results.

Broadband Circuit Impedance

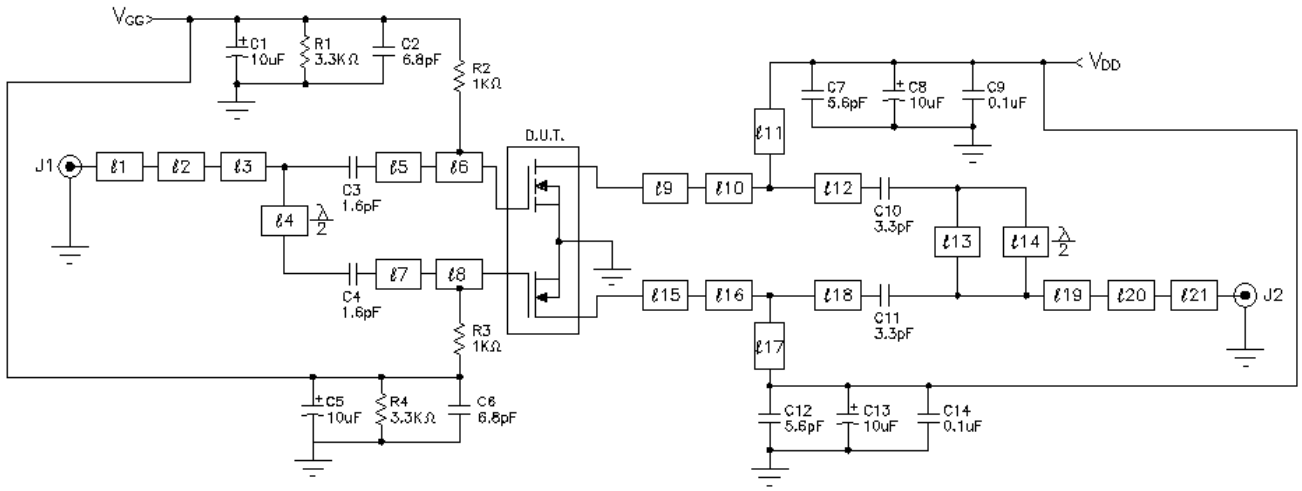
V_{DD} = 28 V, I_{DQ} = 1.2 A, Pout = 20 W Avg 2 Tone 1 MHz Spacing





Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
2100	5.2	-6.58	2.52	-7.6
2110	5.0	-6.62	2.48	-6.8
2140	4.9	-6.73	2.56	-6.2
2170	4.8	-6.85	2.62	-5.78
2200	4.7	-7.10	2.72	-5.17

Test Circuit

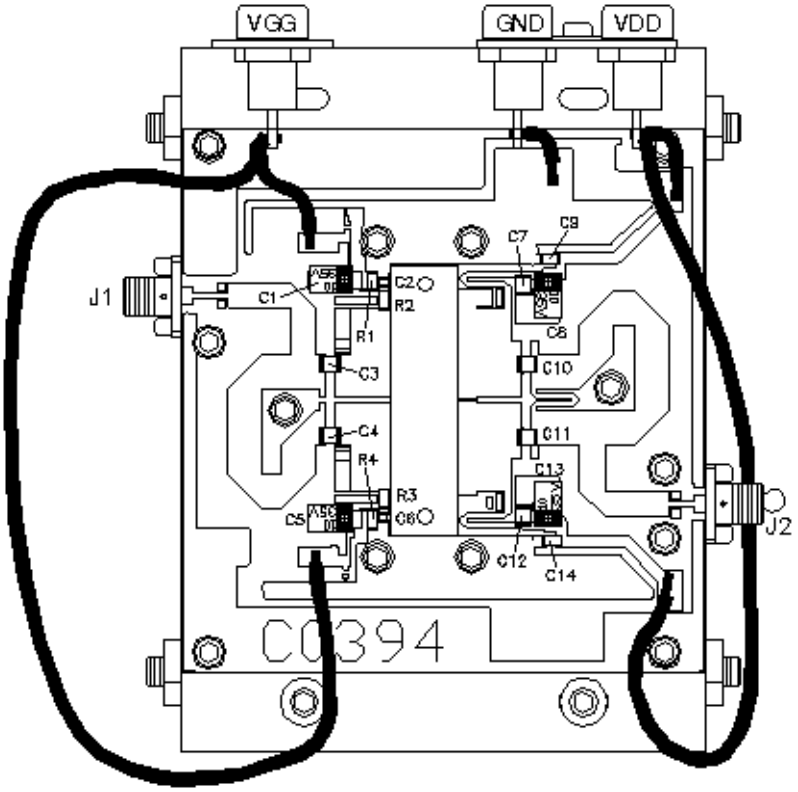


Test Circuit (cont.)

Test Circuit Schematic for 2170 MHz

DUT	PTF 102003	LDMOS Transistor
1, 21	0.02 @ 2170 MHz	Microstrip 29.20
2	0.07 @ 2170 MHz	Microstrip 50
3	0.26 @ 2170 MHz	Microstrip 20.10
4, 14	0.50 @ 2170 MHz	Microstrip 15.50
5, 7	0.03 @ 2170 MHz	Microstrip 13.10
6, 8	0.08 @ 2170 MHz	Microstrip 6.80
9, 15	0.04 @ 2170 MHz	Microstrip 5.50
10, 16	0.06 @ 2170 MHz	Microstrip 13.10
11, 17	0.26 @ 2170 MHz	Microstrip 53.60
12, 18	0.02 @ 2170 MHz	Microstrip 10.40
13	0.42 @ 2170 MHz	Microstrip 53.60
19	0.27 @ 2170 MHz	Microstrip 20.10
20	0.05 @ 2170 MHz	Microstrip 50

C1, C5, C8, C13	Capacitor, 10 µF, 35 V, Tant TE Series SMD, Digi-Key PCS6106TR
C2, C6	Capacitor, 6.8 pF, 100A 6R8
C3, C4	Capacitor, 1.6 pF, ATC 600B 1R6 BW
C7, C12	Capacitor, 5.6 pF, 100B 5R6
C9, C14	Capacitor, 0.1 µF, 50 V, Digi-Key PCC103BCT
C10, C11	Capacitor, 3.3 pF, ATC 600B 3R3 BW
J1, J2	Connector, SMA Female, Panel Mount
R1, R4	Resistor, 3.3 K ohms, 1/16W 5% 0603 Digi-Key P3.3K GCT
R2, R3	Resistor, 1 K ohms, 1/16W 5% 0603 Digi-Key P1.0K GCT
PCB	4003, .020", 1 oz. copper both sides, 1 layer. AlliedSignal

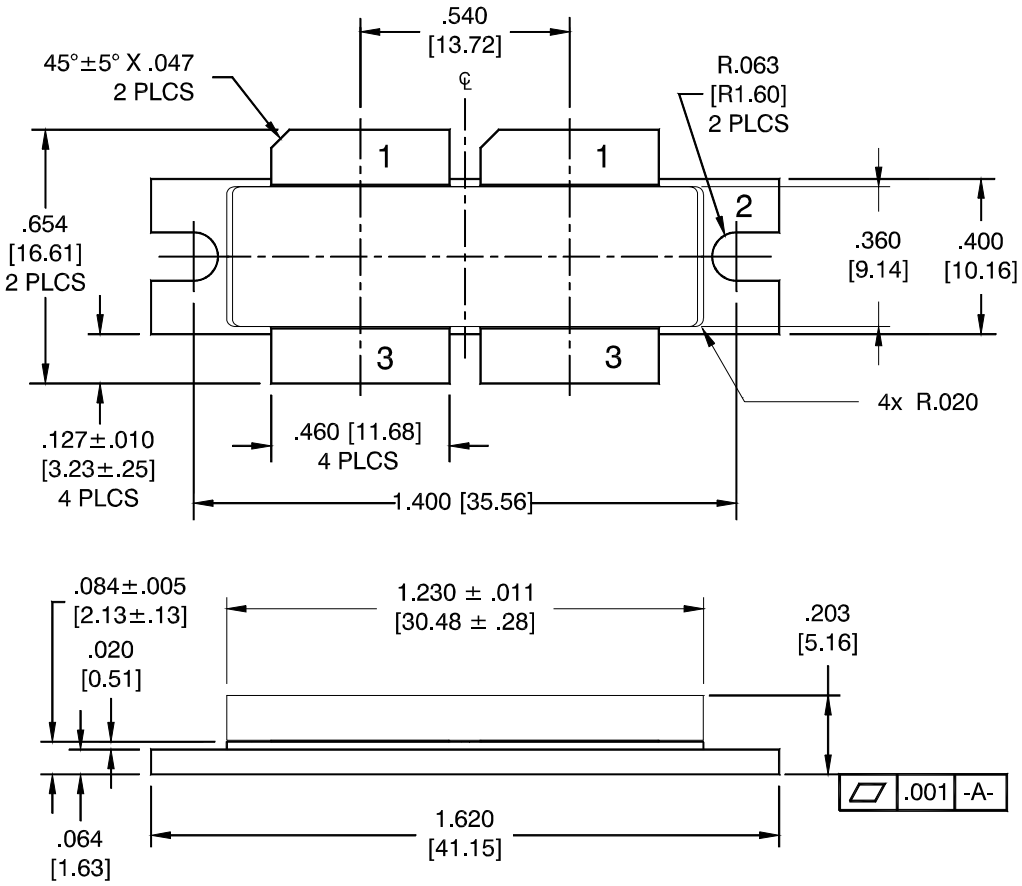


Assembly Diagram (not to scale)

PTF 102003

Case Outline Specifications

Case 20275



All tolerances ±0.005"
unless specified otherwise

Pins: 1.Drain 2.Source 3.Gate
Lead Thickness:
.005±0.001 [0.13±0.03]

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