PSD4XX
ZPSD4XX

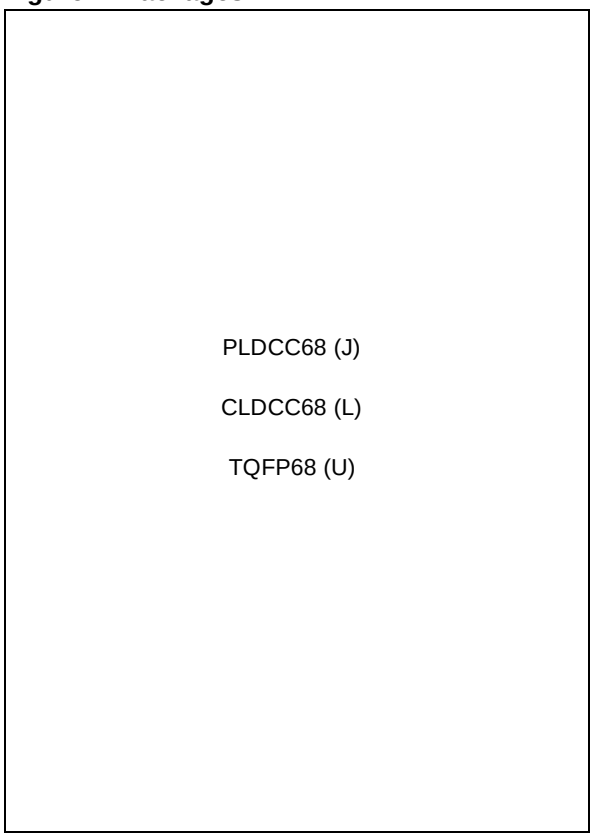
Low Cost Field Programmable Microcontroller Peripherals

NOT FOR NEW DESIGN

FEATURES SUMMARY

- Single Supply Voltage:
  - 5 V±10% for PSD4XX
  - 2.7 to 5.5 V for PSD4XX-V
- Up to 1 Mbit of UV EPROM
- Up to 16 Kbit SRAM
- Input Latches
- Programmable I/O ports
- Page Logic
- Programmable Security

Figure 1. Packages



This is information on a product still in production but not recommended for new designs.

PSD4XX Family

PSD4XX/ZPSD4XX

Field-Programmable Microcontroller Peripherals

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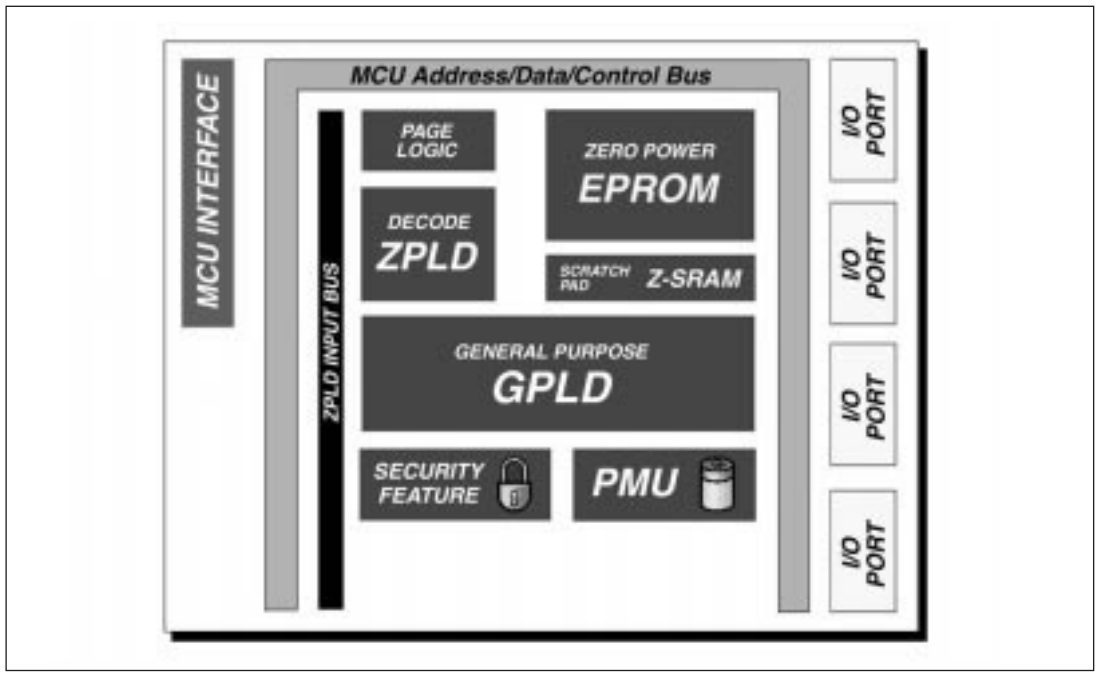
Programmable Peripheral
PSD4XX Family
Field-Programmable Microcontroller Peripherals

1.0 Introduction

The PSD4XX family is a microcontroller peripheral that integrates high-performance and user-configurable blocks of EPROM, programmable logic, and SRAM into one part. The PSD4XX products also provide a powerful microcontroller interface that eliminates the need for external “glue logic”. The no “glue logic” concept provides a user-programmable interface to a variety of 8- and 16-bit (multiplexed or non-multiplexed) microcontrollers that is easy to use. The part’s integration, small form factor, low power consumption, and ease of use make it the ideal part for interfacing to virtually any microcontroller.

The PSD4XX provides two Zero-power PLDs (ZPLD): a Decode PLD (DPLD) and a General-purpose PLD (GPLD). A configuration bit (Turbo) can be set by the MCU, and will automatically place the ZPLDs into Standby Mode if no inputs are changing. The ZPLDs are designed to consume minimum power using Zero-power CMOS technology that uses only 10 µA (typical) standby current. Unused product terms are automatically disabled, also reducing power, regardless of the Turbo bit setting.

The main function of the DPLD is to perform address decoding for the internal I/O ports, EPROM, and SRAM. The address decoding can be based on up to 24 bits of address inputs, control signals ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, etc.), and internal page logic. The DPLD supports separate program and data spaces (for 8031 compatible MCUs).



The General-purpose PLD (GPLD) can be used to implement various logic functions defined by the user, such as:

- State machines
- Loadable counters and shift registers
- Inter-processor mailbox
- External control logic (chip selects, output enables, etc.).

The GPLD has access to up to 59 inputs, 118 product terms, 24 macrocells, and 24 I/O pins.

1.0 Introduction (cont.)

The PSD4XX has 40 I/O pins that are divided among 5 ports. Each I/O pin can be individually configured to provide many functions, including the following:

- MCU I/O
- GPLD I/O
- Latched address output (for MCUs with multiplexed data bus)
- Data bus (for MCUs with non-multiplexed data bus).

The PSD4XX can easily interface with virtually any 8- or 16-bit microcontroller with a multiplexed or non-multiplexed bus. All of the MCU control signals are connected to the ZPLDs, enabling the user to generate signals for external devices.

The PSD4XX provides between 256 Kbits and 1 Mbit of EPROM that is divided in to four equal-sized blocks. Each block can occupy a different address location, allowing for versatile address mapping. The access time of the EPROM includes the address latching and DPLD decoding.

The PSD4XX has an optional 16 Kbit SRAM that can be battery-backed by connecting a battery to the Vstby pin. The battery will protect the contents of the SRAM in the event of a power failure. Therefore, you can place data in the SRAM that you want to keep after the power is switched off. Power switchover to the battery automatically occurs when V_{CC} drops below V_{stby}.

A four-bit Page Register enables easy access to the I/O section, EPROM, and SRAM for microcontrollers with limited address space. The Page Register outputs are connected to both ZPLDs and thus can also be used for external paging schemes.

The Power Management Unit (PMU) of the PSD4XX enables the user to control the power consumption on selected functional blocks, based on system requirements. For microcontrollers that do not generate a chip select input for the PSD, the Automatic Power-Down (APD) unit of the PMU can be setup to enable the PSD to enter Power Down Mode or Sleep Mode, based on the inactivity of ALE (or AS).

Implementing your design has never been easier than with PSDsoft—ST's software development suite. Using PSDsoft, you can do the following:

- Configure your PSD4XX to work with virtually any microcontroller
- Specify what you want implemented in the programmable logic using a design file
- Simulate your design
- Download your design to the part using a programmer.

2.0 Key Features

❑ Single-chip programmable peripheral for microcontroller-based applications

❑ 256K to 1 Mbit of UV EPROM with the following features:
- Configurable as 32, 64, or 128 K x 8; or as 16, 32, or 64 K x 16
- Divided into four equally-sized mappable blocks for optimized address mapping
- As fast as 70 ns access time, which includes address decoding
- Built-in Zero-power technology

❑ 16 Kbit SRAM is configurable as 2K x 8 or 1K x 16. The access time can be as quick as 70 ns, including address decoding. The contents of the SRAM can be battery-backed by connecting a battery to the Vstby pin. The SRAM also has built-in Zero-power technology.

❑ 40 I/O pins (divided into five 8-bit ports) that can be individually configured for:
- Standard MCU I/O
- PLD/macrocell I/O
- Latched address output
- High-order address inputs
- Special function I/O
- Open-drain output

2.0 Key Features

- ❑ Two Zero-power Programmable Logic Devices (ZPLDs): the Decode PLD (DPLD) and the General-purpose PLD (GPLD) can be used for:
  - Up to 59 Input and 126 output product terms
  - 24 Macrocells and I/O
  - Decode up to 16 MB of address
  - State machines and state logic
  - Generate external signals (chip selects, bus interface, etc.)
- ❑ Microcontroller logic that eliminates the need for external “glue logic” has the following features:
  - Ability to interface to multiplexed and non-multiplexed buses
  - Built-in address latches for multiplexed address/data bus
  - ALE and Reset polarity are programmable
  - Multiple configurations are possible for interface to many different microcontrollers
- ❑ Page logic is connected to the ZPLDs and expands the MCU address space to up to 16 times
- ❑ Programmable power management allows:
  - SRAM, EPROM, and ZPLDs to enter standby mode automatically
  - Disabling of the clock input to the ZPLDs
  - ZPLDs to enter a special low power mode (Sleep Mode), based on Turbo bit setting
- ❑ A security bit prevents reading the PSD4XX configuration and the ZPLD contents. Setting this bit will prevent the device from being copied on a device programmer.
- ❑ Built-in security enables the user to block read accesses from a device programmer
- ❑ Package choices include 68-pin PLCC, 68-pin CLDCC, and 80-pin TQFP
- ❑ Programmable polarity Reset output (includes hysteresis), based on Reset input
- ❑ Simple, menu-driven software (PSDsoft) allows configuration and design entry on a PC.

3.0 Notation

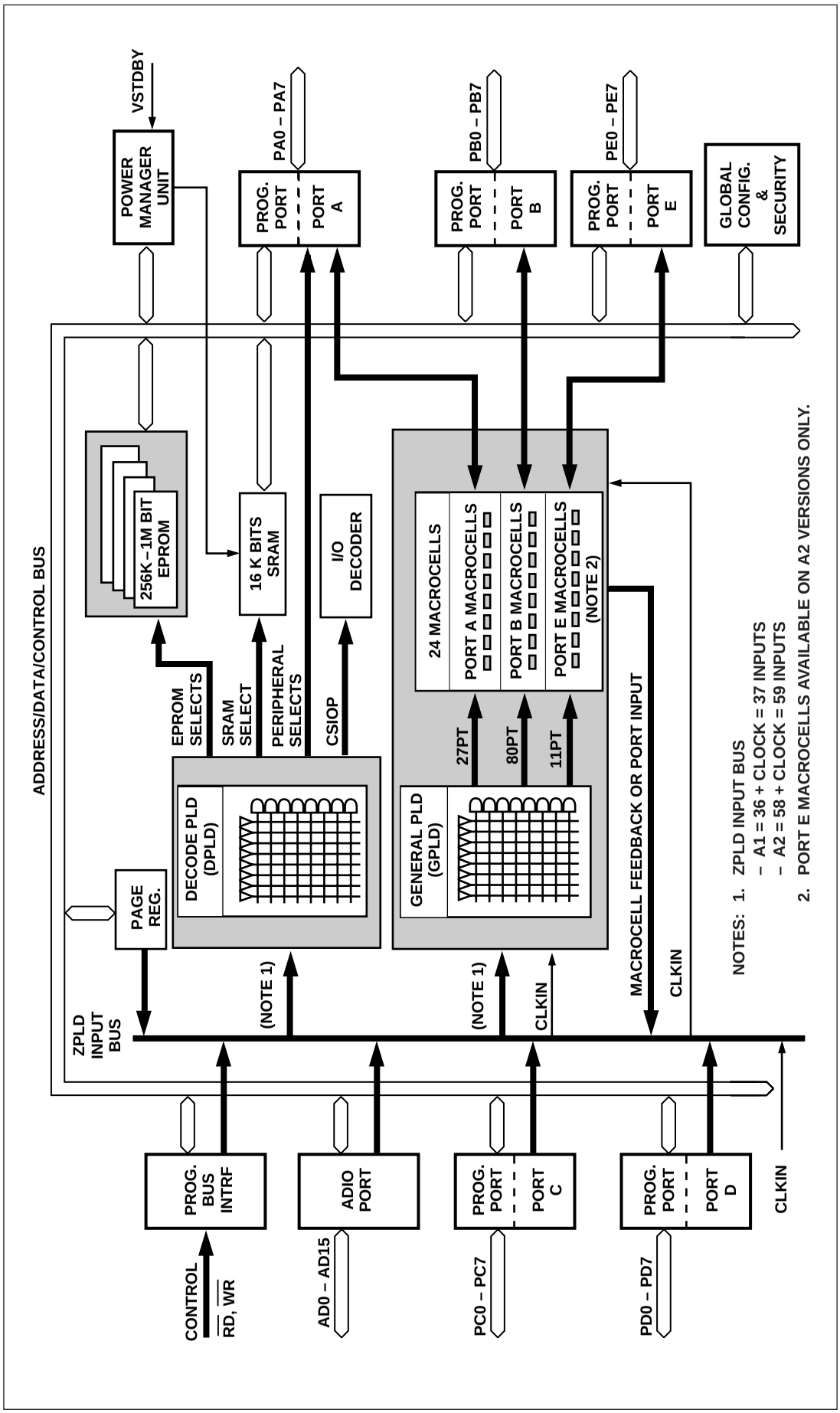
Throughout this data sheet, references are made to the PSD4XX. In most cases, these references also cover the ZPSD4XX and ZPSD4XXV products. Exceptions will be noted.

The main difference between the ZPSD4XX and the PSD4XX is the standby current (Isb). The ZPSD4XX devices have been rated for a lower standby current. Also, there is no low-voltage version of the PSD4XX. There is only the low-voltage version of the ZPSD4XX, which has a V suffix.

4.0 Zero-Power Background

Portable and battery powered systems have recently become major embedded control application segments. As a result, the demand for electronic components having extremely low power consumption has increased dramatically. Recognizing this need, ST has developed a new Zero Power technology. PSD4XX products virtually eliminate the DC component of power consumption reducing it to standby levels. Eliminating the DC component is the basis for the words “Zero Power”. PSD4XX products also minimize the AC power component when the chip is changing states. The result is a programmable microcontroller peripheral family that replaces discrete circuit functions while drawing minimal current.

Figure 1. PSD4XX Block Diagram



5.0 Integrated Power Management™ Operation

Upon each address or logic input change to the ZPSD, the device powers up from low power standby for a short time. Then the ZPSD consumes only the necessary power to deliver new logic or memory data to its outputs as a response to the input change. After the new outputs are stable, the ZPSD latches them and automatically reverts back to standby mode. The I_{CC} current flowing during standby mode and during DC operation is identical and is only a few microamperes.

The ZPSD automatically reduces its DC current drain to these low levels and does not require controlling by the CSI (Chip Select Input). Disabling the CSI pin unconditionally forces the ZPSD to standby mode independent of other input transitions.

The only significant power consumption in the ZPSD occurs during AC operation.

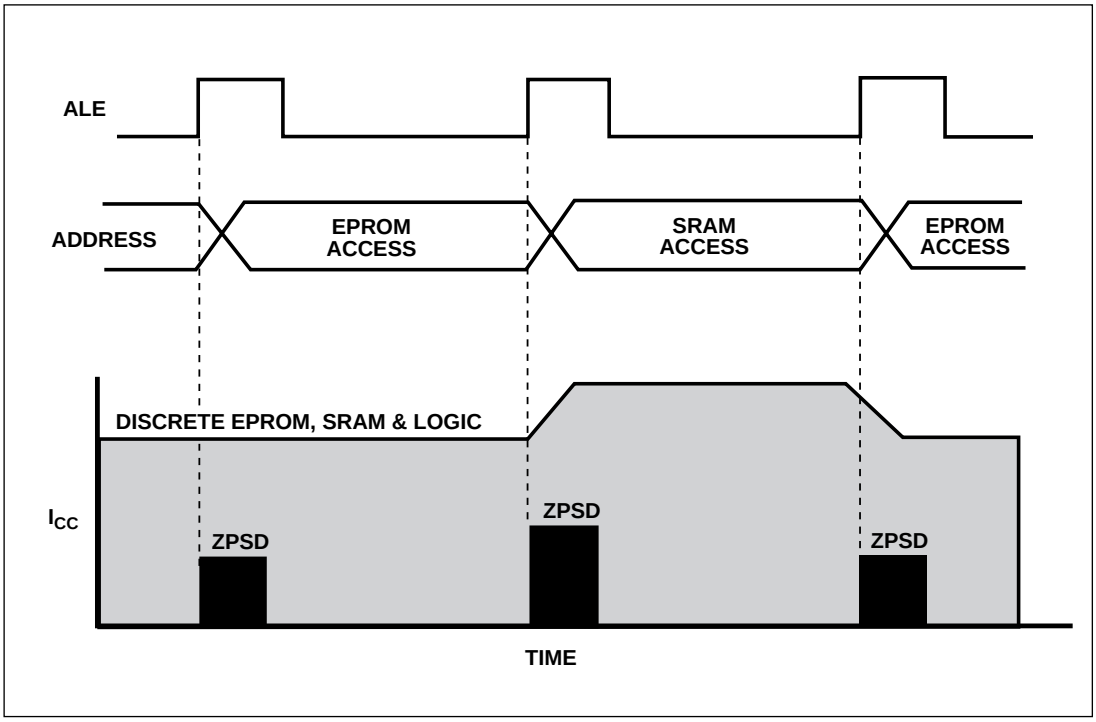
The ZPSD contains the first architecture to apply zero power techniques to memory and logic blocks.

Figure 2 compares ZPSD Zero-power operation to the operation of a discrete solution. A standard microcontroller (MCU) bus cycle usually starts with an ALE (or AS) pulse and the generation of an address. The ZPSD detects the address transition and powers up for a short time. The ZPSD then latches the outputs of the PAD, EPROM and SRAM to the new values. After finishing these operations, the ZPSD shuts off its internal power, entering standby mode. The time taken for the entire cycle is less than the ZPSD's "access time."

The ZPSD will stay in standby mode if inputs do not change between bus cycles. In an alternate system implementation using discrete EPROM, SRAM, and other discrete components, the system will consume operating power during the entire bus cycle. This is because the chip select inputs on the memory devices are usually active throughout the entire cycle. The AC power consumption of the ZPLD may be calculated using the composite frequency of the MCU address and control signals, as well as any other logic inputs to the ZPLD.

NOTE: The ZPSD4XX is rated for lower standby current (I_{SB}) than the PSD4XX.

Figure 2. Zero-Power Operation vs. Discrete Implementation



6.0 Design Flow

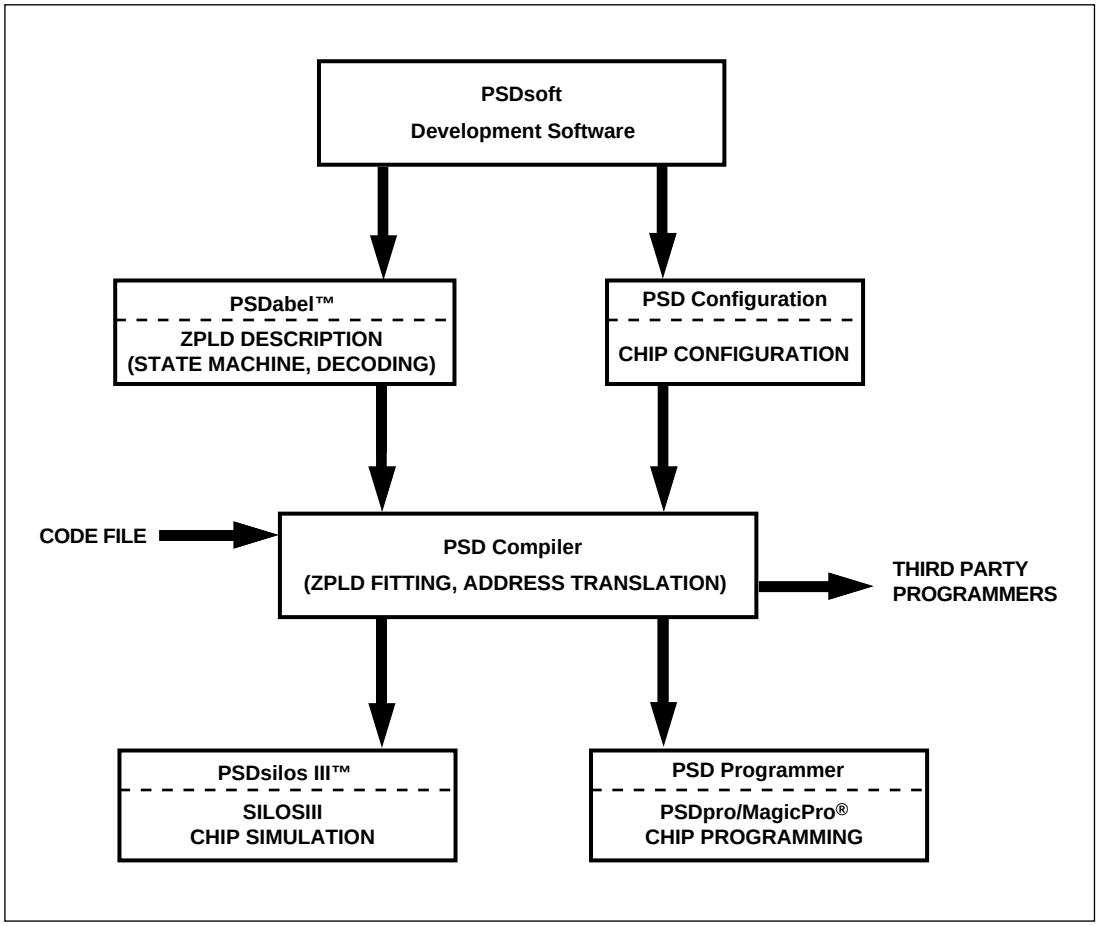
Shown in Figure 3 (below) is the software design flow for a PSD4XX device. PSDsoft—ST's software development suite—is used throughout the design phase. You start with a design file that is written in PSDabel—a high-level hardware description language (HDL). Before you compile your design, you must also configure the PSD4XX so it knows what signals to expect from your microprocessor and what pre-runtime options should be set (such as the security bit).

Once you have a design file and have configured the device, you are ready to run the Fitter and Address Translator. The Fitter accepts input from PSDabel and PSD Configuration, synthesizes this user logic and configuration, and fits the design to the PSD silicon. The Address Translator process allows the user to map the MCU firmware from a cross-compiler (in Intel HEX or S-Record format) into the NVM memory blocks within the PSD. As a result, the MCU firmware is merged with the logic and configuration definition of the PSD.

The output of the Address Translator and the Fitter is the required object file that is used by a programmer to program the PSD device. The object file includes chip configuration, the PLD fusemap, and MCU firmware information.

PSDsilosIII is an optional program that provides functional chip-level simulation of the PSD4XX. PSDsoft automatically creates files for input to the simulator. These files convey relevant design information to the simulator. As a result, the user only has to create a stimulus file since all of the signals and node names are taken from the design file.

Figure 3. PSDsoft Development Tools



7.0 PSD4XX Family

There are 12 unique devices in the PSD4XX family. The part classifications are based on ZPLD configuration and size, EPROM size, and data bus width. The features of each part are listed in Table 1. See the ordering information section at the end of this document.

Table 1. PSD4XX Product Matrix

Part #	Bus Bit	DPLD + GPLD			I/O Pins	PMU	EPROM K Bit	SRAM K Bit
		Inputs	Product Terms	Registered Macrocells				
401A1	x8/x16	37	113	8	40	Yes	256	16
411A1	x8	37	113	8	40	Yes	256	16
402A1	x8/x16	37	113	8	40	Yes	512	16
412A0	x8	37	113	8	40	Yes	512	–
412A1	x8	37	113	8	40	Yes	512	16
403A1	x8/x16	37	113	8	40	Yes	1024	16
413A1	x8	37	113	8	40	Yes	1024	16
401A2	x8/x16	59	126	24	40	Yes	256	16
411A2	x8	59	126	24	40	Yes	256	16
402A2	x8/x16	59	126	24	40	Yes	512	16
412A2	x8	59	126	24	40	Yes	512	16
403A2	x8/x16	59	126	24	40	Yes	1024	16
413A2	x8	59	126	24	40	Yes	1024	16

NOTE: PMU = Power Management Unit.

8.0 Table 2. PSD4XX Pin Descriptions

The following table describes the pin names and pin functions of the PSD4XX. Pins that have multiple names and/or functions are defined by user configuration.

Pin Name	Pin Function	Type	Function Descriptions
ADIO0 – ADIO15	Address/data bus	I/O	1. Address/data bus, multiplexed bus mode 2. Address bus, non-multiplexed bus mode
RD	Multiple Names 1. $\overline{\text{Read}}$ 2. $\overline{\text{E}}$ 3. $\overline{\text{DS}}$ 4. $\overline{\text{LDS}}$	I	Multiple functions 1. Read signal 2. E signal (Clock) 3. Data strobe signal 4. Low byte data strobe
WR	Multiple Names 1. $\overline{\text{WR}}$ 2. R/$\overline{\text{W}}$ 3. $\overline{\text{WRL}}$	I	Multiple functions 1. Write signal 2. Read-write signal 3. Low byte write signal
CSI	Chip Select Input	I	Active low, select PSD4XX standby mode if high.
RESET	Reset Input	I	Reset I/O ports, ZPLD/macrocells, and Configuration Registers. Active low.
CLKIN	Input clock	I	Clock input to ZPLD macrocells, ZPLD Array and APD counter. Connect to ground if Clock Input not used.
PA0 – PA7	I/O Port A	I/O	Multiple functions 1. I/O port 2. ZPLD/macrocell I/O port 3. Latched address outputs (PA0 – PA7) → (A0 – A7) 4. High address inputs (A16 – A23)
PB0 – PB7	I/O Port B	I/O	Multiple functions 1. I/O port 2. ZPLD/macrocell I/O port 3. Latched address outputs (PB0–PB7) → (A0–A7) or (A8–A15)
PC0 – PC7	I/O Port C	I/O CMOS or OD	Multiple functions 1. I/O port 2. ZPLD input port* 3. Latched address outputs (PC0 – PC7) → (A0–A7) 4. Data Port (D0 – D7, non-multiplexed bus)
PD0 – PD7	I/O Port D	I/O CMOS or OD	Multiple functions 1. I/O port 2. ZPLD input port* 3. Latched address outputs (PD0–PD7) → (A0–A7) or (A8–A15) 4. Data Port (D8–D15, non-multiplexed bus)

*Available only in PSD4XXA2 and ZPSD4XXA2 Series.

8.0 Table 2. PSD4XX Pin Descriptions (Cont.)

Pin Name	Pin Function	Type	Function Descriptions
PE0	Port PE, pin 0 1. $\overline{BHE}$ 2. $\overline{PSEN}$ 3. $\overline{WRH}$ 4. $\overline{UDS}$ 5. SIZ0 6. PE0 7. PE0 8. PE0	I/O	Multiple functions 1. High byte enable, 16 bit data 2. Read program memory, 8031 signal 3. Write high data byte 4. Upper Data Strobe 5. Byte enable, 68300 signal 6. I/O pin 7. ZPLD I/O pin 8. Latched Address Out – A0
PE1	Port PE, pin 1 1. ALE 2. PE1 3. PE1 4. PE1	I/O	Multiple functions 1. Address strobe 2. I/O pin 3. ZPLD I/O pin 4. Latched Address Out – A1
PE2	Port PE, pin 2 1. PE2 2. PE2 3. PE2	I/O	Multiple functions 1. I/O pin 2. ZPLD I/O pin* 3. Latched Address Out – A2
PE3	Port PE, pin 3 1. PE3 2. PE3 3. PE3	I/O	Multiple functions 1. I/O pin 2. ZPLD I/O pin* 3. Latched Address Out – A3
PE4	Port PE, pin 4 1. PE4 2. PE4 3. PE4	I/O	Multiple functions 1. I/O pin 2. ZPLD I/O pin* 3. Latched Address Out – A4
PE5	Port PE, pin 5 1. PE5 2. PE5 3. PE5	I/O	Multiple functions 1. I/O pin 2. ZPLD I/O pin* 3. Latched Address Out – A5
PE6	Port PE, pin 6 1. PE6 2. PE6 3. PE6	I/O	Multiple functions 1. I/O pin 2. ZPLD I/O pin* 3. Latched Address Out – A6
PE7	Port PE, pin 7 1. APD CLK 2. PE7 3. PE7 4. PE7	I/O	Multiple functions 1. Automatic Power Down Clock Input 2. I/O pin 3. ZPLD I/O pin* 4. Latched Address Out – A7
Vstdby	Vstdby	I	SRAM power pin for standby operation (battery backup)
V_{CC}	V_{CC}	I	V_{CC} power pin
GND	GND	I	Ground pin

*Available only in PSD4XXA2 and ZPSD4XXA2 Series.

9.0 The PSD4XX Architecture

PSD4XX consists of five major functional blocks:

- ZPLD Blocks
- Bus Interface
- I/O Ports
- Memory Block
- Power Management Unit

The functions of each block are described in the following sections. Many of the blocks perform multiple functions, and are user configurable. The chip configurations are specified by the user in the PSDsoft Development Software. Other configurations are specified by setting up the appropriate bits in the configuration registers during run time.

9.1 The ZPLD Block

The PSD4XX series devices provide two ZPLD configurations. The ZPLD in the **PSD4XXA1** devices has 8 registered macrocells, 8 combinatorial macrocells, and up to 113 product terms.

The **PSD4XXA2** has a full function ZPLD with 24 registered macrocells and up to 126 product terms.

9.1.1 The PSD4XXA1 ZPLD Block

Key Features

- 2 Embedded ZPLD devices
- 8 registered and 8 combinatorial macrocells
- Combinatorial/registered outputs
- Maximum 113 product terms
- Programmable output polarity
- User configured register clear/preset
- User configured register clock input
- 37 Inputs
- Accessible via 16 I/O pins
- Power Saving Mode
- UV-Erasable

General Description

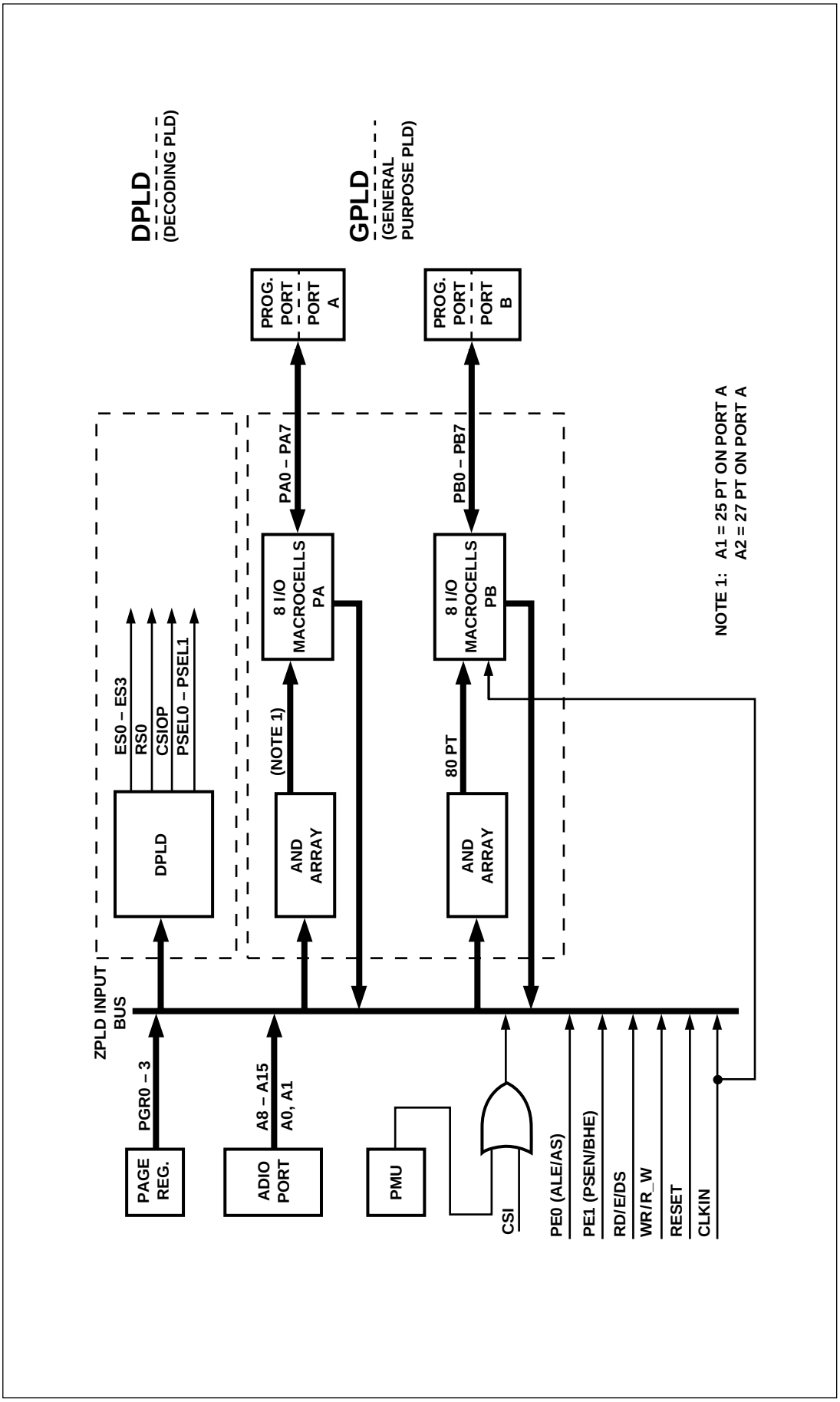
The ZPLD block has 2 embedded PLD devices:

- *DPLD*
  The Address Decoding PLD, generating select signals to internal I/O or memory blocks.
- *GPLD*
  The General Purpose PLD provides 8 registered and combinatorial programmable macrocells for general or complex logic implementation; dedicated to user application.

Figure 4 shows the architecture of the ZPLD. The PLD devices all share the same input bus. The true or complement of the 37 input signals are fed to the programmable AND-ARRAY. Names and sources of the input signals are shown in Table 3. The PB signals, depending on user configuration, can either be macrocell feedbacks or inputs from Port B.

The PSD4XX Architecture (cont.)

Figure 4. ZPLD Block Diagram



9.0 The PSD4XX Architecture (cont.)

Table 3. ZPLD Input Signals

Signal Name	From
PA0 – PA7	Port A inputs or Macrocell PA feedback
PB0 – PB7	Port B inputs or Macrocell PB feedback
PE0 – PE1	Port E inputs (signals ALE, PSEN/BHE)
PGR0 – PGR3	Page Mode Register
A8 – A15, A0, A1	MCU Address Lines
RD/E/DS	MCU bus signal
WR/R_W	MCU bus signal
CLKIN	Input Clock
RESET	Reset input
CSI	CSI input (ORed with power down from PMU)

9.1.1.1 The DPLD

The DPLD is used for internal address decoding generating the following eight chip select signals:

- *ES0 – ES3*
  EPROM selects, block 0 to block 3
- *RS0*
  SRAM block select
- *CSIOP*
  I/O Decoder chip select
- *PSEL0 – PSEL1*
  Peripheral I/O mode select signals

The I/O Decoder enabled by the CSIOP generates chip selects for on-chip registers or I/O ports based on address inputs A[7:0].

As shown in Figure 4, the DPLD consists of a large programmable AND ARRAY. There are a total of 37 inputs and 8 outputs. Each output consists of a single product term. Although the user can generate select signals from any of the inputs, the select signals are typically a function of the address and Page Register inputs. The select signals are defined by the user in the ABEL file (PSDabel).

The address line inputs to the DPLD include A0, A1 and A8 – A15. If more address lines are needed, the user can bring in the lines through Port A to the DPLD.

9.0 The PSD4XX Architecture (cont.)

9.1.1.2 The GPLD

The structure of the General Purpose PLD consists of a programmable AND ARRAY and 2 sets of I/O Macrocells. The ARRAY has 37 input signals, same as the DPLD. From these inputs, “ANDed” functions are generated as product term inputs to the macrocells. The I/O Macrocell sets are named after the I/O Ports they are linked to, e.g., the macrocells connected to Port B are named PB Macrocells. The PB macrocells are registered macrocells with D-type flip-flops, where PA consists of combinatorial macrocells.

9.1.1.3 TPA Macrocell Structure

Figure 5 shows the PA Macrocell block, which consists of 8 identical combinatorial macrocells. Each macrocell output can be connected to its own I/O pin on Port A. There is one user programmable global product term that is output from the GPLD’s AND ARRAY which is shared by all the macrocells in Port A:

- **PA.OE**
  Enable or tri-state Port A output pins

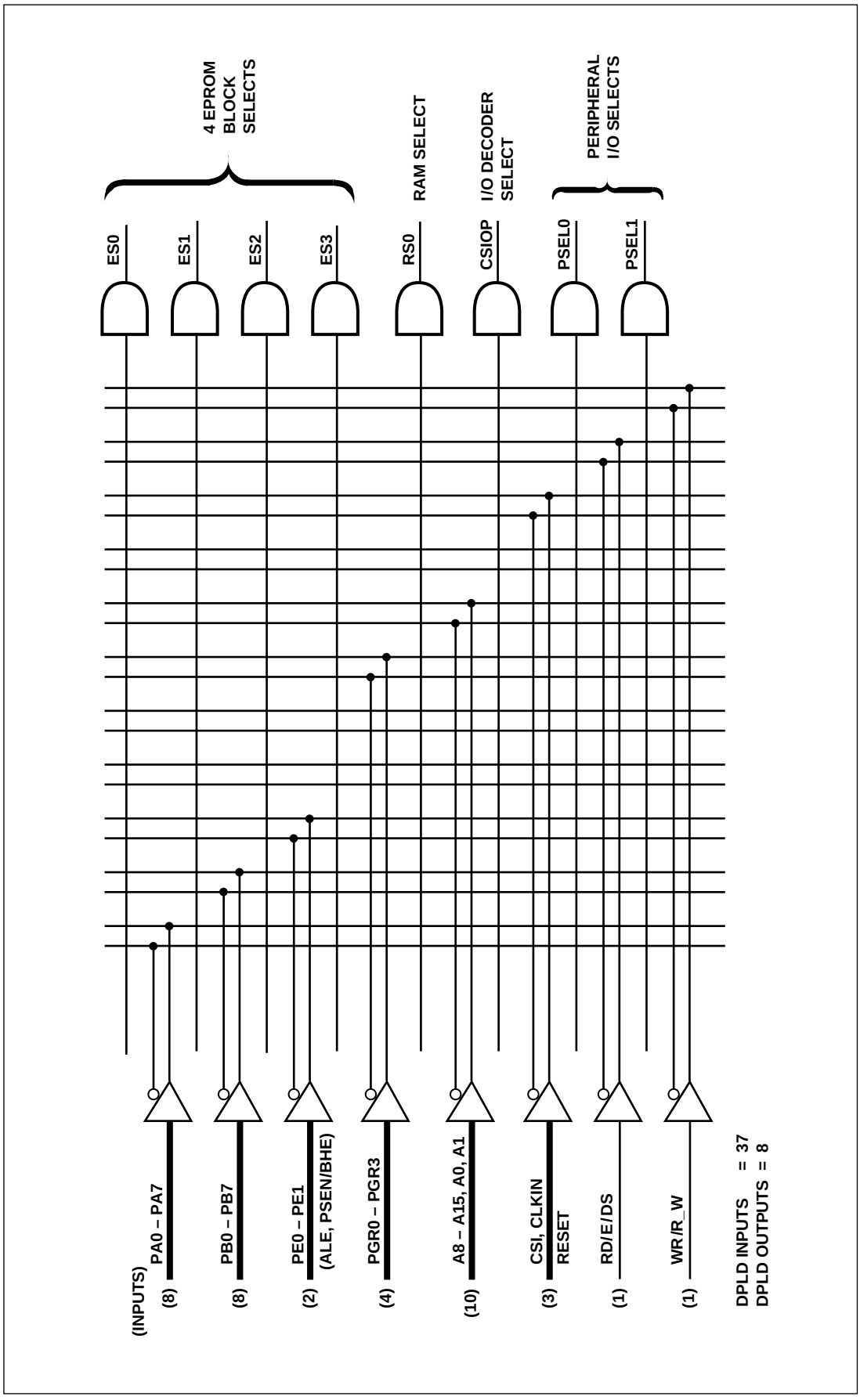
The circuit of a PA Macrocell is shown in Figure 6. There are 4 product terms from the GPLD’s AND ARRAY as inputs to the macrocell. Users can select the polarity of the output, and configure the macrocell to operate as:

- **GPLD Input**
  Use Port A pin as dedicated input

- **GPLD Output**
  Use Port A pin as dedicated output

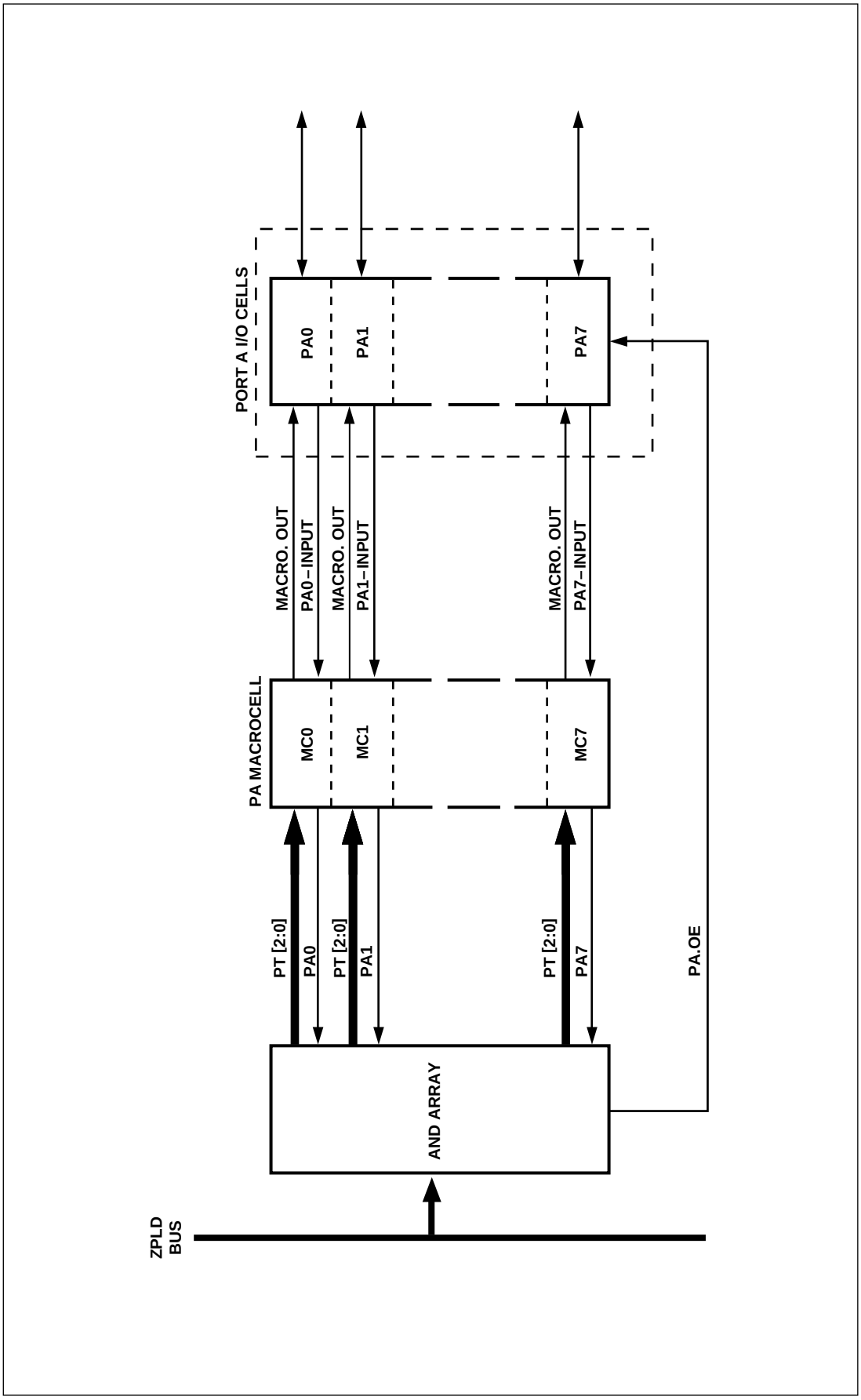
9.0 The PSD4XX Architecture (cont.)

Figure 5. DPLD Logic Array



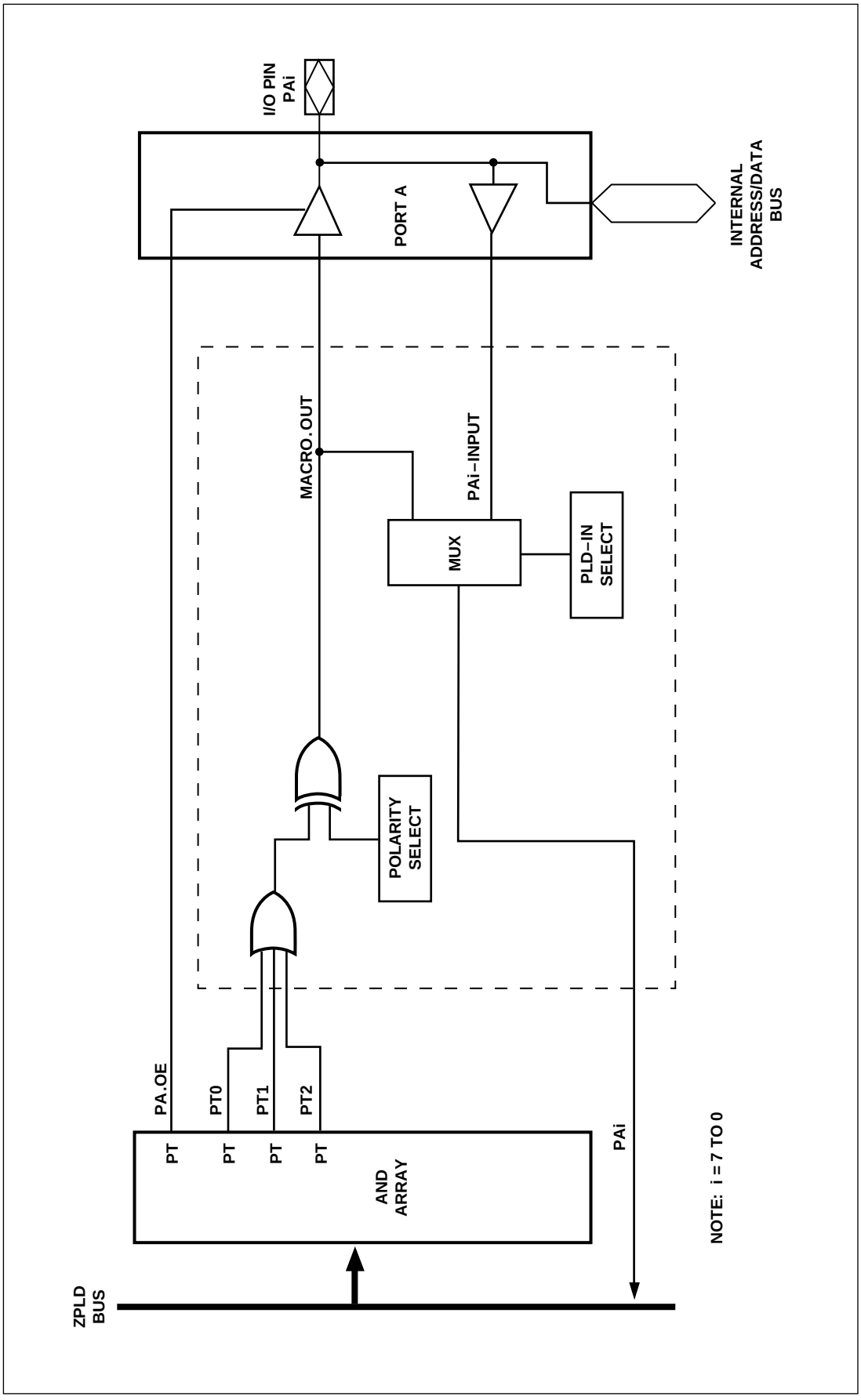
9.0 The PSD4XX Architecture (cont.)

Figure 6. PA Macrocell Block Diagram



9.0 The PSD4XX Architecture (cont.)

Figure 7. PA MacrocelI



9.0 The PSD4XX Architecture (cont.)

9.1.1.4 Port B Macrocell Structure

Figure 7 shows the PB Macrocell block, which consists of 8 identical macrocells. Each macrocell output can be connected to its own I/O pin on Port B. The two inputs, CLKIN and MACRO-RST, are used as clock and clear inputs to all the macrocells. The CLKIN comes directly from the CLKIN input pin. The MACRO-RST is the same as the Reset input pin except it is user configurable.

The circuit of a PB Macrocell is shown in Figure 8. There are 10 product terms from the GPLDs AND ARRAY as inputs to the macrocell. Users can select the polarity of the output, and configure the macrocell to operate as:

- **Registered Output**
  Select output from D flip flop.
- **Combinatorial Output**
  Select output from OR gate.
- **GPLD Input**
  Use Port B pin as dedicated input.
- **GPLD Output**
  Use Port B pin as dedicated output.
- **GPLD I/O**
  Use Port B pin as bidirectional pin.
- **Macrocell Feedback**
  Register feedback for state machine implementations or expander feedback from the combinatorial output, to possibly expand the number of product terms available to another macrocell.

  In case of "Buried Feedback", where the output of the macrocell is not connected to a Port B pin, Port B can be configured to perform other user defined I/O functions.

Each D flip flop in the macrocells has its own dedicated asynchronous clear, preset and clock input. The signals are defined as follow:

- **PRESET**
  Active only if defined by a product term (PBi.PR)
- **CLEAR**
  Two selectable inputs: Reset input and/or user defined product term (PBi.RE)
- **CLK**
  Two selectable inputs – CLKIN input or user defined product term (PBi.CLK).
  The macrocell is operated in Synchronous Mode if the clock input is CLKIN, and is in Asynchronous Mode if the clock is a product-term clock defined by the user.

Figure 9 shows the input/output path of a PB macrocell to the Port pin with which it is associated. If the Port pin is specified as a PB output pin in the PSDsoft, the MUX in the I/O Port Cell selects the PB Macrocell as an output of the Port pin. The output enable signal to the buffer in the I/O cell can be controlled by a product term from the AND Array.

If the Port pin is specified as a ZPLD input pin, the MUX in the PB Macrocell selects the Port input signal to be one of the 61 signals in the ZPLD Input Bus.

9.0 The PSD4XX Architecture (cont.)

9.1.1.5 The ZPLD Power Management

The ZPLD implements a Zero Power Mode, which provides considerable power savings for low to medium frequency operations. To enable this feature, the ZPLD Turbo bit in the Power Management Mode Register 0 (PMMR0) has to be turned off.

If none of the inputs to the ZPLD are switching for a time period of 90ns, the ZPLD puts itself into Zero Power Mode and the current consumption is minimal. The ZPLD will resume normal operation as soon as one or more of the inputs change state.

Two other features of the ZPLD provide additional power savings:

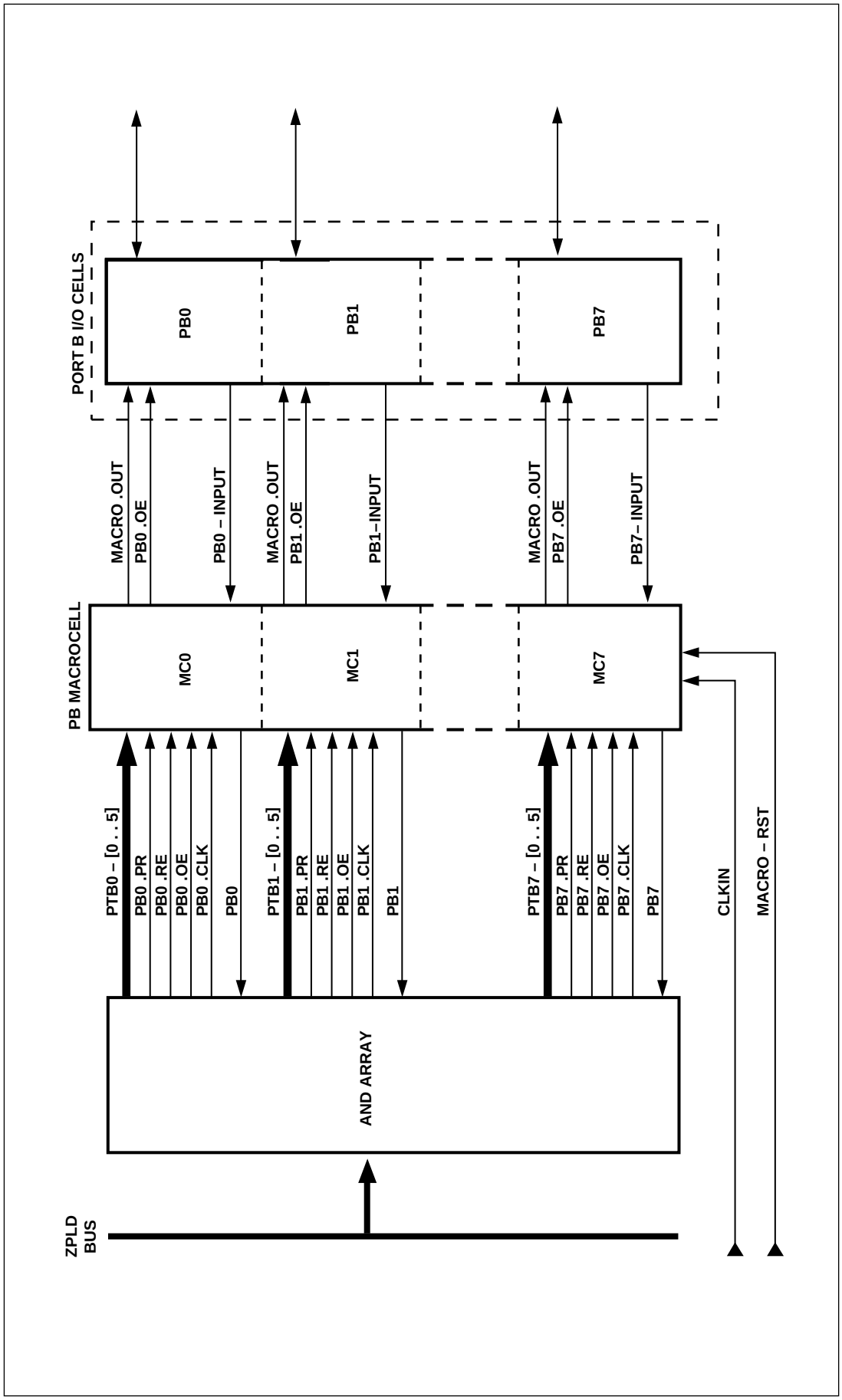
1. **Clock Disable:**
   Users can disable the clock input to the ZPLD and/or macrocells,thereby reducing AC power consumption.

2. **Product Term Disable:**
   Unused product terms in the ZPLD are disabled by the PSDsoft Software automatically for further power savings.

The ZPLD power configuration is described in the Power Management Unit section.

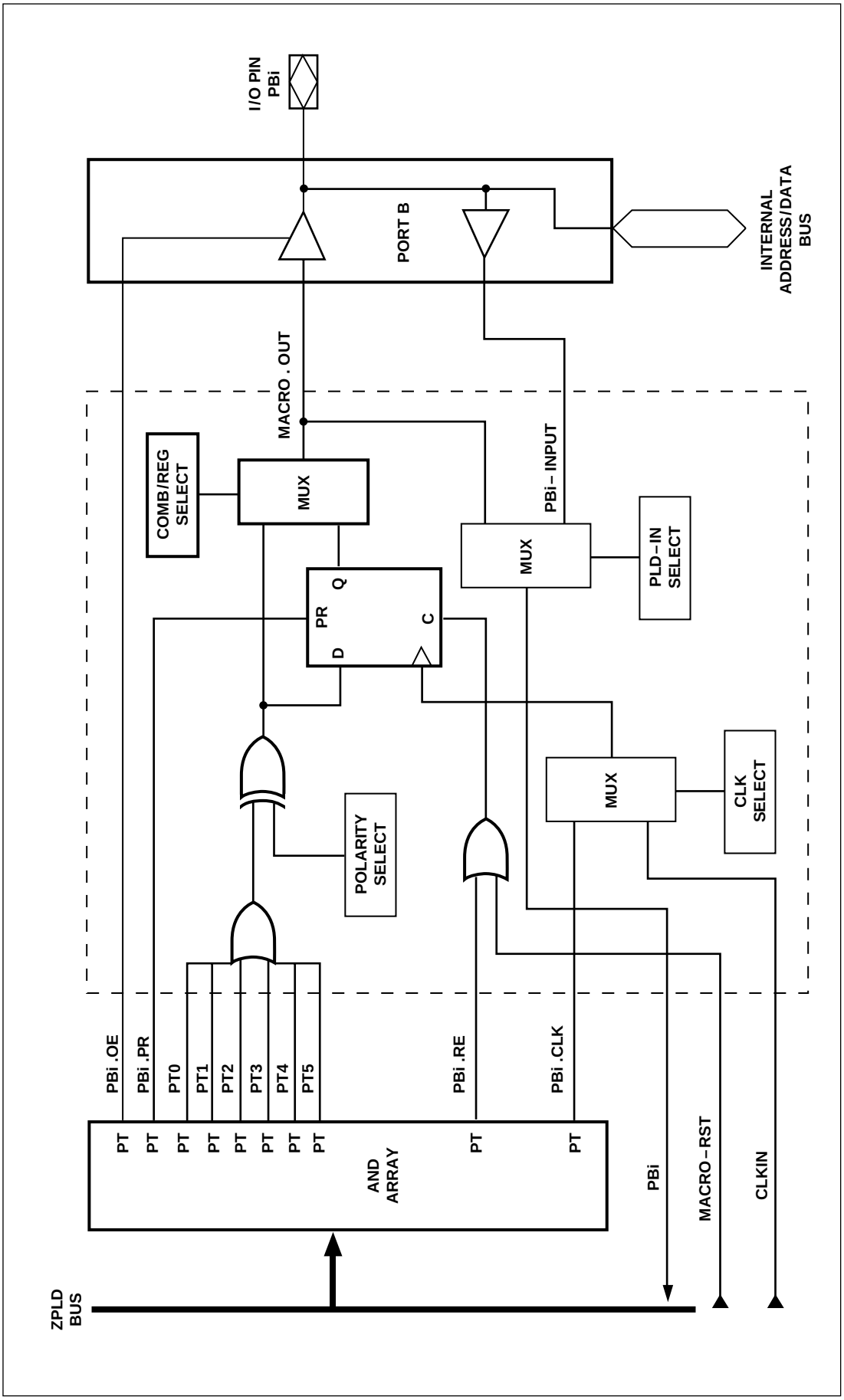
9.0 The PSD4XX Architecture (cont.)

Figure 8. PB Macrocell Block Diagram



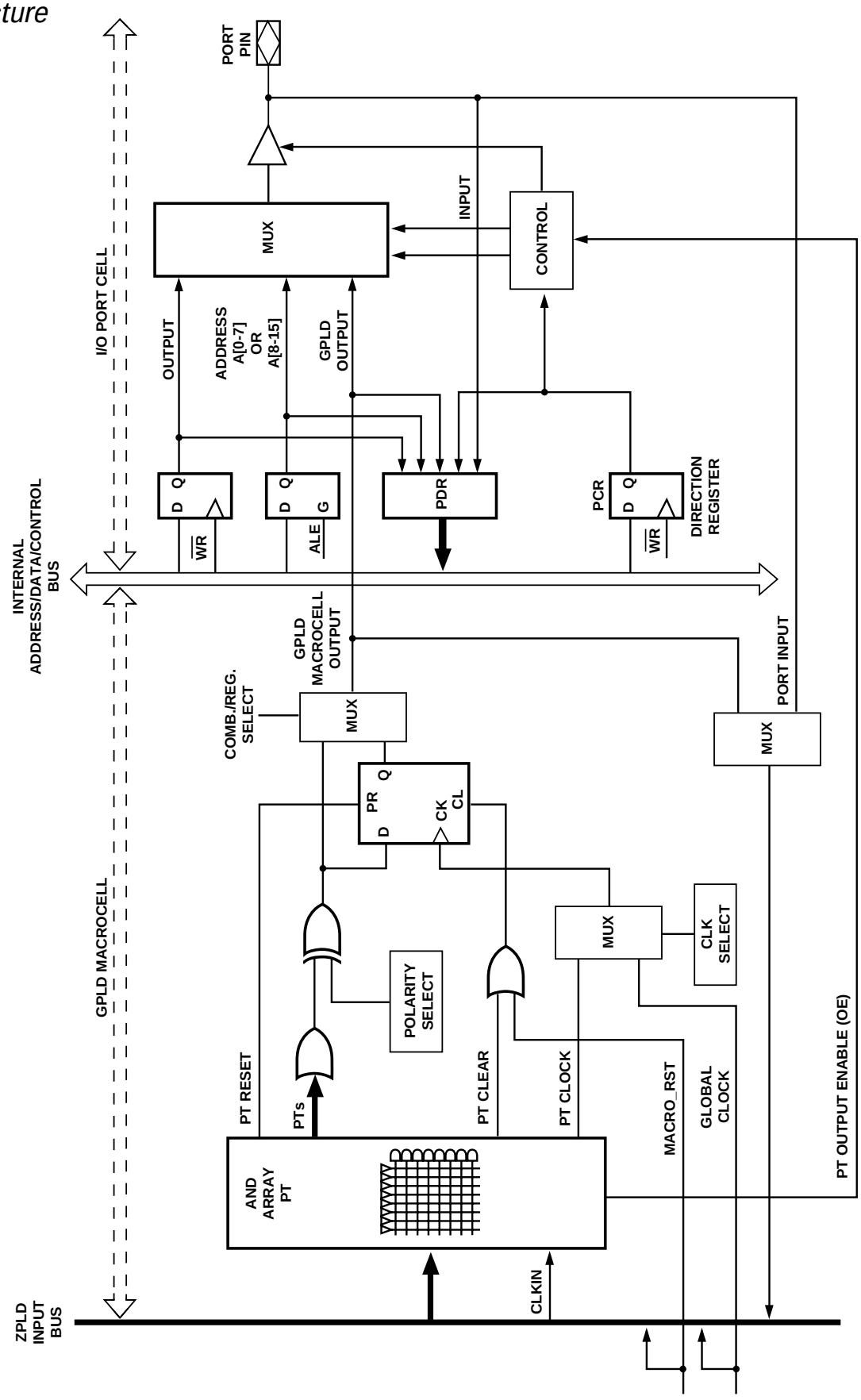
9.0 The PSD4XX Architecture (cont.)

Figure 9. PB MacrocelI



9.0 The PSD4XX Architecture (cont.)

Figure 10. PB Macrocell Input/Output Port



The PSD4XX Architecture (cont.)

9.1.2 The PSD4XXA2 ZPLD Block

Key Features

- 2 Embedded ZPLD devices
- 24 macrocells
- Combinatorial/registered outputs
- Maximum 126 product terms
- Programmable output polarity
- User configured register clear/preset
- User configured register clock input
- 59 Inputs
- Accessible via 24 I/O pins
- Power Saving Mode
- UV-Erasable

General Description

The ZPLD block has 2 embedded PLD devices:

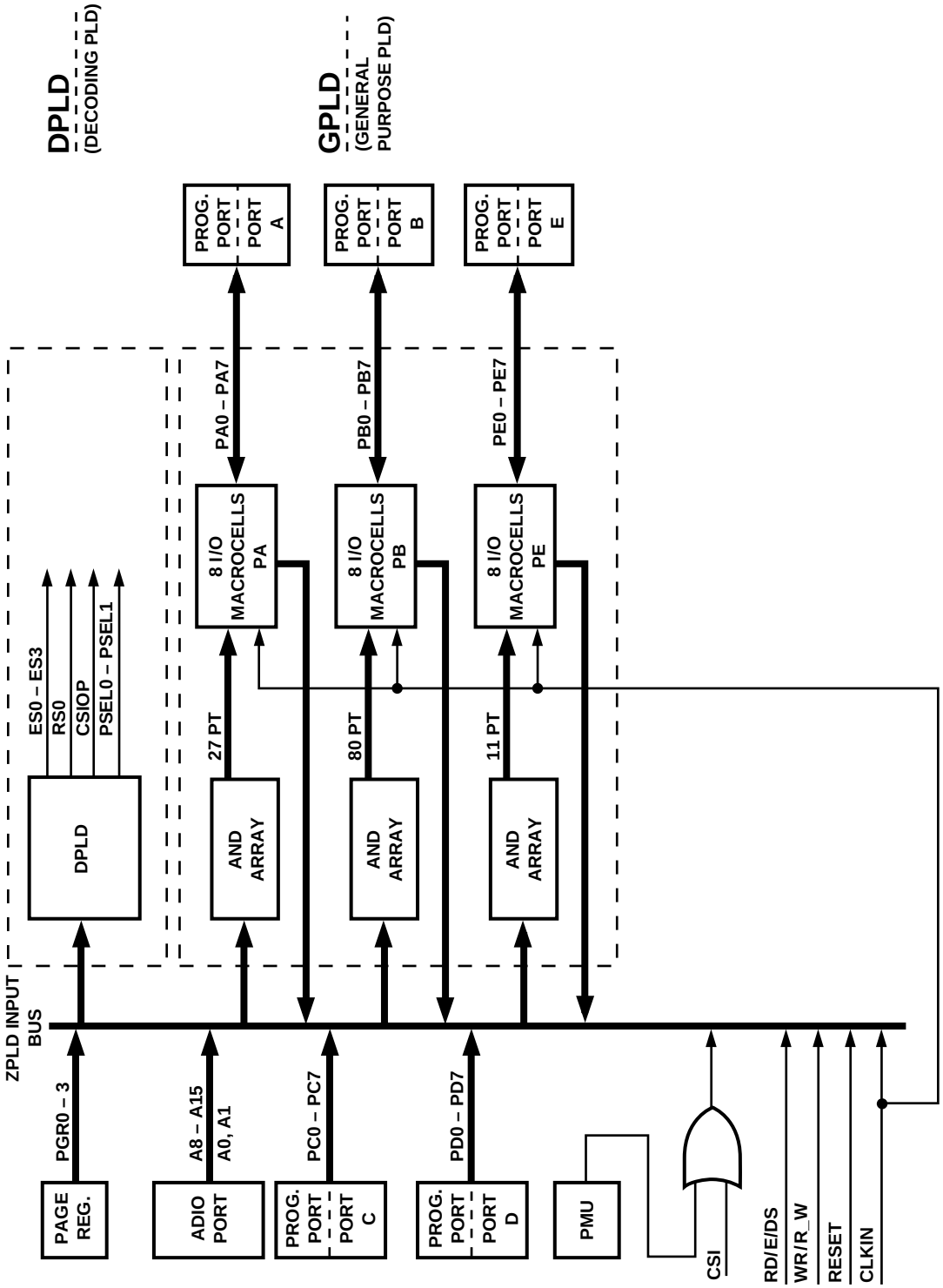
- *DPLD*
  The Address Decoding PLD, generating select signals to internal I/O or memory blocks.

- *GPLD*
  The General Purpose PLD provides 24 programmable macrocells for general or complex logic implementation; dedicated to user application.

Figure 11 shows the architecture of the ZPLD. The PLD devices all share the same input bus. The true or complement of the 59 input signals are fed to the programmable AND-ARRAY. Names and source of the input signals are shown in Table 4. The PA, PB, PE signals, depending on user configuration, can either be macrocell feedbacks or inputs from Port A, B or E.

The PSD4XX Architecture (cont.)

Figure 11. PSD4XXA2 ZPLD Block Diagram



The PSD4XX Architecture (cont.)

Table 4. ZPLD Input Signals

Signal Name	From
PA0 – PA7	Port A inputs or Macrocell PA feedback
PB0 – PB7	Port B inputs or Macrocell PB feedback
PE0 – PE7	Port E inputs or Macrocell PE feedback
PC0 – PC7	Port C inputs
PD0 – PD7	Port D inputs
PGR0 – PGR3	Page Mode Register
A8 – A15, A0, A1	MCU Address Lines
RD/E/DS	MCU bus signal
WR/R_W	MCU bus signal
CLKIN	Input Clock
RESET	Reset input
CSI	$\overline{CSI}$ input (ORed with power down from PMU)

9.1.2.1 The DPLD

The DPLD is used for internal address decoding generating the following eight chip select signals:

- *ES0 – ES3*
  EPROM selects, block 0 to block 3
- *RS0*
  SRAM block select
- *CSIOP*
  I/O Decoder chip select
- *PSEL0 – PSEL1*
  Peripheral I/O mode select signals

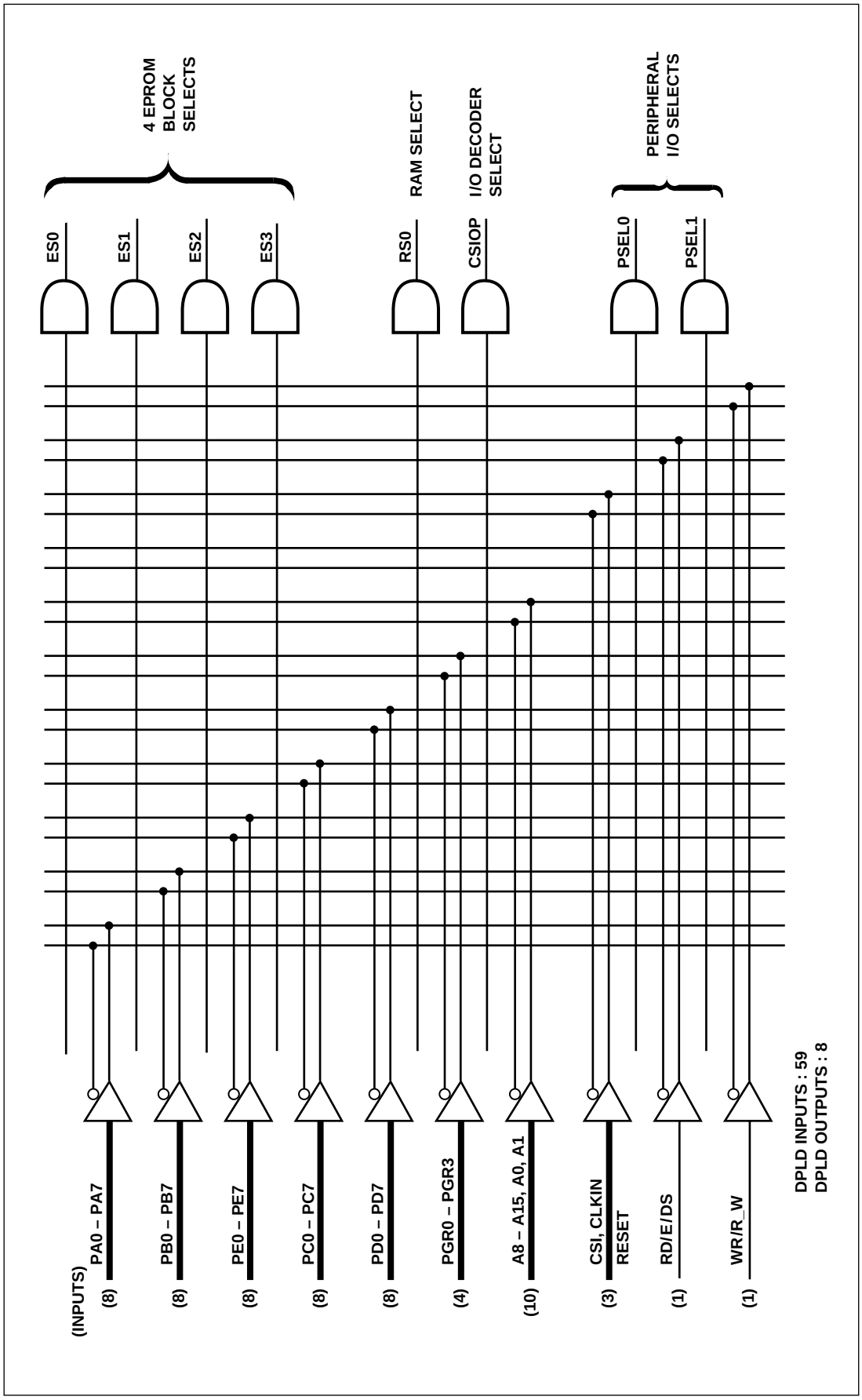
The I/O Decoder enabled by the CSIOP generates chip selects for on-chip registers or I/O ports based on address inputs A[7:0].

As shown in Figure 12, the DPLD consists of a large programmable AND ARRAY. There are a total of 59 inputs and 8 outputs. Each output consists of a single product term. Although the user can generate select signals from any of the inputs, the select signals are typically a function of the address and Page Register inputs. The select signals are defined by the user in the ABEL file (PSDabel).

The address line inputs to the DPLD include A0, A1 and A8 – A15. If more address lines are needed, the user can bring in the lines through Port A to the DPLD.

The PSD4XX Architecture (cont.)

Figure 12. DPLD Logic Array



The PSD4XX Architecture (cont.)

9.1.2.2 The GPLD

The structure of the General Purpose PLD consists of a programmable AND ARRAY and 3 sets of I/O Macrocells. The ARRAY has 59 input signals, same as the DPLD. From these inputs, “ANDed” functions are generated as product term inputs to the macrocells. The I/O Macrocell sets are named after the I/O Ports they are linked to, e.g., the macrocells connected to Port A are named PA Macrocells. The 3 sets of macrocells, PA, PB and PE, are similar in structure and function.

Figure 13 shows the output/input path of a GPLD macrocell to the Port pin with which it is associated. If the Port pin is specified as a GPLD output pin in PSDsoft, the MUX in the I/O Port Cell selects the GPLD macrocell as an output of the Port pin. The output enable signal to the buffer in the I/O cell can be controlled by a product term from the AND ARRAY.

If the Port pin is specified as a ZPLD input pin, the MUX in the GPLD macrocell selects the Port input signal to be one of the 61 signals in the ZPLD Input Bus.

9.1.2.3 Port A Macrocell Structure

Figure 14 shows the PA Macrocell block, which consists of 8 identical macrocells. Each macrocell output can be connected to its own I/O pin on Port A. There are 3 user programmable global product terms output from the GPLD’s AND ARRAY which are shared by all the macrocells in Port A:

- **PA.OE**
  Enable or tri-state Port A output pins
- **PA.PR**
  Preset D flip flop in the macrocells
- **PA.RE**
  Reset/Clear D flip flop in the macrocells

Two other inputs, CLKIN and MACRO-RST, are used as clock and clear inputs to the D flip flop. The CLKIN comes directly from the CLKIN input pin. The MACRO-RST is the same as the Reset input pin except it is user configurable.

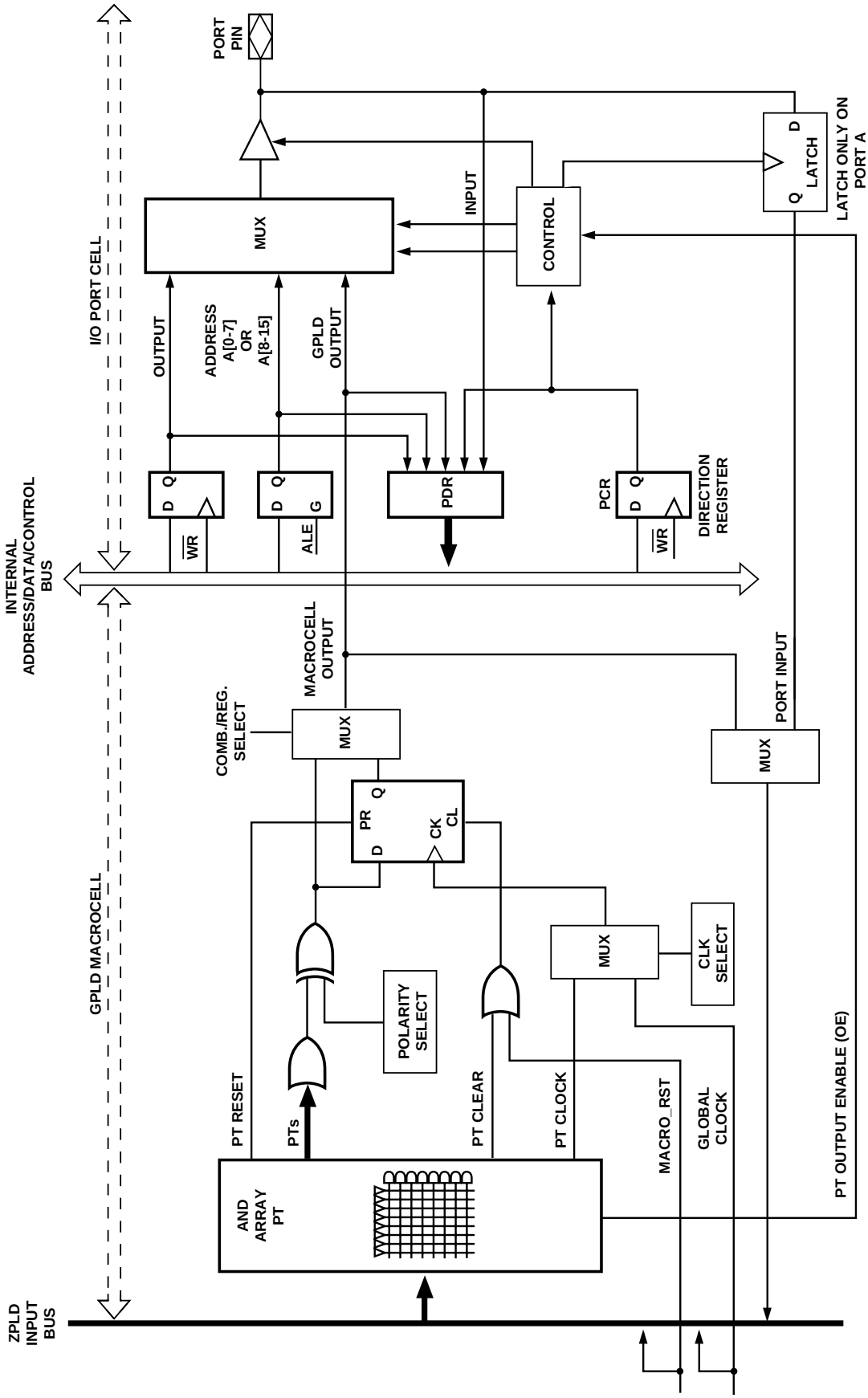
The circuit of a PA Macrocell is shown in Figure 15. There are 6 product terms from the GPLD’s AND ARRAY as inputs to the macrocell. Users can select the polarity of the output, and configure the macrocell to operate as:

- **Registered Output**
  Select output from D flip flop
- **Combinatorial Output**
  Select output from OR gate
- **GPLD Input**
  Use Port A pin as dedicated input
- **GPLD Output**
  Use Port A pin as dedicated output
- **GPLD I/O**
  Use Port A pin as bidirectional pin
- **Macrocell Feedback**
  Register feedback for state machine implementations or expander feedback from the combinatorial output, to expand the number of product terms available to another macrocell.

  In case of "Buried Feedback", where the output of the macrocell is not connected to a Port A pin, Port A can be configured to perform other user defined I/O functions.

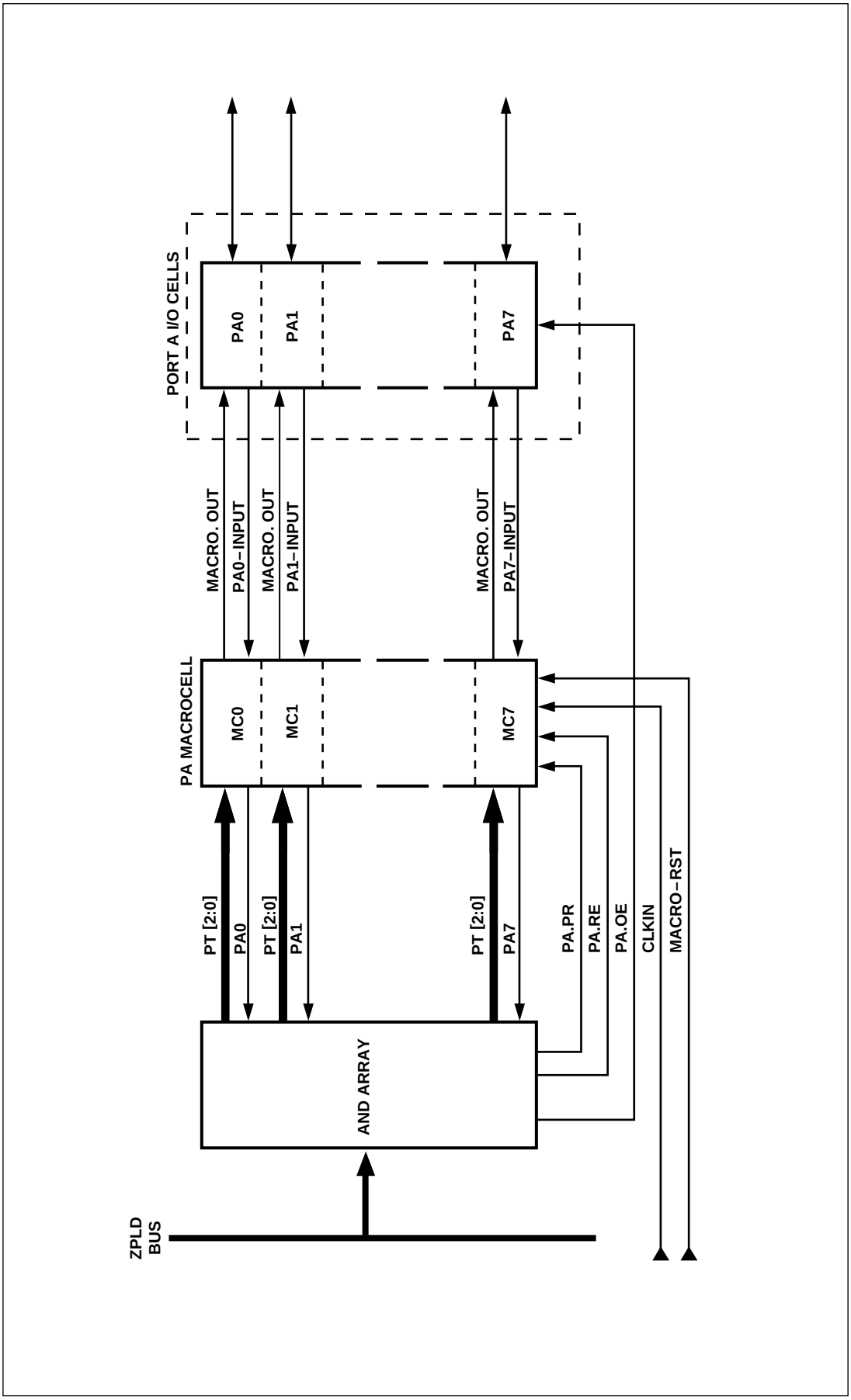
The two global product terms assigned for asynchronous clear (PA.RE) and preset (PA.PR) are mainly for proper PA Macrocell initialization. The macrocell flip-flop can also be cleared during reset by MACRO-RST, if such an option is chosen. The clock source is always the input clock CLKIN.

Figure 13. GPLD Macrocell Input/Output Port



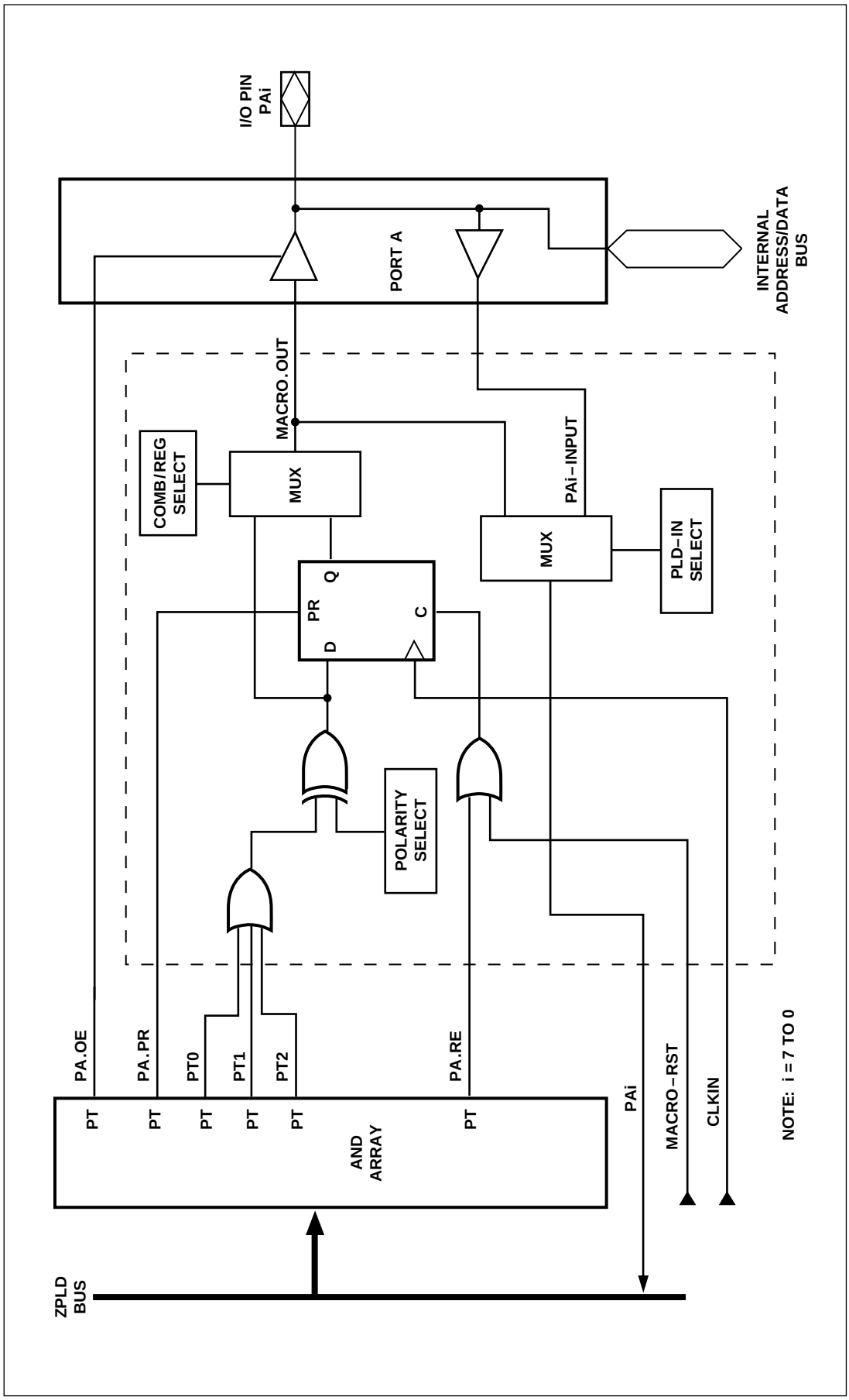
The PSD4XX Architecture (cont.)

Figure 14. PA MacrocelI Block Diagram



The PSD4XX Architecture (cont.)

Figure 15. PSD4XXA2 PA MacrocelI



The PSD4XX Architecture (cont.)

9.1.2.4 Port B Macrocell Structure

Figure 16 shows the PB Macrocell block, which consists of 8 identical macrocells. Each macrocell output can be connected to its own I/O pin on Port B. The two inputs, CLKIN and MACRO-RST, are used as clock and clear inputs to all the macrocells. The CLKIN comes directly from the CLKIN input pin. The MACRO-RST is the same as the Reset input pin except it is user configurable.

The circuit of a PB Macrocell is shown in Figure 17. There are 10 product terms from the GPLD's AND ARRAY as inputs to the macrocell. Users can select the polarity of the output, and configure the macrocell to operate as:

- **Registered Output**
  Select output from D flip flop.
- **Combinatorial Output**
  Select output from OR gate.
- **GPLD Input**
  Use Port B pin as dedicated input.
- **GPLD Output**
  Use Port B pin as dedicated output.
- **GPLD I/O**
  Use Port B pin as bidirectional pin.
- **Macrocell Feedback**
  Register feedback for state machine implementations or expander feedback from the combinatorial output, to possibly expand the number of product terms available to another macrocell.

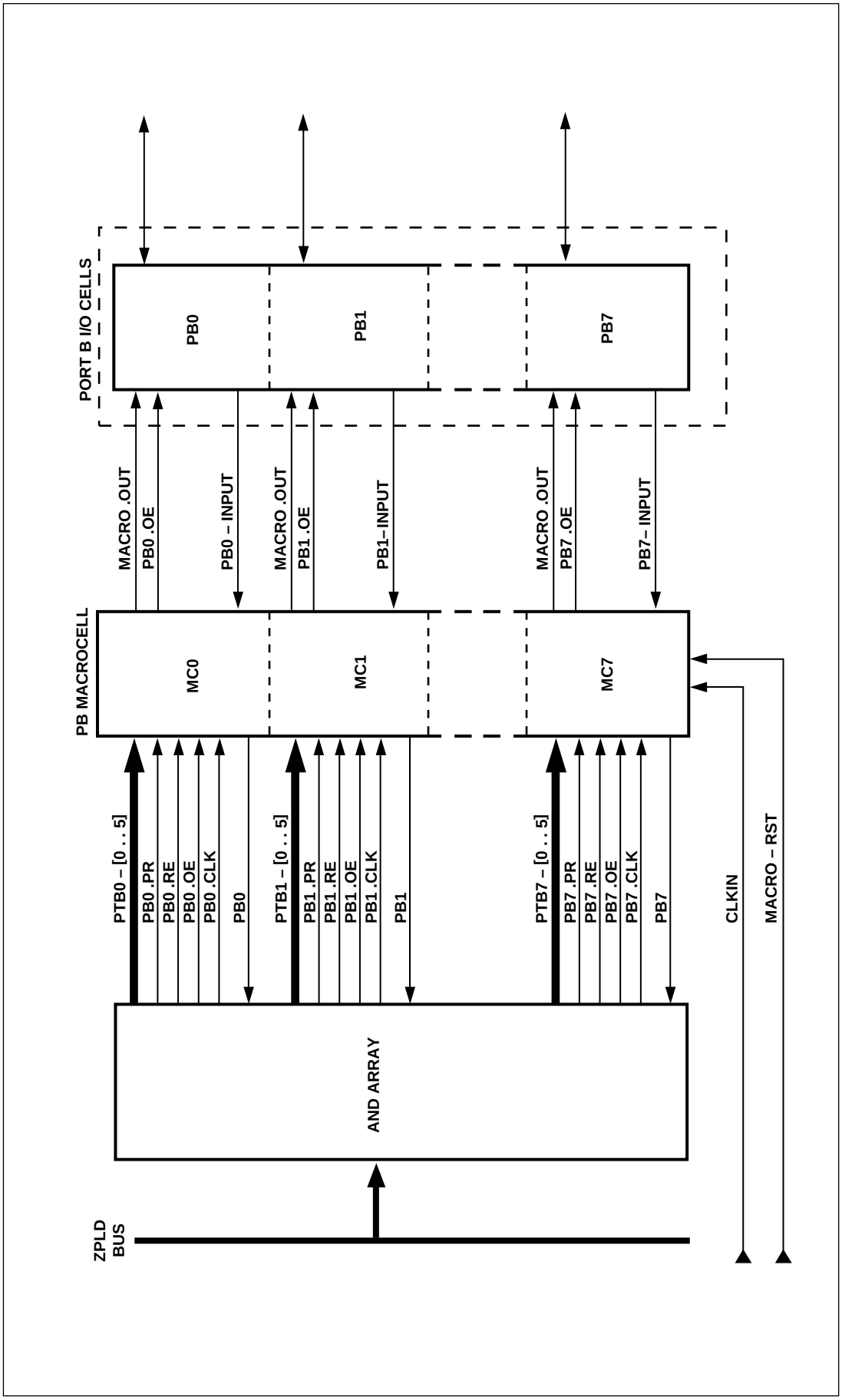
  In case of "Buried Feedback", where the output of the macrocell is not connected to a Port B pin, Port B can be configured to perform other user defined I/O functions.

Each D flip flop in the macrocells has its own dedicated asynchronous clear, preset and clock input. The signals are defined as follow:

- **PRESET**
  Active only if defined by a product term (PBx.PR)
- **CLEAR**
  Two selectable inputs: Reset input or user defined product term (PBx .RE)
- **CLK**
  Two selectable inputs – CLKIN input or user defined product term (PBx.CLK). The macrocell is operated in Synchronous Mode if the clock input is CLKIN, and is in Asynchronous Mode if the clock is a product-term clock defined by the user.

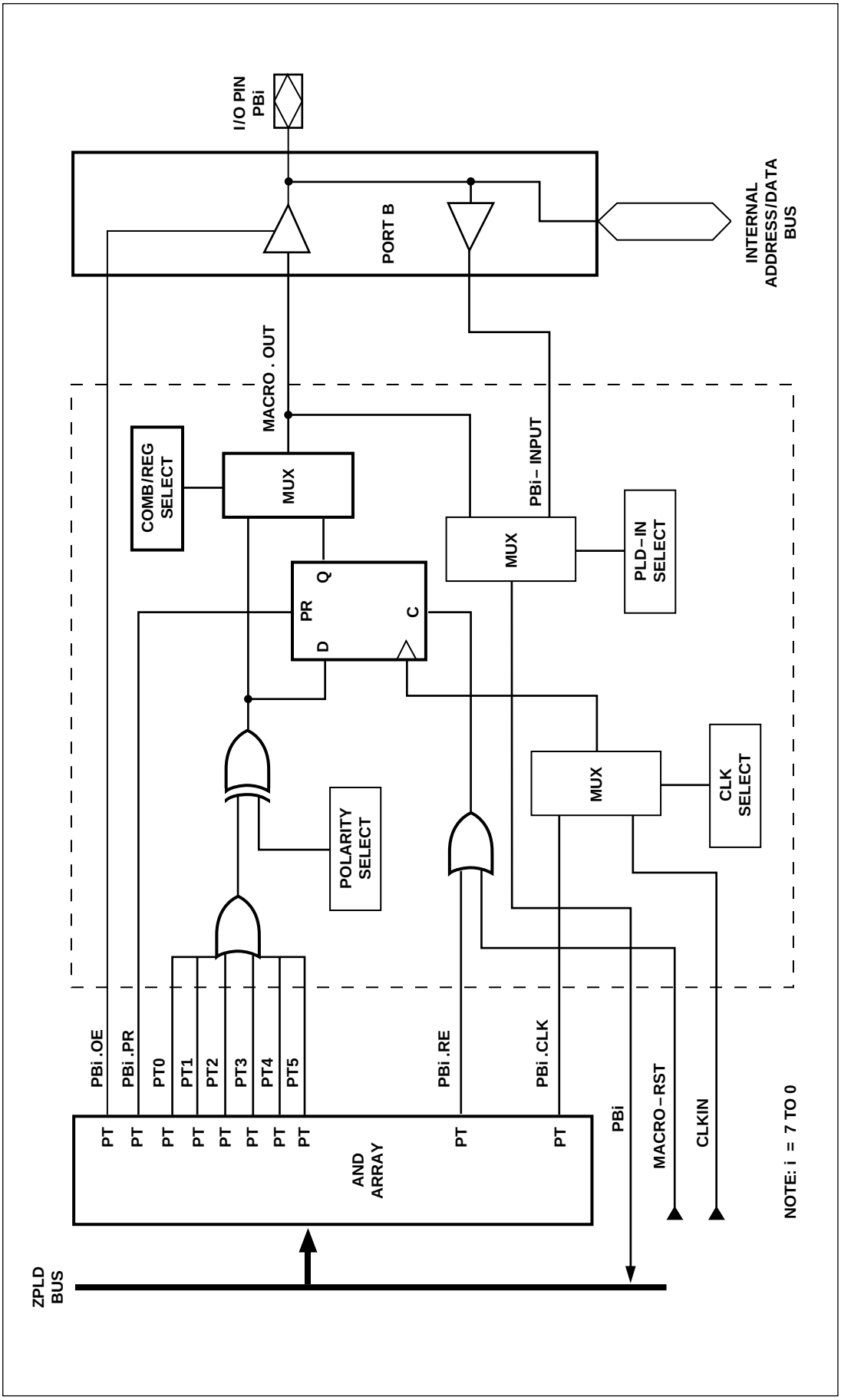
The PSD4XX Architecture (cont.)

Figure 16. PSD4XXA2 PB Macrocell Block Diagram



The PSD4XX Architecture (cont.)

Figure 17. PSD4XXA2 PB MacrocelI



The PSD4XX Architecture (cont.)

9.1.2.5 Port E Macrocell Structure

Figure 18 shows the PE Macrocell block, which consists of 8 identical macrocells. Each macrocell output can be connected to its own I/O pin on Port E. There are 3 user programmable global product terms output from the GPLD's AND ARRAY which are shared by all the macrocells in Port E:

- **PE.OE**
  Enable or tri-state Port PE output pins
- **PE.PR**
  Preset D flip flop in the macrocells
- **PE.RE**
  Reset/Clear D flip flop in the macrocells

Two other inputs, CLKIN and MACRO-RST, are used as clock and clear inputs to the D flip flop. The CLKIN comes directly from the CLKIN input pin. The MACRO-RST is the same as the Reset input pin except it is user configurable.

The circuit of a PE Macrocell is shown in Figure 19. There is only one product term from the GPLD's AND ARRAY as input to the macrocell. Users can select the polarity of the output and configure the macrocell to operate as:

- **Registered Output**
  Select output from D flip flop
- **Combinatorial Output**
  Select output from OR gate
- **GPLD Input**
  Use Port E pin as dedicated input
- **GPLD Output**
  Use Port E pin as dedicated output
- **GPLD I/O**
  Use Port E pin as bidirectional pin
- **Macrocell Feedback**
  Register feedback for state machine implementations or expander feedback from the combinatorial output, to possibly expand the number of product terms available to another macrocell.

  In case of "Buried Feedback", where the output of the macrocell is not connected to Port E pin, Port E can be configured to perform other user defined I/O functions. If pins PE0 and PE1 are used as bus control signal inputs (ALE, PSEN/BHE), the corresponding macrocells' feedbacks are disabled. The bus control signals are connected to the ZPLD Input Bus.

The two global product terms assigned for asynchronous clear (PE.RE) and preset (PE.PR) are for proper PE Macrocell initialization.

The macrocell flip-flop can also be cleared during reset by MACRO-RST as an option. The clock source is always the input clock CLKIN.

The PSD4XX Architecture (cont.)

9.1.2.6 The ZPLD Power Management

The ZPLD implements a Zero Power Mode, which provides considerable power savings for low to medium frequency operations. To enable this feature, the ZPLD Turbo bit in the Power Management Mode Register 0 (PMMR0) has to be turned off.

If none of the inputs to the ZPLD are switching for a time period of 70ns, the ZPLD puts itself into Zero Power Mode and the current consumption is minimal. The ZPLD will resume normal operation as soon as one or more of the inputs change state.

Two other features of the ZPLD provide additional power savings:

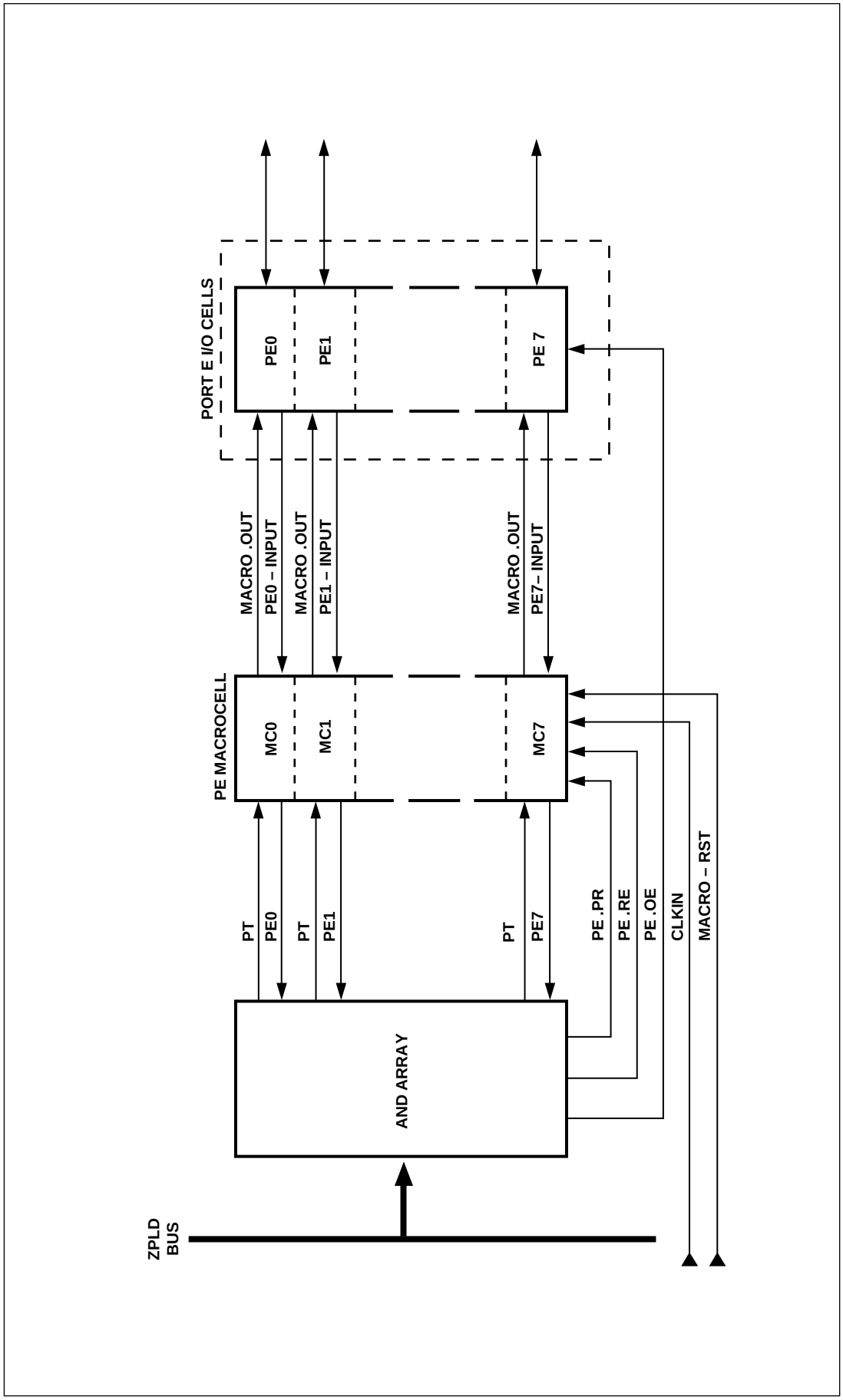
1. **Clock Disable:**
   Users can disable the clock input to the ZPLD and/or macrocells, thereby reducing AC power consumption.

2. **Product Term Disable:**
   Unused product terms in the ZPLD are disabled by the PSDsoft Software automatically for further power savings.

The ZPLD power configuration is described in the Power Management Unit section.

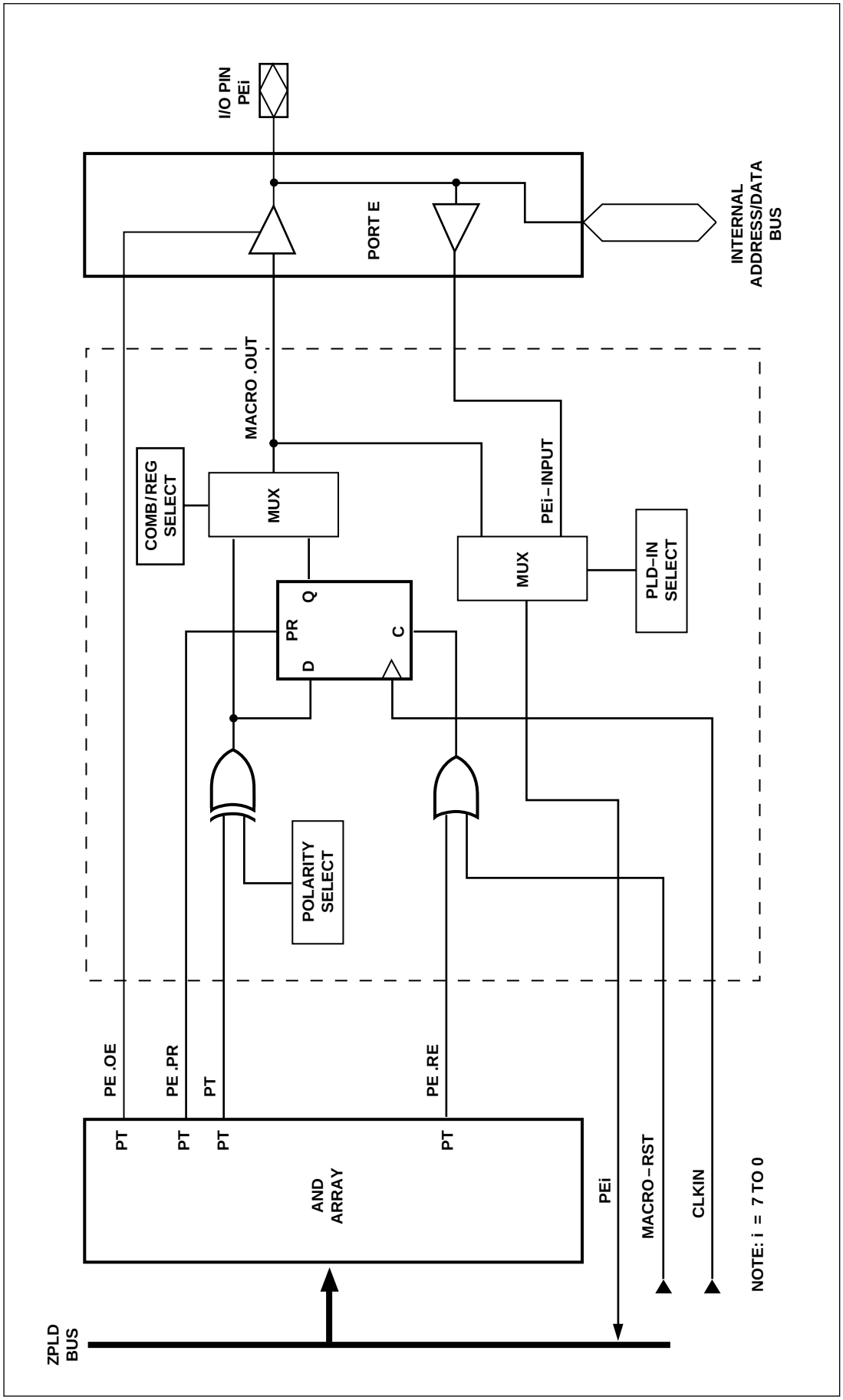
The PSD4XX Architecture (cont.)

Figure 18. PE Macrocell Block Diagram



The PSD4XX Architecture (cont.)

Figure 19. PE MacroeII



The PSD4XX Architecture (cont.)

9.2 Bus Interface

The Bus Interface is very flexible and can be configured to interface to most microcontrollers with no glue logic. Table 5 lists some of the bus types to which the Bus Interface is able to interface.

Table 5. Typical Microcontroller Bus Types

Multiplexed	Data Bus Width	Bus Control Signals	Microcontroller
Mux	8	$\overline{WR}$, $\overline{RD}$, $\overline{PSEN}$, A0	8031/80C51
Mux/ Non-mux	8/16	R/$\overline{W}$, E, $\overline{BHE}$, A0	68HC11
Mux	8/16	$\overline{WR}$, $\overline{RD}$, $\overline{BHE}$, A0	80C196/80C186
Mux	16	$\overline{WRL}$, $\overline{RD}$, $\overline{WRH}$, A0	80C196SP
Non-mux	16	R/$\overline{W}$, $\overline{LDS}$, $\overline{UDS}$	68302
Non-mux	8/16	R/$\overline{W}$, $\overline{DS}$, SIZ0, A0	68340
Non-mux	16	R/$\overline{W}$, $\overline{DS}$, $\overline{BHE}$, $\overline{BLE}$	68330, 68331
Non-mux	8	$\overline{RD}$, $\overline{WR}$	68HC05C
Non-mux	16	R/$\overline{W}$, E, $\overline{LSTRB}$, A0	68HC12
Non-mux	16	R/$\overline{W}$, $\overline{DS}$	68HC16

9.2.1 Bus Interface Configuration

The Bus Interface Logic is user configurable. The type of bus interface is specified by the user in the PSDsoft software (PSD configuration). The bus control input pins have multi-function capabilities. By choosing the right configuration, the PSD4XX is able to interface to most microcontrollers, including the ones listed in Table 5. In Table 6, the names of the bus control input signal pins and their multiple functions are shown. For example, Pin PE0 can be configured by the PSD configuration software to perform any one of the five functions. Examples on the interface between the PSD4XX and some typical microcontrollers are shown in following sections.

The PSD4XX Architecture (cont.)

Table 6. Alternate Pin Functions

Pin Name	Pin Function 1	Pin Function 2	Pin Function 3	Pin Function 4	Pin Function 5
RD	$\overline{RD}$	E	$\overline{DS}$	$\overline{LDS}$	
WR	$\overline{WR}$	R/$\overline{W}$	$\overline{WRL}$		
PE0	$\overline{BHE}$	$\overline{PSEN}$	$\overline{WRH}$	$\overline{UDS}$	SIZ0
PE1	ALE				
AD0	A0	$\overline{BLE}$			

9.2.2 PSD4XX Interface To a Multiplexed Bus

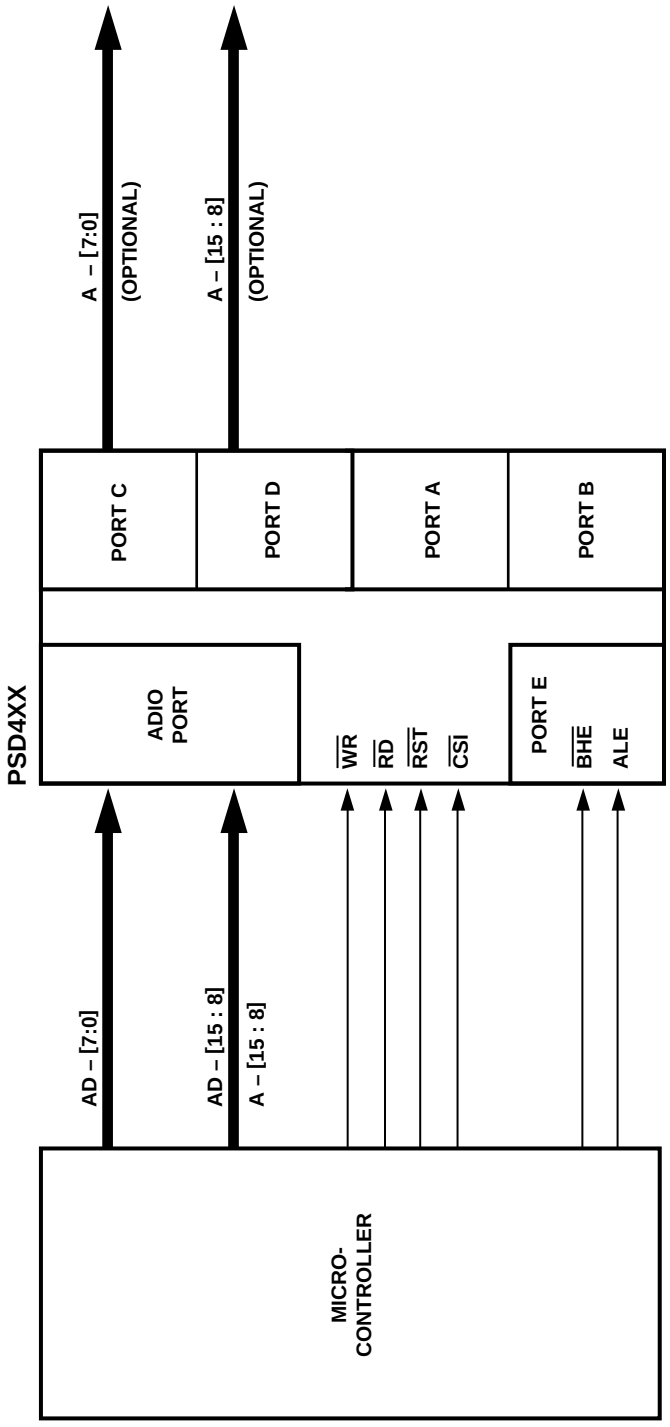
Figure 20 shows a typical connection to a microcontroller with a multiplexed bus. The ADIO port of the PSD4XX is connected directly to the microcontroller address/data bus (AD0-AD15 for 16 bit bus). The ALE input signal latches the address lines internally. In a read bus cycle, data is driven out through the ADIO Port transceivers after the specified access time. The internal ADIO Port connection for a 16 bit multiplexed bus is shown in Figure 21. The ADIO Port is in tri-state mode if none of the PSD4XX internal devices are selected.

9.2.3 PSD4XX Interface To Non-Multiplexed Bus

Figure 22 shows a PSD4XX interfacing to a microcontroller with a non-multiplexed address/data bus. The address bus is connected to the ADIO Port, and the data bus is connected to Port C and/or Port D, depending on the bus width. There is no need for the ADIO Port to latch the address internally, but the user is offered the option to do so in the PSD4XX PSDsoft Software. The data Ports are in tri-state mode when the PSD4XX is not accessed by the microcontroller.

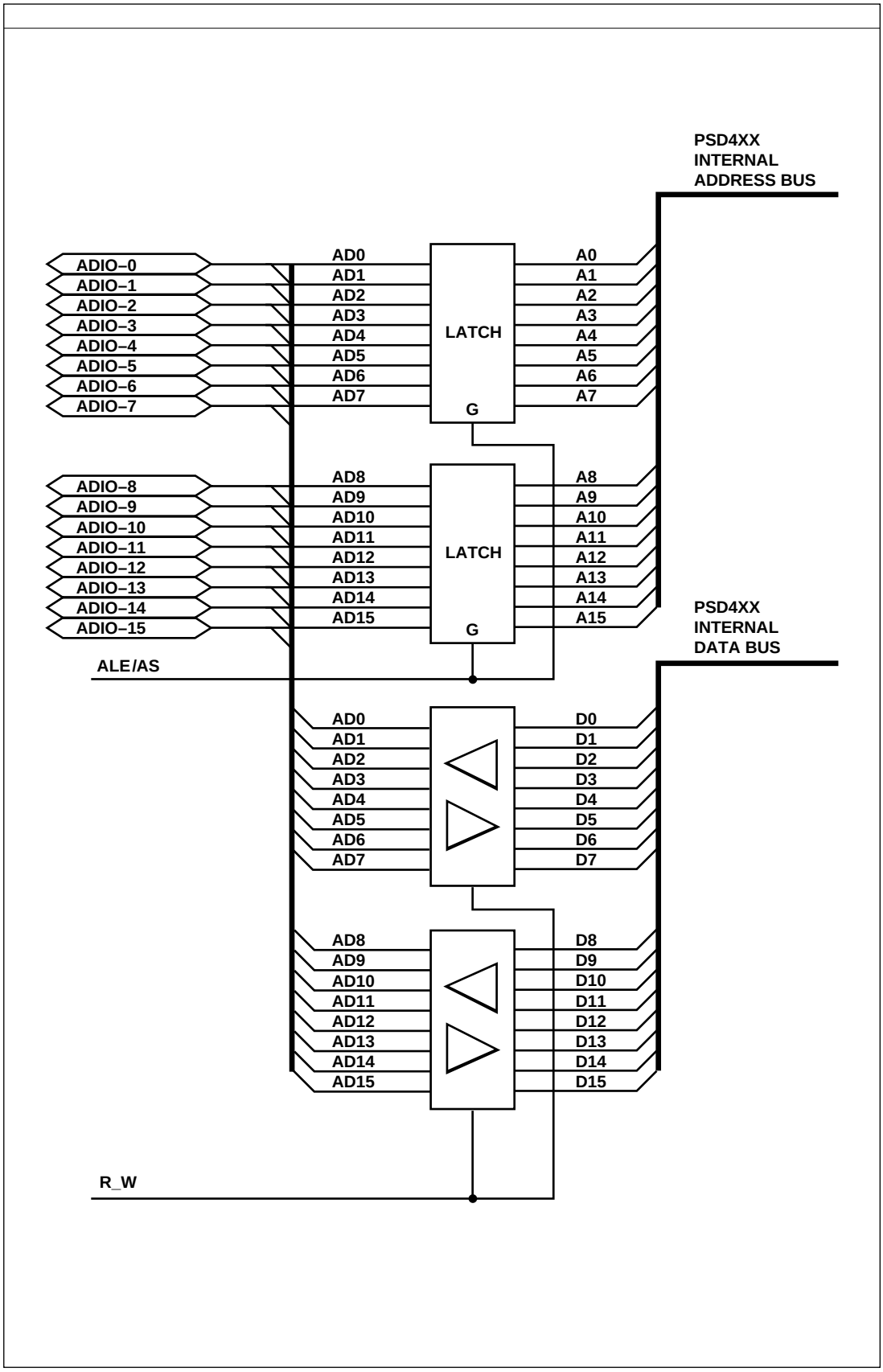
The PSD4XX Architecture (cont.)

Figure 20. Multiplexed Bus, 8 or 16-Bit Data Bus



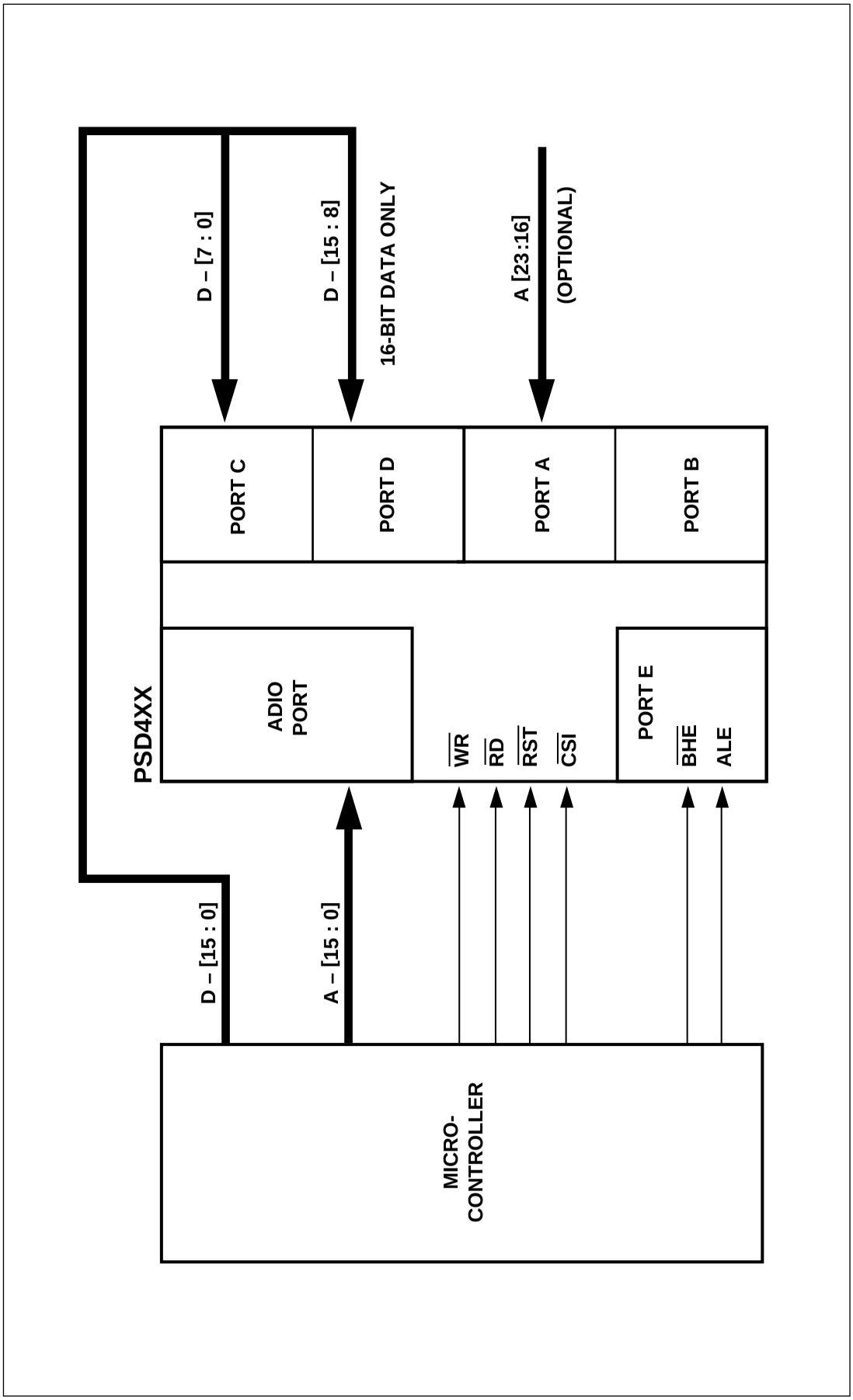
The PSD4XX Architecture (cont.)

Figure 21. ADIO Port, 16-Bit Multiplexed Bus Interface



The PSD4XX Architecture
(cont.)

Figure 22. Non-Multiplexed, 8 or 16-Bit Data



The PSD4XX Architecture (cont.)

9.2.4 Data Byte Enable

Microcontrollers have different data byte orientations with regard to the data bus. The following tables show how the PSD4XX handles the byte enable under different bus configurations. Even byte refers to locations with address A0 equal to “0”, and odd byte as locations with A0 equal to “1”.

Table 7. 8-Bit Data Bus

$\overline{BHE}$	A0	D7 – D0
X	0	Even Byte
X	1	Odd Byte

Table 8. 16-Bit Data Bus With $\overline{BHE}$

$\overline{BHE}$	A0	D15 – D8	D7 – D0
0	0	Odd byte	Even byte
0	1	Odd byte	–
1	0	–	Even byte

Table 9. 16-Bit Data Bus With $\overline{WRH}$ and $\overline{WRL}$

$\overline{WRH}$	$\overline{WRL}$	D15 – D8	D7 – D0
0	0	Odd byte	Even byte
0	1	Odd byte	–
1	0	–	Even byte

Table 10. 16-Bit Data Bus With SIZ0, A0

SIZ0	A0	D15 – D8	D7 – D0
0	0	Even byte	Odd byte
1	0	Even byte	–
1	1	–	Odd byte

Table 11. 16-Bit Data Bus With $\overline{UDS}$, $\overline{LDS}$

$\overline{LDS}$	$\overline{UDS}$	D15 – D8	D7 – D0
0	0	Even byte	Odd byte
1	0	Even byte	–
0	1	–	Odd byte

The PSD4XX Architecture (cont.)

9.2.5 Optional Features

The PSD4XX provides two optional features to add flexibility to the Bus Interface:

1. *Address In*

   Port A can be configured as high order address (A16-A23) inputs to the ZPLD for EPROM or other decoding. Inputs are latched by ALE/AS if Multiplexed Bus is selected. Other Ports can be configured as address input ports for the ZPLD. These inputs should not be used for EPROM decoding and are not latched internally.

2. *Address Out*

   For multiplexed bus only. Latched address lines A0-A15 are available on Port A, B, C or D.

Details on the optional features are described in the I/O Port section.

9.2.6 Bus Interface Examples

The next four figures show the PSD4XX interfacing with some popular microcontrollers. The examples show only the basic bus connections; some of the pin names on the PSD4XX parts change to reflect the actual pin functions.

Figure 23 shows the interface to the 80C31. The 80C31 has a 16 bit address bus and an 8-bit data bus. The lower address byte is multiplexed with the data bus. The $\overline{RD}$ and $\overline{WR}$ signals are used for accessing the data memory (SRAM) and the $\overline{PSEN}$ signal is for reading program memory (EPROM). The ALE signal is active high and is used to latch the address internally. Port C provides latched address outputs A[7:0]. Ports A, B, D, and E (PE2-PE7) can be configured to perform other functions. The RSTOUT reset to the 80C31 is generated by the ZPLD from the $\overline{RESET}$ input. This configuration eliminates any reset race condition between the 80C31 and the PSD4XX.

Figure 24 shows the 68HC11 interface, which is similar to the 80C31 except the PSD4XX generates internal $\overline{RD}$ and $\overline{WR}$ from the 68HC11's E and R/$\overline{W}$ signals.

In Figure 25, the Intel 80C196 microcontroller is interfaced to the PSD4XX. The 80C196 has a multiplexed 16-bit address and data bus. The $\overline{BHE}$ signal is used for data byte selection. Ports C and D are used as output ports for latched address A[15:0]. Pins PE6 and PE7 can be programmed as ZPLD outputs to provide the READY and BUSWIDTH control signals to the 80C196.

Figure 26 shows Motorola's MC68331 interfacing to the PSD4XX. The MC68331 has a 16-bit data bus and a 24-bit address bus. D15 – D8 from the MC68331 are connected to Port D, and D7 – D0 are connected to Port C.

Figure 23. Interfacing PSD4XX With 80C31

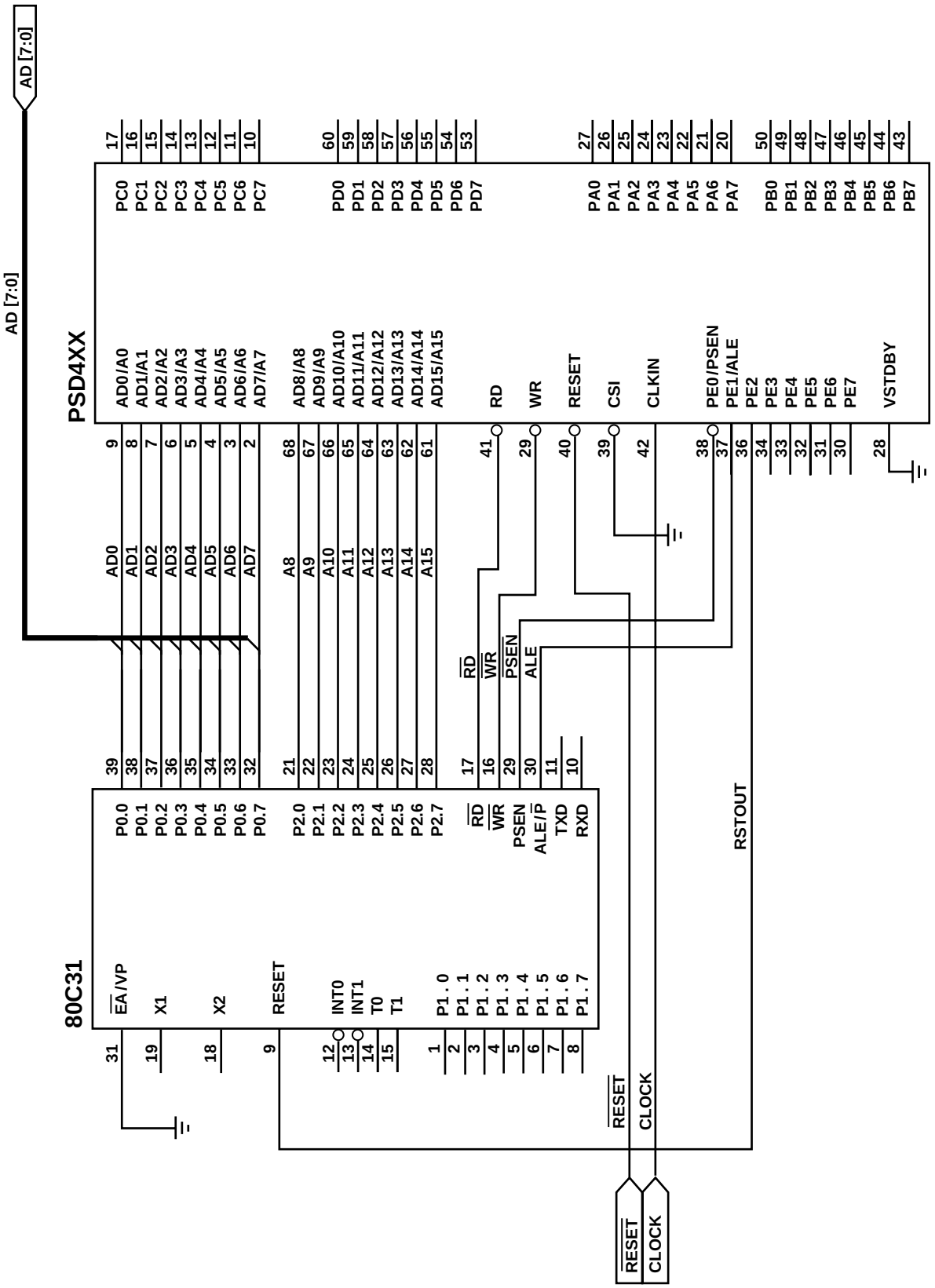


Figure 24. Interfacing PSD4XX With 68HC11

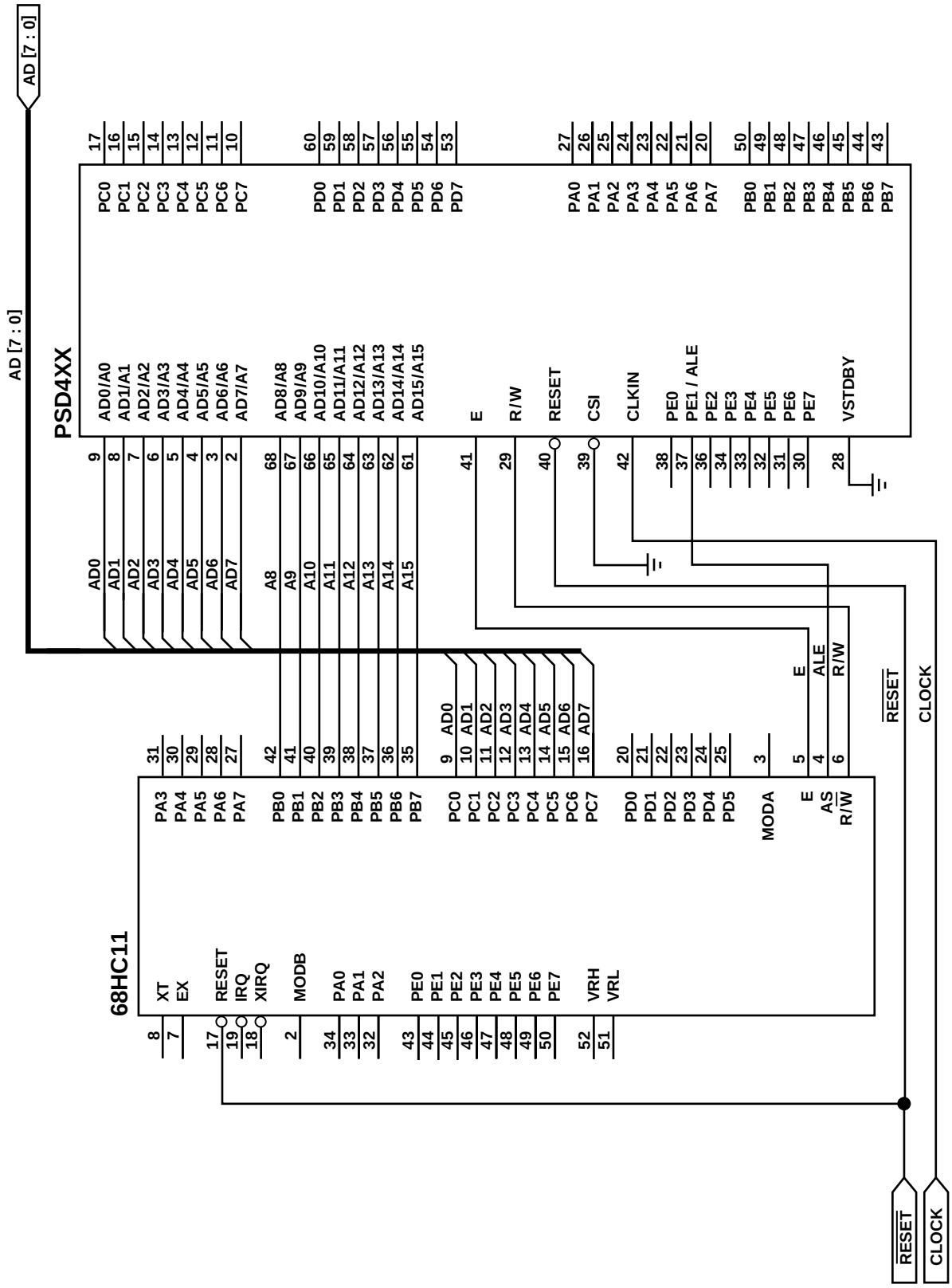


Figure 25. Interfacing PSD4XX With 80C196

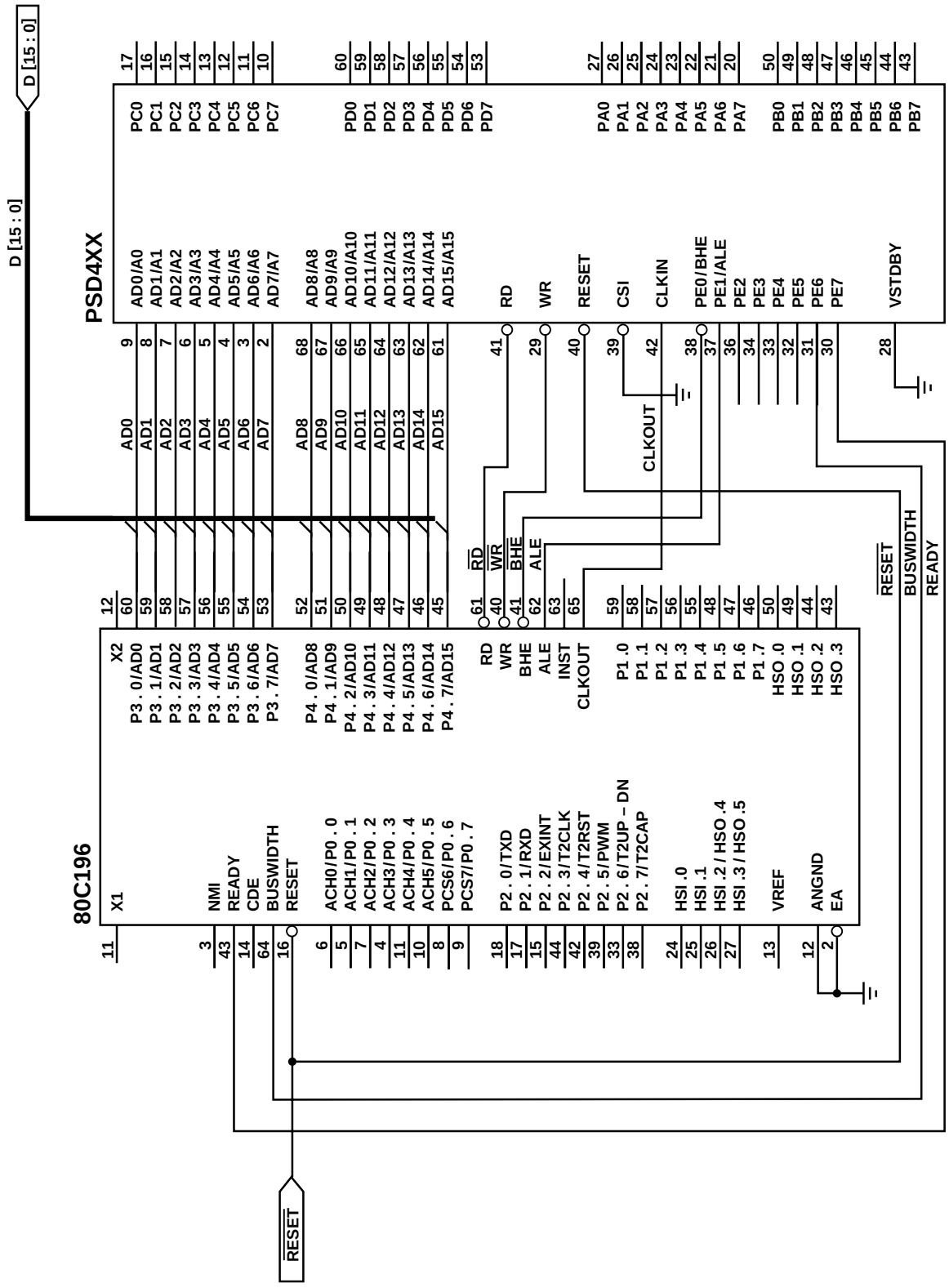
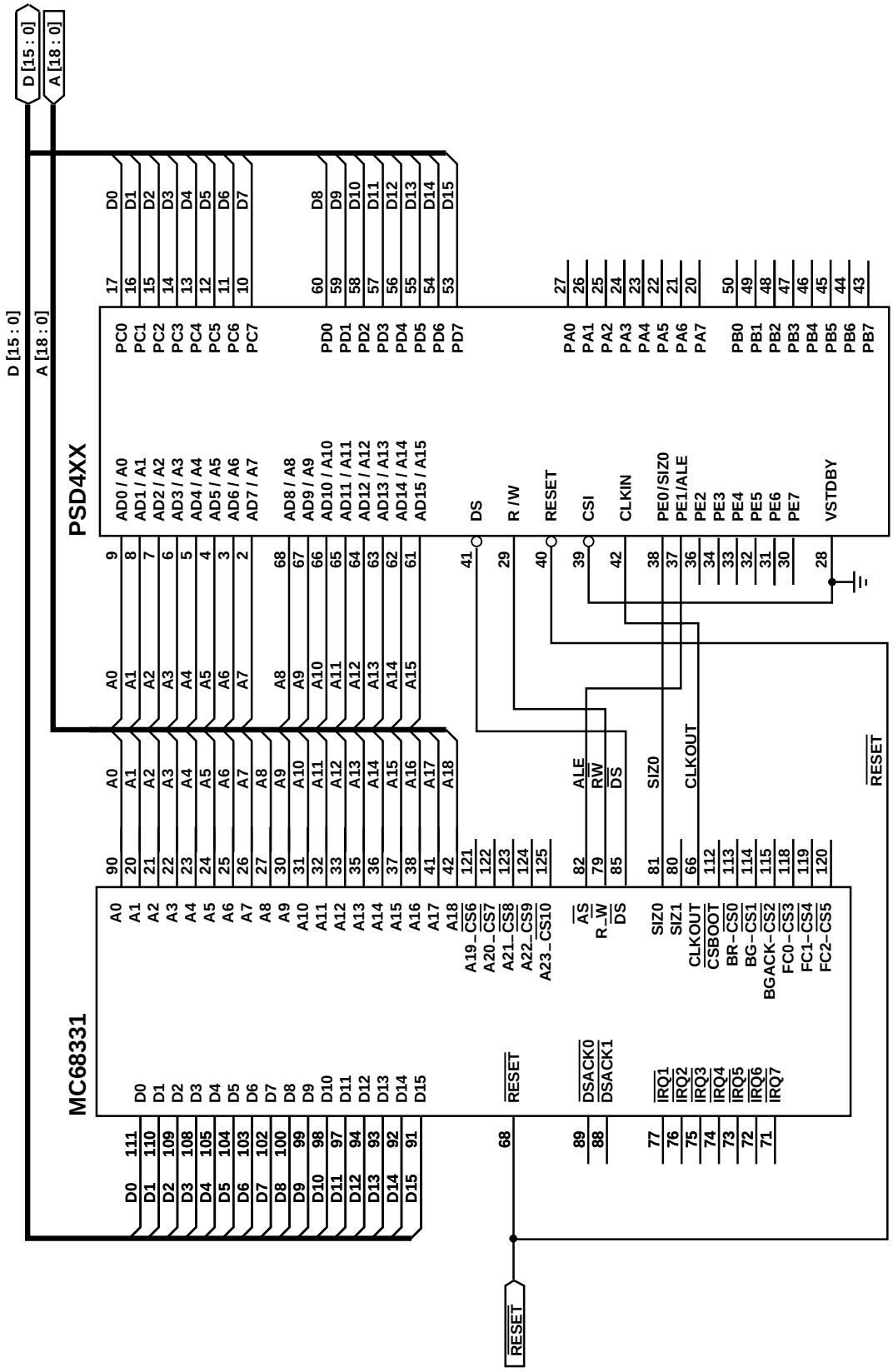


Figure 26. Interfacing PSD4XX With Motorola 68331



The PSD4XX Architecture (cont.)

9.3 I/O Ports

There are 5 programmable 8-bit I/O ports: Port A, Port B, Port C, Port D and Port E. These ports all have multiple operating modes, depending on the configuration. Some of the basic functions are providing input/output for the ZPLD, or can be used for standard I/O. Each port pin is individually configurable, thus enabling a single 8-bit port to perform multiple functions. The I/O ports occupy 256 bytes of memory space as defined by “CSIOP”. Refer to the System Configuration section for I/O register address offset.

To set up the port configuration the user is required to:

1. Define I/O Port Chip Select (CSIOP) in the ABEL file.
2. Initialize certain port configuration registers in the user’s program and/or
3. Specify the configuration in the PSD4XX PSDsoft Software.
4. Unused input pins should be tied to V_{CC} or GND.

The following is a description of the operating modes of the I/O ports. The functions of the port registers are described in later sections.

9.3.1 Standard MCU I/O

The Standard MCU I/O Mode provides additional I/O capability to the microcontroller. In this mode, the ports can perform standard I/O functions such as sensing or controlling various external I/O devices. Operation options of this mode are as follows:

❑ *Configuration*

1. Declare pins or signals which are used as I/O in the ABEL file.
2. Set the bit or bits in the Control Register to "1".
3. *As Output Port*
   – Write output data to Data Out Register
   – Set Direction Register to output mode
4. *As Input Port*
   – Set Direction Register to input mode
   – Read input from Data In Register

The port remains an output or input port as long as the Direction Register is not changed.

9.3.2 PLD I/O

The PLD I/O mode enables the port to be configured as an input to the ZPLD, or as an output from the GPLD macrocell. The output can be tri-stated with a control signal defined by a product term from the ZPLD. This mode is configured by the user in the PSD4XX PSDsoft Software, and is enabled upon power up. For a detailed description, see the section on the ZPLD.

❑ *Configuration*

1. Declare pins or signals in the ABEL file (PSDsoft).
2. Write logic equations in the ABEL file.
3. PSD Compiler maps the PLD functions to the PSD.

The PSD4XX Architecture (cont.)

9.3.3 Address Out

For microcontrollers with a multiplexed address/data bus, the I/O ports in Address-Out mode are able to provide latched address outputs (A0 – A15) to external devices. This mode of operation requires the user to:

❑ *Configuration*

1. Declare the pins used as address line outputs in the ABEL file (PSDsoft).
2. Write “0” to the corresponding bit in the Control Register associated with each I/O port.
3. Set the Direction Register to Output Mode.

9.3.4 Address In

There are two Address In modes:

1. For Port A - as other address line (A2-A7 and A16-A23) inputs to the DPLD. Additional address inputs included in the EPROM decoding must come from Port A. The address inputs are latched internally by ALE/AS if Multiplexed Bus is specified in PSDsoft.
2. For Ports C and D – as address inputs to the ZPLD for general decoding, should not be used in EPROM decoding.

❑ *Configuration*

1. Declare pins or signals used as Address In in the ABEL file (PSDsoft).
2. Write latch equations in the .ABL file, e.g., A16.LE = ALE.
3. Include latched address in logic equations.

9.3.5 Data Port

In this mode, the port is acting as a data bus port for a microcontroller which has a non-multiplexed address/data bus. The Data Port is connected to the data bus of the microcontroller and the ADIO port is connected to the address bus.

❑ *Configuration*

Select the non-multiplexed bus option in PSD configuration (PSDsoft).

9.3.6 Alternate Function In

This mode is per-pin configurable and enables the user to define pin PE7 of Port E as Automatic Power Down (APD) CLK input.

❑ *Configuration*

1. Select input functions in PSD configuration.
2. PSD Compiler assigns pins for the selected options.

The PSD4XX Architecture (cont.)

9.3.7 Peripheral I/O

This mode enables the microcontroller to read or write to a peripheral though Port A. When there is no read/write operation, Port A is tri-stated. One of the applications of Peripheral I/O is in a DMA based design.

❑ *Configuration*

1. Declare the pins used as pheripheral I/O in the ABEL file.
2. Write logic equations for PSEL0 and PSEL1.
3. Write a “1” to the PIO bit in the VM Register to activate the Peripheral I/O operation. See the section on Peripheral I/O for a detailed description.

9.3.8 Open Drain Outputs

This mode enables the user to configure Ports C and D pins as open drain outputs. CMOS output is the default configuration. Writing “1” to the corresponding bit in the Open Drain Register changes the pin to open drain output.

Table 12. Operating Modes of the I/O Ports

Table 12 summarizes the operating modes of the I/O ports. Not all the functions are available to every port.

Port Mode	Port A	Port B	Port C	Port D	Port E
Standard MCU I/O	Yes	Yes	Yes	Yes	Yes
PLD I/O	Yes	Yes	Input Only*	Input Only*	Yes*
Address Out	Yes	Yes	Yes	Yes	Yes
Address In	Yes	Yes**	Yes**	Yes**	
Data Port			Yes	Yes	
Alternate Function In					Yes
Peripheral I/O	Yes				
Open Drain			Yes	Yes	

* PSD4XXA2 and ZPSD4XXA2 Only.

** For external decoding. Cannot be latched by ALE

The PSD4XX Architecture (cont.)

9.3.9 Port Registers

There are two sets of registers per I/O port: the Port Configuration Registers (PCR) which consist of four 8-bit registers; and the Port Data Registers (PDR) which include three 8-bit registers. The PCR is used for setting up the port configuration, while the PDR enables the microcontroller to write or read port data or status bits. Tables 13 and 14 show the names and the registers and the ports to which they belong.

All the registers in the PCR and PDR are 8-bits wide and each bit is associated with a pin in the I/O port. In Table 15, the LSB of the Data In Register of Port A is connected to pin PA0, and the MSB is connected to PA7. This pin configuration also applies to other registers and ports. For example, in the Direction Register of Port A, writing a hex value of 07 to the register configures pins PA0 – PA2 as output pins, while PA3 – PA7 remain as input pins.

Registers can be accessed by the microcontroller during normal read/write bus cycles. The I/O address offset of the registers are listed in the System Configuration section.

Table 13. Port Configuration Registers (PCR)

Register Name	Port	Write/Read
Control Register	A,B,C,D,E	Write/Read
Direction Register	A,B,C,D,E	Write/Read
Open Drain Register	C,D	Write/Read
PLD – I/O Register	A,B,E	Read

Table 14. Port Data Registers (PDR)

Register Name	Port	Read/Write
Data In Register	A,B,C,D,E	Read
Data Out Register	A,B,C,D,E	Write/Read
Macrocell Out Register	A,B,E	Read

Table 15.
Data In Register – Port A

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7 Pin	PA6 Pin	PA5 Pin	PA4 Pin	PA3 Pin	PA2 Pin	PA1 Pin	PA0 Pin

Direction Register – Port A
(Example: Pins PA0 – PA2 as Output, PA3 – PA7 as Input)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7 Pin	PA6 Pin	PA5 Pin	PA4 Pin	PA3 Pin	PA2 Pin	PA1 Pin	PA0 Pin
= 0	= 0	= 0	= 0	= 0	= 1	= 1	= 1

The PSD4XX Architecture (cont.)

9.3.9.1 Control Register

This register is used in both Standard MCU I/O Mode and Address Out modes. For setting a Standard MCU I/O Mode, a “1” must be written to the corresponding bit in the register. Writing a “0” to the register is required for the Address Out mode. The register has a default value of “0” after reset.

9.3.9.2 Direction Register

This register is used to control the direction of data flow in the I/O Ports. Writing a “1” to the corresponding bit in the register configures the port to be an output port, and a “0” forces the port to be an input port. The I/O configuration of the port pins can be determined by reading the Direction Register. After reset, the pins are in input mode.

9.3.9.3 Open Drain

This register determines whether the output pin driver of Ports C or D is a CMOS driver or an Open Drain driver. Writing a “0” to the register selects a CMOS driver, while a “1” selects an Open Drain driver.

9.3.9.4 PLD – I/O Register

This is a read only status register. Reading a "1" indicates the corresponding pin is configured as a PLD pin. A "0" indicates the pin is an I/O pin.

9.3.9.5 Data In Register

This register is used in the Standard MCU I/O Mode configuration to read the input pins.

9.3.9.6 Data Out Register

This register holds the output data in the Standard MCU I/O Mode. The contents of the register can also be read.

9.3.9.7 Macrocell Out Register

This register enables the user to read the outputs of the GPLD macrocell (PA, PB, and PE macrocells).

9.3.9.8 I/O Register Address Offset

The I/O Register can be accessed by the microcontroller during normal read/write bus cycles. The address of a register is defined as:

CSIOP + register address offset

The CSIOP is the base address that is defined in the ABEL file and occupies a 256 byte space. The register address offset lies within this 256 byte space. Tables 16 and 16a are the address offset of the registers.

The PSD4XX Architecture (cont.)

Table 16. Register Address Offset

Register Name	Address Offset				
	Port A	Port B	Port C	Port D	Port E
Data In	00	01	10	11	20
Control	02	03	12	13	22
Data Out	04	05	14	15	24
Direction	06	07	16	17	26
Open Drain			18	19	
PLD – I/O	0A	0B			2A
Macrocell Out	0C	0D			2C (PSD4XXA2/ ZPSD4XXA2)

Table 16a. Register Address Offset

(For 16-bit Motorola Microcontrollers in 16-bit mode. Use Table 16 if 8-bit mode is selected.)

Register Name	Address Offset				
	Port A	Port B	Port C	Port D	Port E
Data In	01	00	11	10	21
Control	03	02	13	12	23
Data Out	05	04	15	14	25
Direction	07	06	17	16	27
Open Drain			19	18	
PLD – I/O	0B	0A			2B
Macrocell Out	0D	0C			2D (PSD4XXA2/ ZPSD4XXA2)

The PSD4XX Architecture (cont.)

9.3.10 Port A – Functionality and Structure

Port A is the most flexible of all the I/O ports. It can be configured to perform one or more of the following functions:

- ❑ Standard MCU I/O Mode
- ❑ PLD I/O
- ❑ Address Out – latched address lines A[0-7] are assigned to pins PA[0-7].
- ❑ Address In – input port for other address lines, inputs can be latched by ALE.
- ❑ Peripheral I/O

Figure 27 shows the structure of a Port A pin. If the pin is configured as an output port, the multiplexer selects one of its three inputs as output. If the pin is configured as an input, the input connects to :

1. Data In Register as input in Standard MCU I/O Mode

or

2. PA Macrocell as PLD input

or

3. PA Macrocell through a latch latched by ALE, as Address In input.

9.3.11 Port B – Functionality and Structure

Port B is similar to Port A in structure. It can be configured to perform one or more of the following functions:

- ❑ Standard MCU I/O Mode
- ❑ PLD I/O
- ❑ Address Out – address lines A[0-7] for 8-bit multiplexed bus or address lines A[8-15] for 16-bit multiplexed bus are assigned to pins PB[0-7].

Figure 28 shows the structure of a Port B pin. If the pin is configured as an output port, the multiplexer selects one of its three inputs as output. If the pin is configured as input, the input connects to :

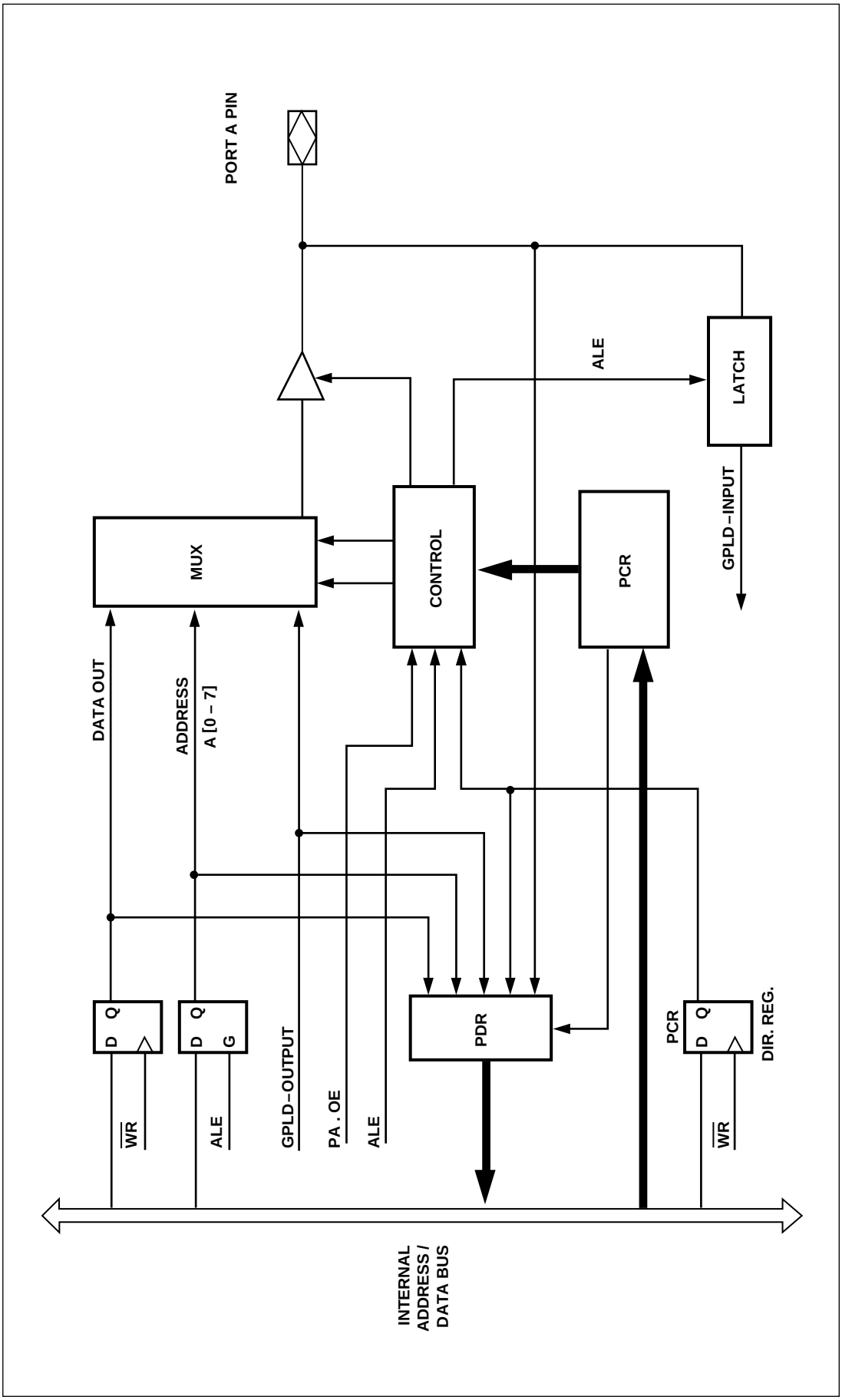
- ❑ Data In Register as input in Standard MCU I/O Mode

or

- ❑ PB Macrocell as PLD input

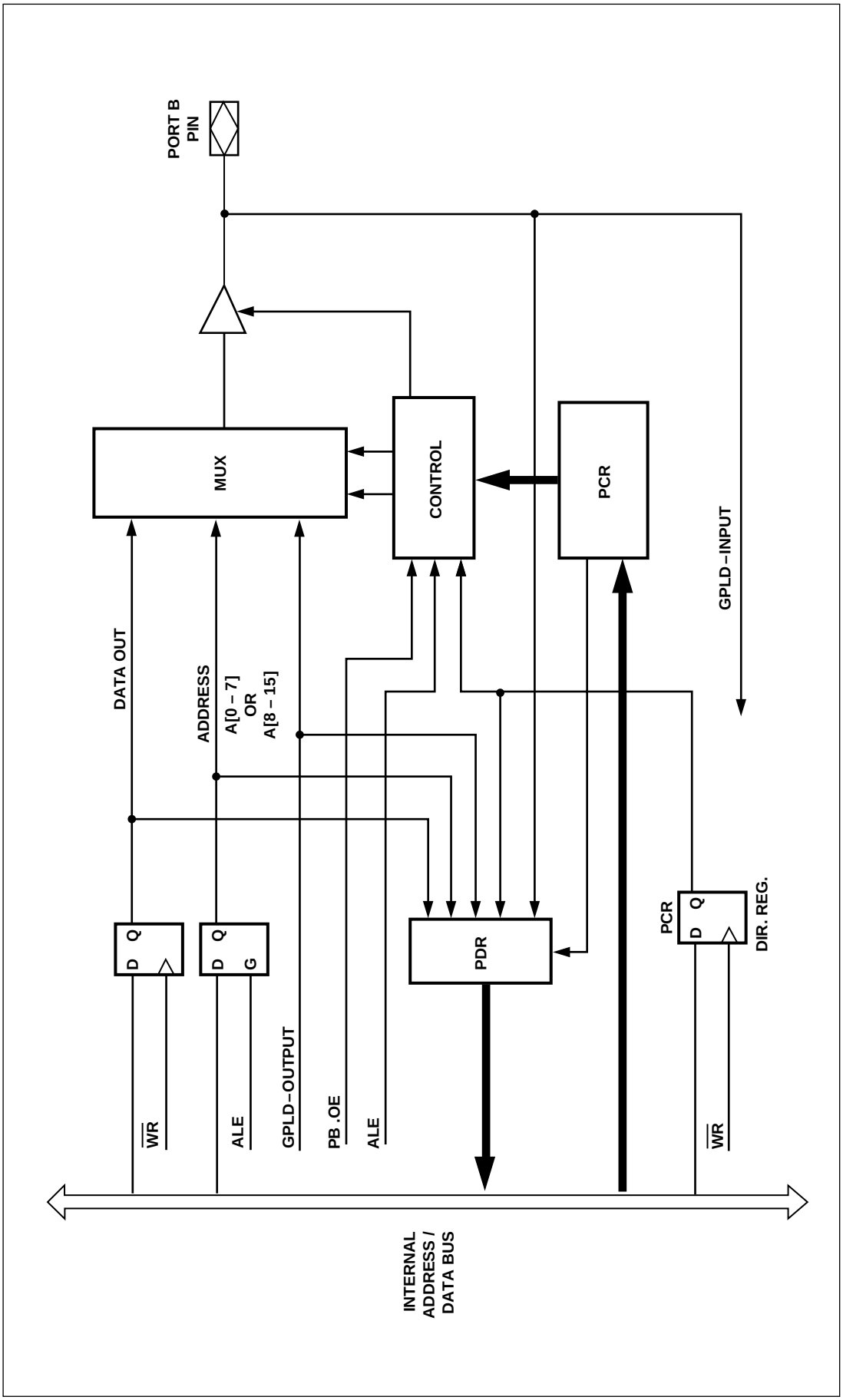
The PSD4XX Architecture (cont.)

Figure 27. Port A Pin Structure



The PSD4XX Architecture (cont.)

Figure 28. Port B Pin Structure



The PSD4XX Architecture (cont.)

9.3.12 Port C and Port D – Functionality and Structure

Ports C and D are identical in function and structure and each can be configured to perform one or more of the following operating modes:

- ❑ Standard MCU I/O Mode
- ❑ PLD Input – direct input to ZPLD (PSD4XXA2 and ZPSD4XXA2 Only)
- ❑ Address Out – latched address outputs
  - Port C: A[0-7] are assigned to pins PC[0-7]
  - Port D: A[0-7] for 8-bit multiplexed bus or A[8-15] for 16-bit multiplexed bus are assigned to pins PD0-7]
- ❑ Data Port
  - Port C: D[0-7] for 8-bit non-multiplexed bus
  - Port D: D[8-15] for 16-bit non-multiplexed bus
- ❑ Open Drain – select CMOS or Open Drain driver

Figures 29 and 30 show the structure of a Port C or D pin. If the pin is configured as output port, the multiplexer selects one of the two inputs as output. If the pin is configured as input, the input connects to :

- ❑ Data In Register as input in the Standard MCU I/O Mode

or

- ❑ ZPLD input (PSD4XXA2 and ZPSD4XXA2 Only)

9.3.13 Port E – Functionality and Structure

Port E can be configured to perform one or more of the following functions:

- ❑ Standard MCU I/O Mode
- ❑ PLD I/O (PSD4XXA2 and ZPSD4XXA2 Only)
- ❑ Address Out – latched address lines A[0-7] are assigned to pins PE[0-7]
- ❑ Alternate Function In – in this mode, the inputs to Port E pins are:
  - **PE0**
    $\overline{BHE}$ or $\overline{PSEN}$ or $\overline{WRH}$ or $\overline{UDS}$ or SIZ0
  - **PE1** – ALE
  - **PE7**
    APD CLK :clock input for Automatic Power Down Counter

Figure 31 shows the structure of a Port E pin. The Control Logic block selects one of four sources through the multiplexer for pin output. If the pin is configured as input, the input goes to:

- ❑ Data In Register as input in Standard MCU I/O Mode

or

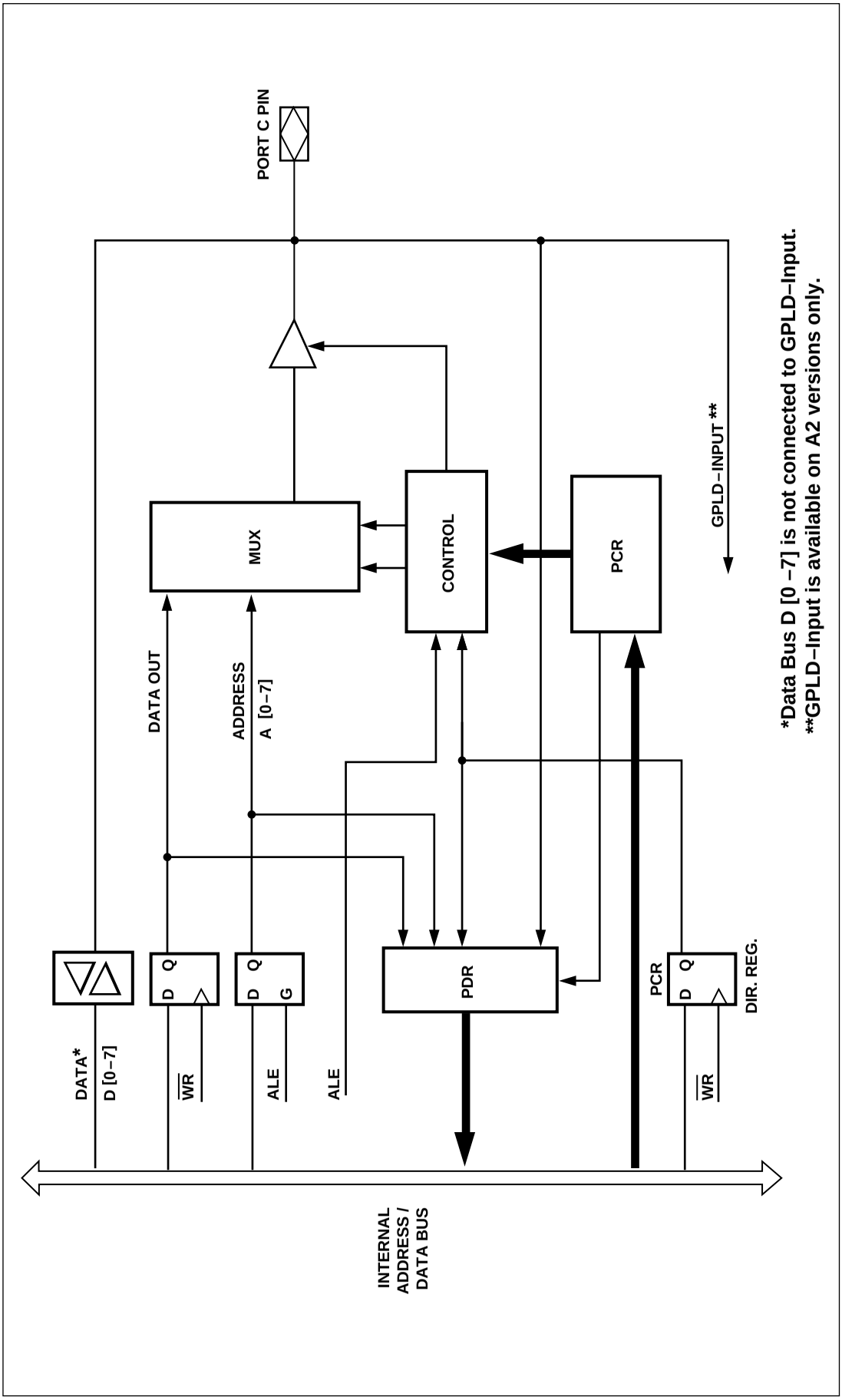
- ❑ PE Macrocell as PLD input (PSD4XXA2 and ZPSD4XXA2 Only)

or

- ❑ Alternate Function In

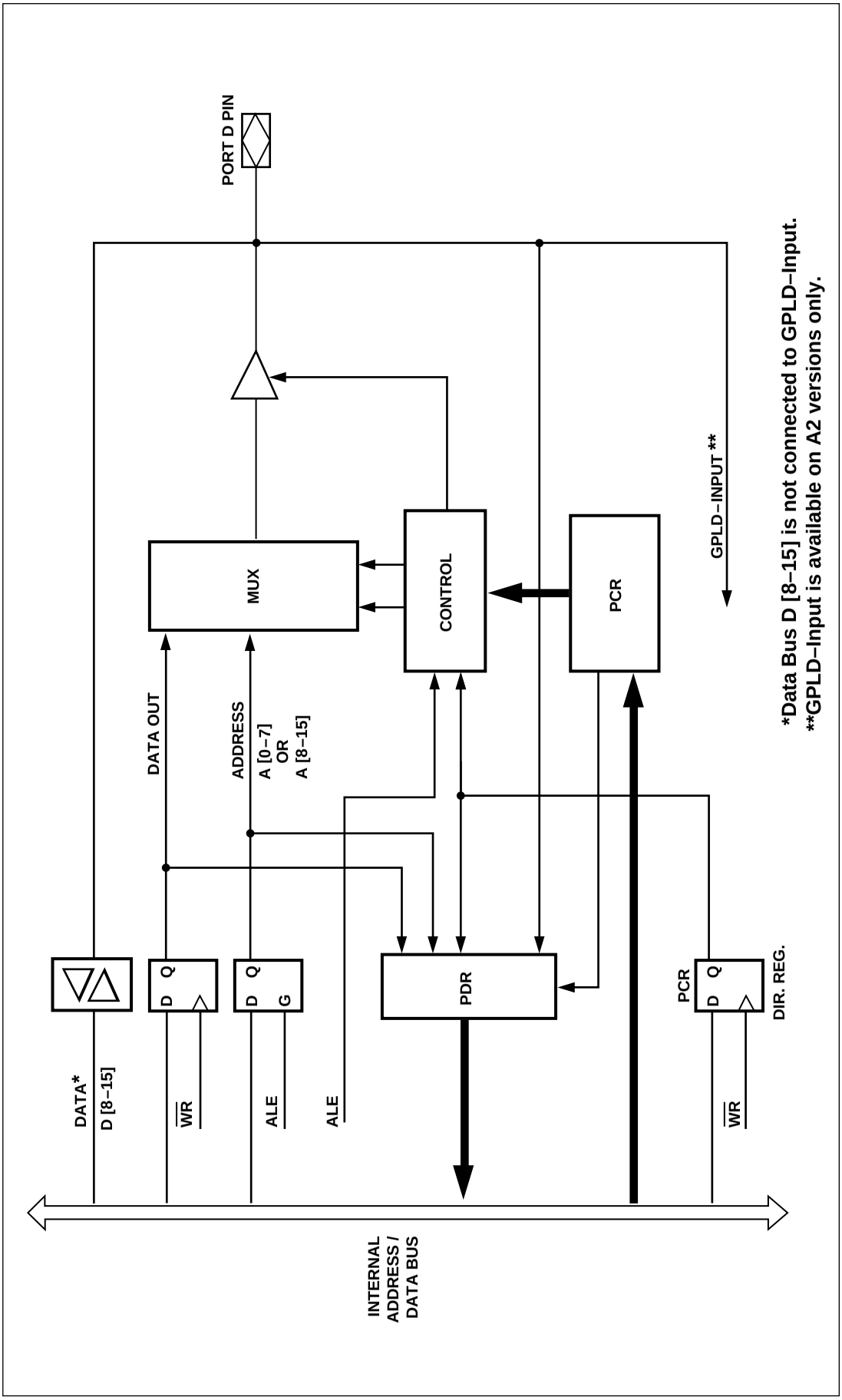
The PSD4XX Architecture (cont.)

Figure 29. Port C Pin Structure



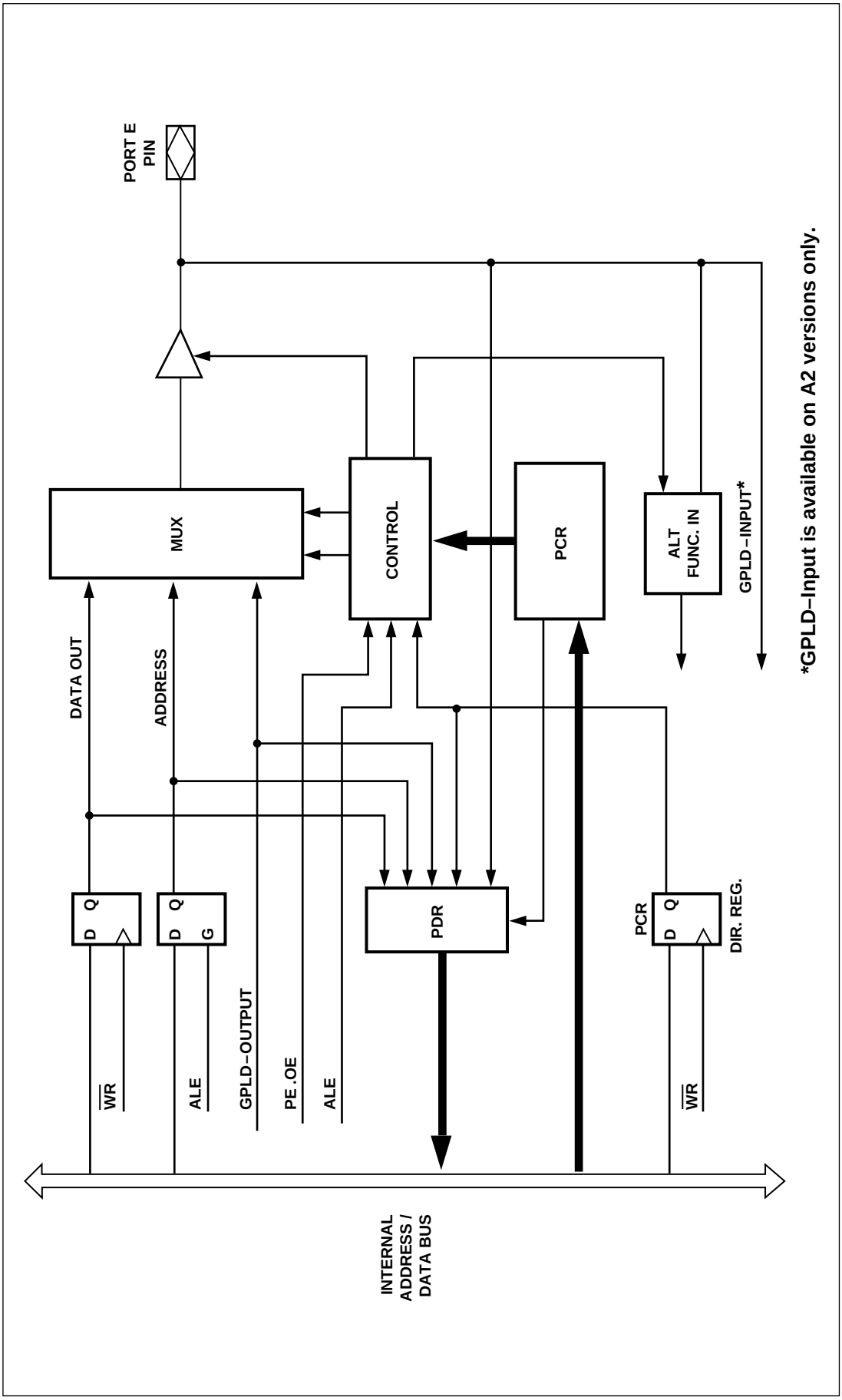
The PSD4XX Architecture (cont.)

Figure 30. Port D Pin Structure



The PSD4XX Architecture (cont.)

Figure 31. Port E Pin Structure



The PSD4XX Architecture (cont.)

9.4 Memory Block

The PSD4XX provides EPROM memory for code storage and SRAM memory for scratch pad usage. Chip selects for the memory blocks come from the DPLD decoding logic and are defined by the user in the PSDsoft Software. Figure 32 shows the organization of the Memory Block.

The PSD4XX family uses Zero-power memory techniques that place memory into Standby Mode between MCU accesses. The memory becomes active briefly after an address transition, then delivers new data to the outputs, latches the outputs, and returns to standby. This is done automatically and the designer has to do nothing special to benefit from this feature. Both the EPROM and SRAM have this feature.

9.4.1 EPROM

The PSD4XX provides three EPROM densities: 256Kbit, 512Kbit, or 1Mbit. The EPROM is divided into four 8K, 16K or 32K byte blocks. Each block has its own chip select signals (ES0 – ES3). The EPROM can be configured as 32K x 8, 64K x 8 or 128K x 8 for microcontrollers with an 8-bit data bus. For 16-bit data buses, the EPROM is configured as 16K x 16, 32K x 16 or 64K x 16.

9.4.2 SRAM

The SRAM has 16Kbits of memory, organized as 2K x 8 or 1K x 16. The SRAM is enabled by chip select signal RS0 from the DPLD. The SRAM has a battery back-up (STBY) mode. This back-up mode is invoked when the V_{CC} voltage drops under the Vstdby voltage by approximately 0.7 V. The Vstdby voltage is connected only to the SRAM and cannot be lower than 2.7 volts.

9.4.3 Memory Select Map

The EPROM and SRAM chip select equations are defined in the ABEL file in terms of address and other DPLD inputs. The memory space for the EPROM chip select (ES0 – ES3) should not be larger than the EPROM block (8KB, 16KB, or 32KB) it is selecting.

The following rules govern how the internal PSD4XX memory selects/space are defined:

- ❏ The EPROM blocks address space cannot overlap
- ❏ SRAM, internal I/O and Peripheral I/O space cannot overlap
- ❏ SRAM, internal I/O and Peripheral I/O space can overlap EPROM space, with priority given to SRAM or I/O. The portion of EPROM which is overlapped cannot be accessed.

The Peripheral I/O space refers to memory space occupied by peripherals when Port A is configured in the Peripheral I/O Mode.

The PSD4XX Architecture (cont.)

9.4.4 Memory Select Map For 8031 Application

The 8031 family of microcontrollers has separate code memory space and data memory space. This feature requires a different Memory Select Map. Two modes of operation are provided for 8031 applications. The selection of the modes is specified in the PSD4XX PSDsoft Software (PSDconfiguration):

- ***Separate Space Mode***
  In this mode, the PSEN signal is used to access code from EPROM, and the RD signal is used to access data from SRAM. The code memory space is separated from the data memory space.
- ***Combined Space Mode***
  In this mode, the EPROM can be accessed by PSEN or RD. The EPROM is used for code and data storage. The memory block's address space cannot overlap.

If data and code memory blocks must overlap each other, the $\overline{RD}$ signal can be included as an additional address input in generating the EPROM chip select signals (ES0 – ES3). In this case the EPROM access time is from the $\overline{RD}$ valid to data valid. Figures 32a and 32b show the memory configuration in the two modes.

In some applications it is desirable to execute program codes in SRAM. The PSD4XX provides this option by enabling PSEN to access SRAM. To activate this option, the SRCODE bit of the VM Register must be set to “1” (see Table 17). SRAM space can overlap EPROM space and has priority when PSEN is used.

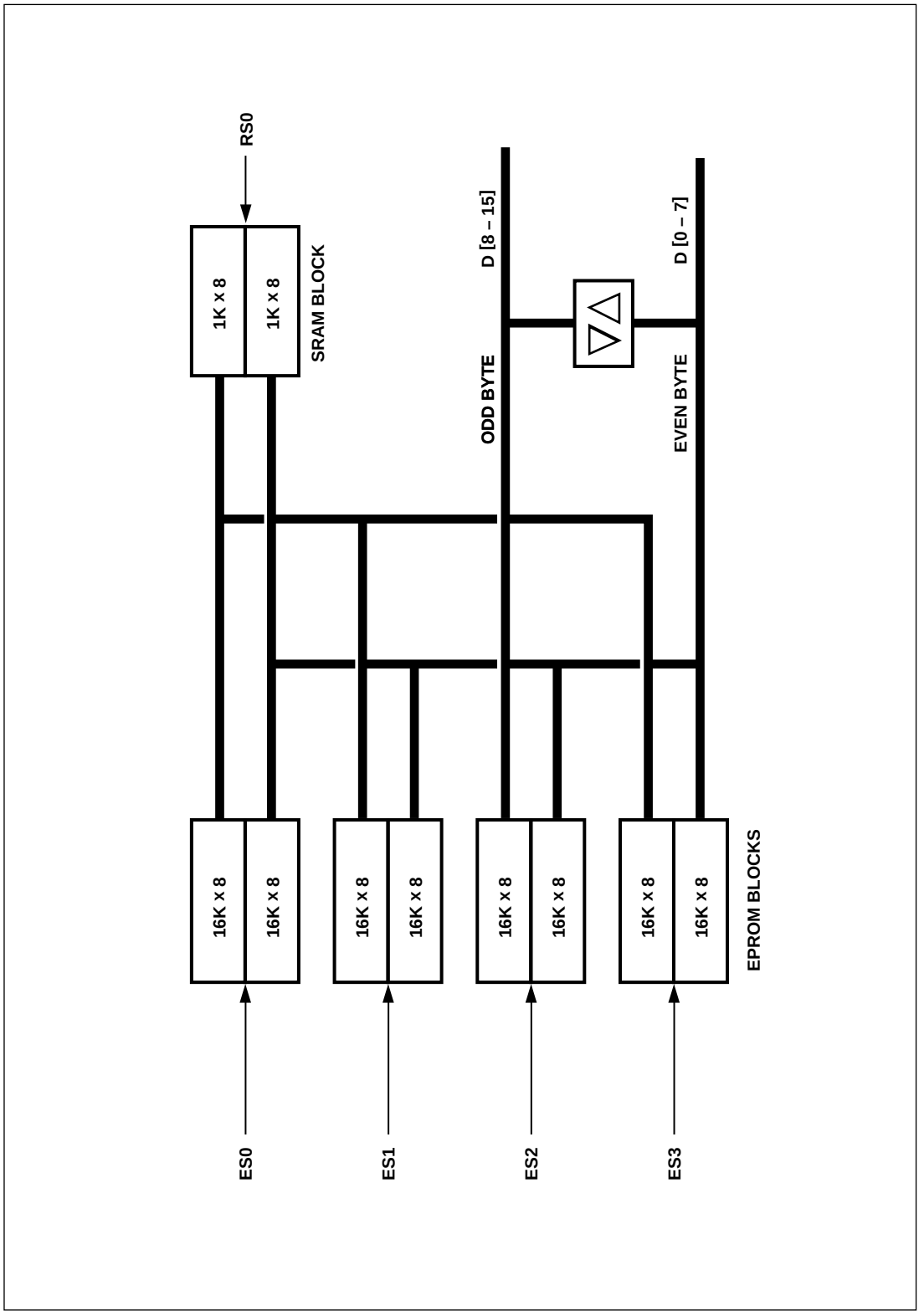
Table 17. VM Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	*	*	SRCODE	PIO
						1 = ON	1 = ON

* = Reserved for future use, bits set to zero.

The PSD4XX Architecture (cont.)

Figure 32. Memory Block Diagram (128KB EPROM)



The PSD4XX Architecture (cont.)

Figure 33a. 8031 Memory Modes

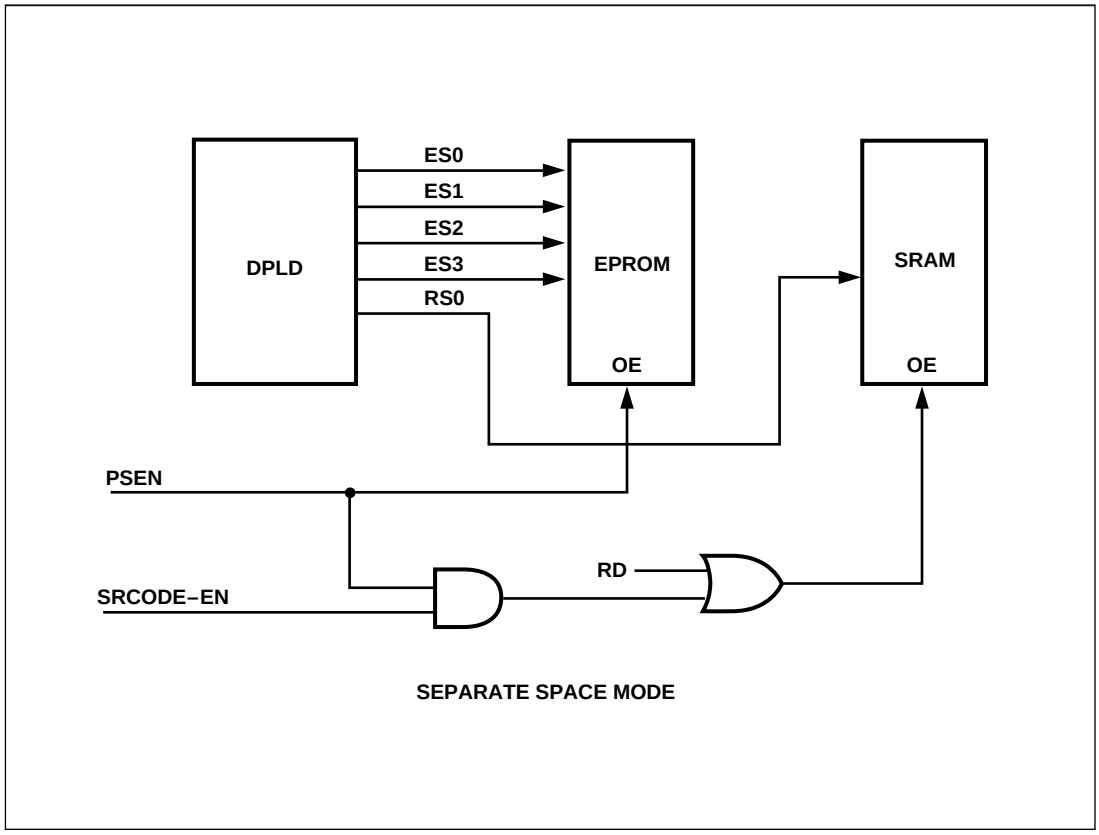
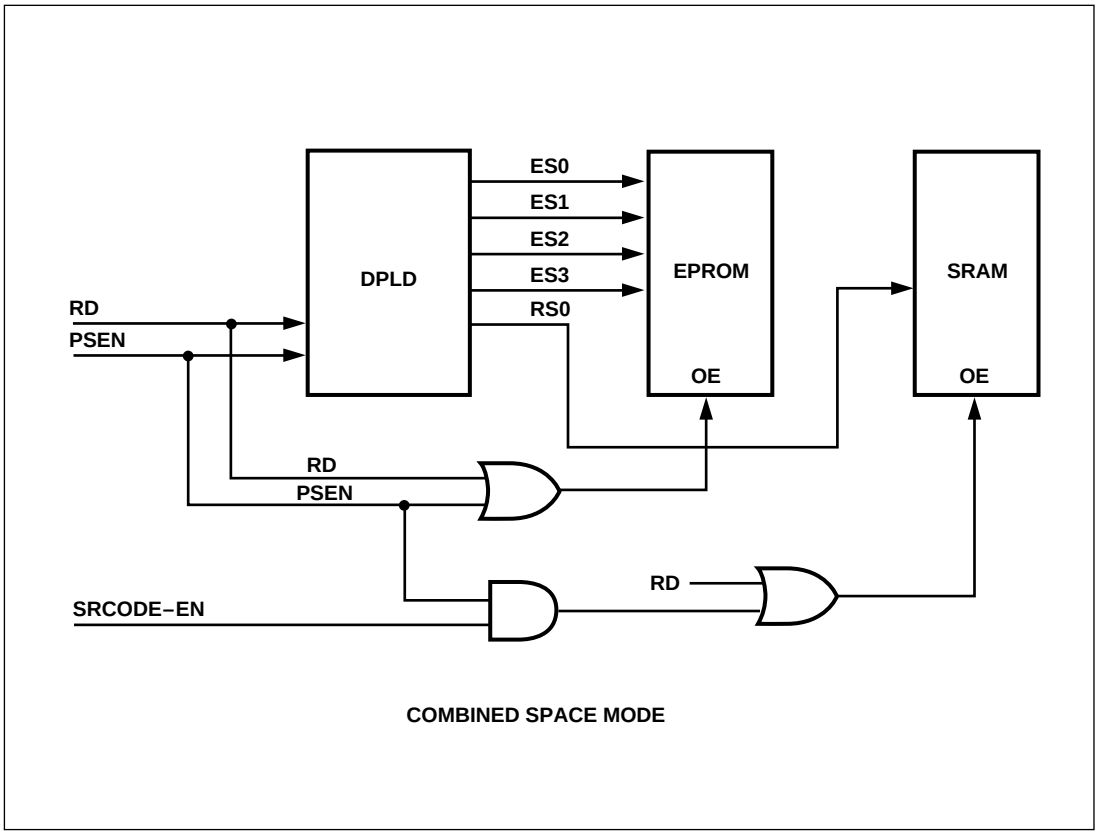


Figure 33b. 8031 Memory Modes



The PSD4XX Architecture (cont.)

9.4.5 Peripheral I/O

The Peripheral I/O Mode is one of the operating modes of Port A. In this mode, Port A is connected to the data bus of peripheral devices. Port A is enabled only when the microcontroller is accessing the devices, otherwise the Port is tri-stated. This feature enables the microcontroller to access external devices without requiring buffers and decoders. Figure 34 shows the structure of Port A in the Peripheral I/O Mode.

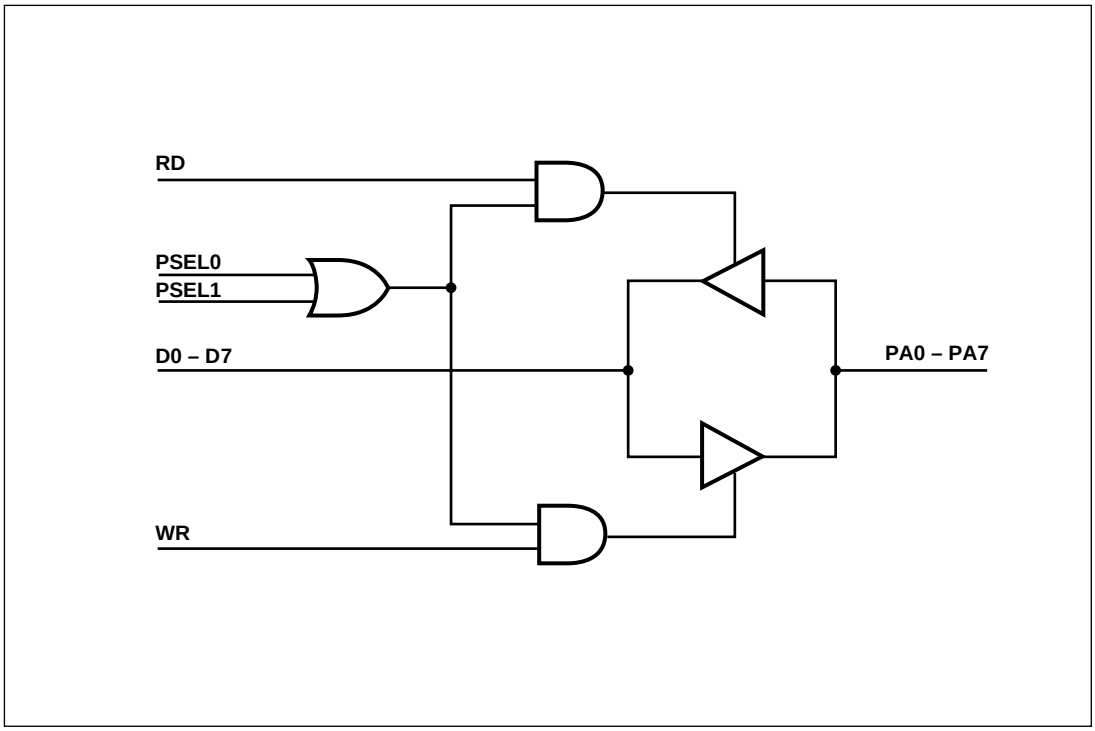
The memory address space occupied by the devices are defined by two signals: PSEL0 and PSEL1. The signals are direct outputs from the Decoding PLD (DPLD). Whenever any of the signals is active, the Port A driver is enabled, and the direction of the data flow is determined by the RD/WR signals.

The Peripheral I/O Mode and the peripheral select signals are configured and defined in the PSDsoft Software (see the section on I/O Port for configuration). The PIO bit in the VM Register (see Table 17) also needs to be set to “1” by the user to initialize the Peripheral I/O Mode.

The Peripheral I/O mode can be used, for example, in DMA applications where the microcontroller does not support DMA operations, such as tri-stating the address/data bus. Figure 35 shows a block diagram of a microcontroller and PSD4XX based design that makes use of this mode. In this application, the microcontroller has a multiplexed bus which is connected to the ADIO port. The C and D ports connect to the peripheral address bus and are both configured in Address Out Mode. Port A is configured in the Peripheral I/O mode and is connected to the peripheral data bus. Ports B and E are used to generate control signals.

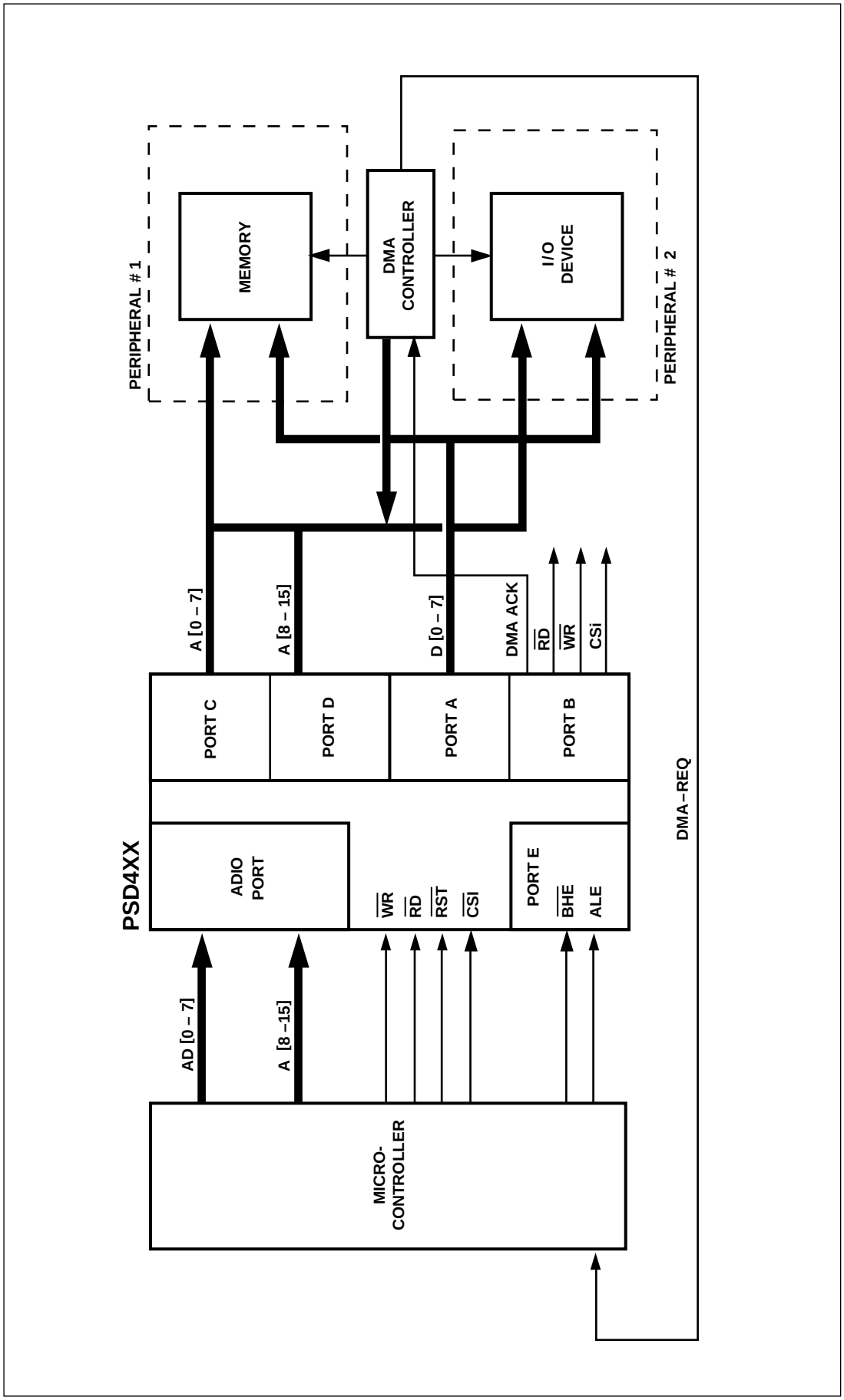
During normal activity, the microcontroller has access to any peripheral (memory or I/O device) through the PSD4XX device. When there is a DMA request, the microcontroller tri-states the address bus on Ports C and D by writing a “0” to the port Direction Registers. The DMA controller then takes over the data and address buses after receiving acknowledgement from the microcontroller.

Figure 34. Port A In Peripheral I/O Mode



The PSD4XX Architecture (cont.)

Figure 35. PSD4XX Peripheral I/O Configuration



The PSD4XX Architecture (cont.)

9.5 Power Management Unit

The PSD4XX provides many power saving options. By configuring the PMMRs (Power Management Mode Registers), the user can reduce power consumption. Table 18 shows the bit configuration of the PMMR0 and PMMR1. The microcontroller is able to control the power consumption by changing the PMMR bits at run time.

9.5.1 Standby Mode

There are two Standby Modes in the PSD4XX:

- *Power Down Mode*
- *Sleep Mode*

9.5.1.1 Power Down Mode

In this mode, the internal devices are shut down except for the I/O ports and the ZPLD. There are three ways the PSD4XX can enter into the Power Down Mode: by controlling the CSI input, by activating the Automatic Power Down (APD) Logic and the ZPLD, or when none of the inputs are changing and the Turbo bit is off.

- *The CSI*

  The CSI input pin is an active low signal. When low, the signal selects and enables the PSD4XX. The PSD4XX enters into Power Down Mode immediately when the signal turns high. This signal can be controlled by the microcontrollers, external logic or it can be grounded. The CSI input turns off the internal bus buffers in Standby Mode. The address and control signals from the microcontroller are blocked from entering the ZPLD as inputs.

- *The APD Logic*

  The APD unit enables the user to enter a power down mode independent of controlling the CSI input. This feature eliminates the need for external logic (decoders and latches) to power down the PSD. The APD unit concept is based on tracking the activity on the ALE pin. If the APD unit is enabled and ALE is not active, the 4-bit APD counter starts counting and will overflow after 15 clocks, generating a PD (Power Down) signal powering down the PSD. If sleep mode is enabled, then PD signal will also activate the sleep mode. Immediately after ALE starts pulsing the PSD will get out of the power down or sleep mode.

  The operation of APD is controlled by the PMMR (see Figure 36a). PMMR1 bit 0 selects the source of the APD counter clock. After reset the APD counter clock is connected to PE7 (APD CLK) on the PSD. In order to guarantee that the APD will not overflow there should be less than 15 APD clocks between two ALE pulses. If CLKIN frequency is adequate, then it can be connected to the APD and PE7 is used for other functions.

  The next step is to select the ALE power down polarity. Usually, MCUs entering power down will freeze their ALE at logic high or low. By programming bit 1 of PMMR0 the power down polarity can be defined for the APD. If the APD detects that the ALE is in the power down polarity for 15 APD counter clocks then the PSD will enter a power down mode. To enable the APD operation, bit 2 in the PMMR0 should be set high.

9.5.1.2 Sleep Mode

The Sleep Mode is activated if the SLEEP EN bit, the APD EN bit, and the ALE Polarity bit in the PMMR are set, and the APD Counter has overflowed after 15 clocks (see Figure 36). In Sleep Mode the PSD4XX consumes less power than the Power Down Mode.

In this mode, the ZPLD still monitors the inputs and responds to them. As soon as the ALE starts pulsing, the PSD4XX exits the Sleep Mode.

The PSD access time from Sleep Mode is specified by t_{LVDV1}. The ZPLD response time to an input transition is specified by t_{LVDV2}.

The PSD4XX Architecture (cont.)

Figure 36. Power Management Unit

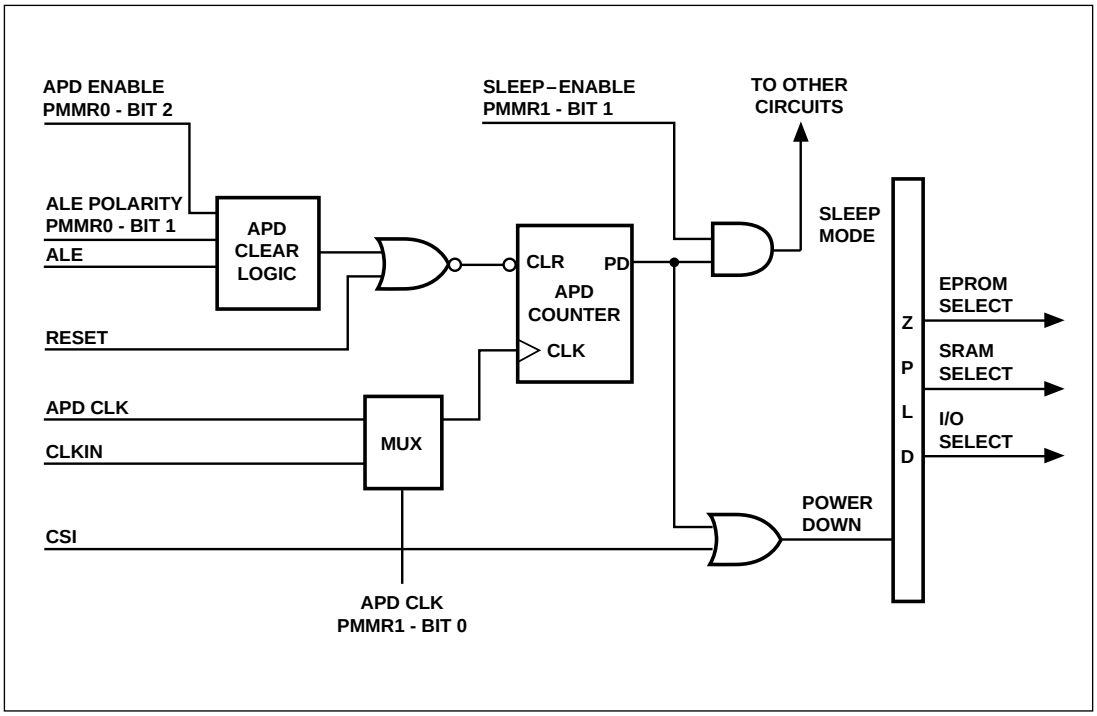
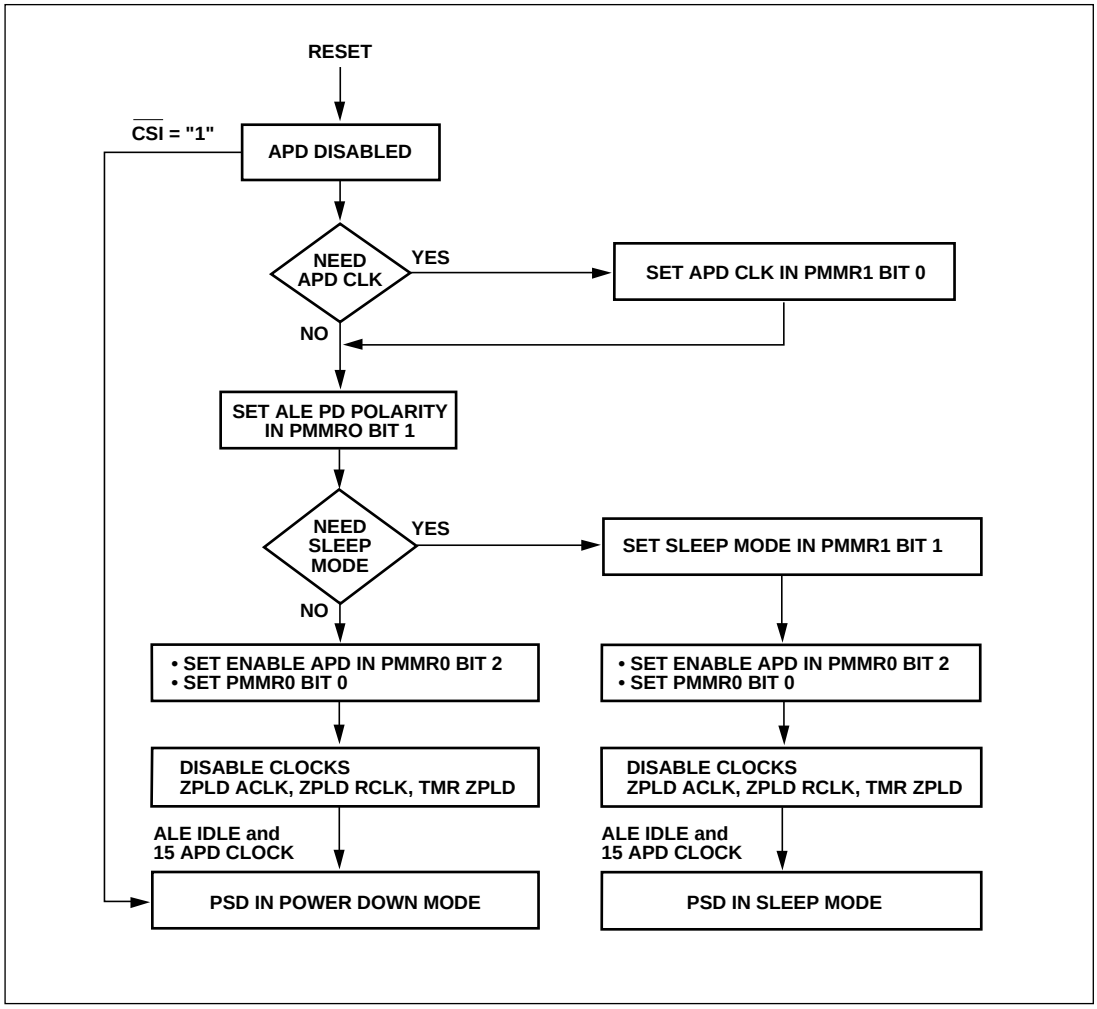


Figure 36a. Automatic Power Down Unit (APD) Flow Chart



The PSD4XX Architecture (cont.)

Table 18. Power Management Mode Registers (PMMR0, PMMR1)

PMMR0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR CLK	ZPLD RCLK	ZPLD ACLK	ZPLD TURBO	CMISER	APD ENABLE	ALE PD Polarity	*
1 = OFF	1 = OFF	1 = OFF	1 = OFF	1 = ON	1 = ON	1 = HIGH	

Bit 0 * = Should be set to High (1) to operate the APD.

Bit 1 0 = ALE Power Down (PD) Polarity Low.
1 = ALE Power Down (PD) Polarity High.

Bit 2 0 = Automatic Power Down (APD) Disable.
1 = Automatic Power Down (APD) Enable.

Bit 3 0 = EPROM/SRAM CMiser is OFF.
1 = EPROM/SRAM CMiser is ON.

Bit 4 0 = ZPLD Turbo is ON. ZPLD is always ON.
1 = ZPLD Turbo is OFF. ZPLD will Power Down when inputs are not changing.

Bit 5 0 = ZPLD Clock Input into the Array from the CLKIN pin input is connected. Every Clock change will Power Up the ZPLD when Turbo bit is OFF.
1 = ZPLD Clock Input into the Array from the CLKIN pin input is disconnected.

Bit 6 0 = ZPLD Clock Input into the the MacroCell registers from the CLKIN pin input is connected.
1 = ZPLD Clock Input into the the MacroCell registers from the CLKIN pin input is disconnected.

Bit 7 * = In the PSD4XX should be set to High (1)

PMMR1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	*	*	Sleep Mode	APD CLK
						1 = ON	1 = CLKIN

Bit 0 0 = Automatic Power Down Unit Clock is connected to Port E7 (PE7) alternate function input.
1 = Automatic Power Down Unit Clock is connected to the PSD Clock input (CLKIN).

Bit 1 0 = Sleep Mode Disabled.
1 = Sleep Mode Enabled.

Bit 2–7 0 = Reserved for future use, should be set to zero.

Table 19. APD Counter Operation

APD EN Bit	*ALE Power Down Polarity*	*ALE Status*	*APD Counter*
0	X	X	Not Counting
1	X	Pulsing	Not Counting
1	1	1	Counting (Activates Standby Mode After 15 Clocks)
1	0	0	Counting (Activates Standby Mode After 15 Clocks)

The PSD4XX Architecture (cont.)

9.5.2 Other Power Saving Options

The PSD4XX provides additional power saving options. These options, except the SRAM Standby Mode, can be enabled/disabled by setting up the corresponding bit in the PMMR.

❑ *EPROM*

The EPROM power consumption in the PSD is controlled by bit 3 in the PMMR0 – EPROM CMiser. Upon reset the CMiser bit is OFF. This will cause the EPROM to be ON at all times as long as CSI is enabled (low). The reason this mode is provided is to reduce the access time of the EPROM by 10 ns relative to the low power condition when CMiser is ON. If CSI is disabled (high) the EPROM will be deselected and will enter standby mode (OFF) overriding the state of the CMiser.

If CMiser is set (ON) then the EPROM will enter the standby mode when not selected. This condition can take place when CSI is high or when CSI is low and the EPROM is not accessed. For example, if the MCU is accessing the SRAM, the EPROM will be deselected and will be in low power mode.

An additional advantage of the CMiser is achieved when the PSD is configured in the by 8 mode (8 bit data bus). In this case an additional power savings is achieved in the EPROM (and also in the SRAM) by turning off 1/2 of the array even when the EPROM is accessed (the array is divided internally into odd and even arrays).

The power consumption for the different EPROM modes is given in the DC Characteristics table under I_{CC} (DC) EPROM Adder.

❑ *SRAM Standby Mode*

The SRAM has a dedicated supply voltage V_{STBY} that can be used to connect a battery. When V_{CC} becomes lower than V_{STBY} –0.6 then the PSD will automatically connect the V_{STBY} as a power source to the SRAM. The SRAM Standby Current (I_{STBY}) is typically 0.5 µA.

SRAM data retention voltage V_{DF} is 2 V minimum.

❑ *Zero Power ZPLD*

ZPLD power/speed is controlled by the ZPLD_Turbo bit (bit 4) in the PMMR0. After reset the ZPLD is in Turbo mode and runs at full power and speed. By setting the bit to “1”, the Turbo mode is disabled and the ZPLD is consuming Zero Power current if the inputs are not switching for an extended time of 70 ns. The propagation delay time will be increased by 10ns after the Turbo bit is set to “1” (turned off) if the inputs change at a frequency of less than 15 MHz.

The PSD4XX Architecture (cont.)

❑ Input Clock

The PSD4XX provides the option to turn off the clock inputs to save AC power consumption. The clock input (CLKIN) is used as a source for driving the following modules:

- ❑ ZPLD Array Clock Input
- ❑ ZPLD MacroCell Clock Flip Flop
- ❑ APD Counter Clock

During power down or if any of the modules are not being used the clock to these modules should be disabled. To reduce AC power consumption, it is especially important to disable the clock input to the ZPLD array if it is not used as part of a logic equation.

The ZPLD Array Clock can be disabled by setting PMMR0 bit 5 (ZPLD ACLK). The ZPLD MacroCell Clock Input can be disabled by setting PMMR0 bit 6 (ZPLD RCLK). The Timer Clock can be disabled by setting PMMR0 bit 7 (TMR CLK). The APD Counter Clock will be disabled automatically if Power Down or Sleep Mode is entered through the APD unit. The input buffer of the CLKIN input will be disabled if bits 5 – 7 PMMR0 are set and the APD has overflowed.

Summary of PSD4XX Timing and Standby Current During Power Down and Sleep Modes

	PLD Propagation Delay	*PLD Recovery Time To Normal Operation*	*Access Time*	*Access Recovery Time To Normal Access*
Power Down	Normal t_{PD} (Note 1)	0	No Access	t_{LVDV}
Sleep	t_{LVDV2} (Note 2)	t_{LVDV3} (Note 3)	No Access	t_{LVDV1}

NOTES: 1. Power Down does not affect the operation of the ZPLD. The ZPLD operation in this mode is based only on the ZPLD_Turbo Bit.
2. In Sleep Mode any input to the ZPLD will have a propagation delay of t_{LVDV2}.
3. PLD recovery time to normal operation after exiting Sleep Mode. An input to the ZPLD during the transition will have a propagation delay time of t_{LVDV3}.

Table 20. I/O Pin Status During Power Down And Sleep Mode

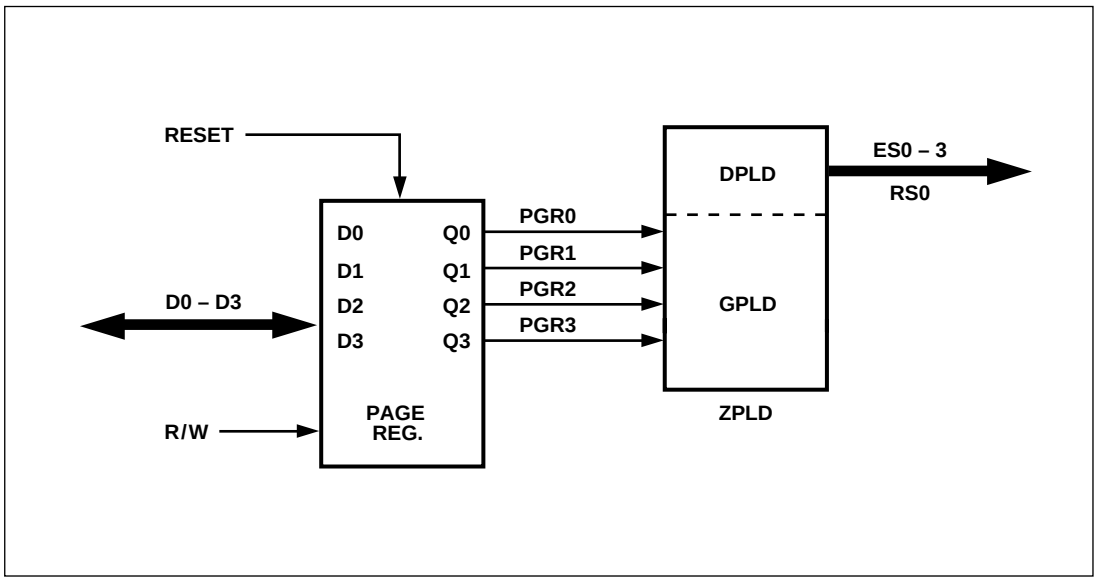
Port Configuration	*Pin Status*
I/O Port	Unchanged
ZPLD Output	Depend on Inputs to the ZPLD
Address Out	Undefined
Data Port	Tri-stated
Peripheral I/O	Tri-stated

10.0 Page Register

The Page Register is 4 bits wide and consists of four D flip flops.The outputs of the Register (PGR0 – PGR3) are connected to the input bus of the ZPLD. By including the four outputs as inputs to the DPLD, the addressing capability of the microcontroller is increased by a factor of 16.

Figure 37 shows the Page Register block diagram. Inputs to the four flip flops are connected to data bus D0-D3. The output of the Register can be read by the microcontroller. The Register can operate as an independent register to the microcontroller if page mode is not implemented.

Figure 35. Page Register



11.0 Security Protection

The PSD4XX has a programmable security bit which offers protection from unauthorized duplication. When the security bit is set, the contents of the EPROM, the PSD4XX non-volatile configuration bits and ZPLD data cannot be read by EPROM programmers.

The security bit is set through the PSDsoft Software and is embedded in the compiled output file. The security bit is UV erasable and a secured part can be erased and then re-programmed.

12.0 System Configuration

The CSIOP signal, which is generated by the DPLD, selects the internal I/O devices or registers. The CSIOP signal takes up 256 bytes of address space and is defined by the user in the PSDSoft Software. The following is an address offset map for the various devices relative to the CSIOP base address.

Some Motorola 16-bit microcontrollers have a different data bus/data byte orientation. This requires a different address offset for the internal PSD4XX I/O devices or registers. Tables 21a and 22a in this section are for this group of microcontrollers which include the M68HC16, M68302 and M683XX.

Table 21. Register Address Offset

Register Name	Address Offset	Register Name	Address Offset
		PAGE REGISTER	E0
		VM	C0
PMMR1	B1	PMMR0	B0

Table 21a. Register Address Offset

(For 16-bit Motorola Microcontrollers in 16-bit mode. Use Table 21 if 8-bit mode is selected.)

Register Name	Address Offset	Register Name	Address Offset
		PAGE REGISTER	E1
		VM	C1
PMMR1	B0	PMMR0	B1

12.0 System Configuration (cont.)

The following table is the address map offset of the I/O port registers.

Table 22. I/O Register Address Offset

Register Name	Address Offset				
	Port A	Port B	Port C	Port D	Port E
Data In	00	01	10	11	20
Control	02	03	12	13	22
Data Out	04	05	14	15	24
Direction	06	07	16	17	26
Open Drain			18	19	
PLD – I/O	0A	0B			2A
Macrocell Out	0C	0D			2C (PSD4XXA2/ ZPSD4XXA2)

Table 22a. Register Address Offset

(For 16-bit Motorola Microcontrollers in 16-bit mode. Use Table 22 if 8-bit mode is selected.)

Register Name	Address Offset				
	Port A	Port B	Port C	Port D	Port E
Data In	01	00	11	10	21
Control	03	02	13	12	23
Data Out	05	04	15	14	25
Direction	07	06	17	16	27
Open Drain			19	18	
PLD – I/O	0B	0A			2B
Macrocell Out	0D	0C			2D (PSD4XXA2/ ZPSD4XXA2)

System Configuration (cont.)

Table 23. Register Function

Register Name	Register Function
Data In	This Register is used to read the inputs on the port pins.
Control	A “0” sets the corresponding port pin in Address Out Mode. A “1” sets the pin in MCU I/O Mode.
Data Out	Holds the output data in the MCU I/O Mode.
Direction	This register is used to control the data flow in the I/O ports. A “0” sets the corresponding pin as an input pin. A “1” sets the pin as an output pin.
Open Drain	A “0” sets the corresponding pin driver as a CMOS driver. A “1” sets the pin driver as an Open Drain Driver.
PLD – I/O	A read only status register; a “1” indicates the corresponding pin is configured as a PLD pin.
Macrocell Out	This register holds the outputs of the GPLD macrocells.
Page Register	A 4-bit register that supports paging.
VM	1. Configures the PSD4XX SRAM to be accessed by “PSEN” as program space (8031 design). 2. Enables the Peripheral I/O Mode of Port A.
PMMR0 PMMR1	Power management registers; enables the PSD4XX Power Down Mode and other power saving configurations.

System Configuration (cont.)

12.1 Reset Input

The reset input to the PSD4XX (RESET) is an active low signal which resets some of the internal devices and configuration registers. The Timing Diagram in the AC/DC characterization section shows the reset signal timing requirement. The active low range has a minimum T1 duration. After the rising edge of RESET, the PSD4XX remains in reset during T2 range. (See Figure 48). The PSD4XX must be reset at power up before it can be used.

12.2 ZPLD and Memory During Reset

While the Reset Input is active, the ZPLD generates outputs as defined in the PSDabel equations. The EPROM and SRAM blocks respond to the microcontroller bus cycle during reset, but the data is not guaranteed.

12.3 Register Values During and After Reset

Table 24 summarizes the status of the volatile register values during and after reset. The default values of the volatile registers are “0” after reset.

12.4 ZPLD Macrocell Initialization

The D flip flops in the macrocells in the GPLD can be cleared by:

- ❏ A product term (.RE) defined by the user in PSDabel, or
- ❏ The MACRO-RST (Reset) input, enabled and defined in PSDabel.

Table 24. Registers Reset Values

Register Name	Device	Reset State
Control	Port A, B, C, D, E	Set to “0” (Address Out Mode)
Data Out (data or address)	Port A, B, C, D, E	Set to “0”
Direction	Port A, B, C, D, E	Set to “0” – Input Mode
Open Drain	Port C, D	Set to “0” – CMOS Outputs
Page Register	Page Logic	Set to “0”
PMMR0, PMMR1	Power Management Unit	Set to “0”
VM	Volatile Memory	Set to “0”

Table 25. I/O Pin Status During Reset and Standby Mode

Port Configuration	Reset	Stand-by Mode
Port I/O	Input	Unchanged
ZPLD Output	Active	Depend on Inputs to the ZPLD
Address Out	Tri-stated	Not Defined
Data Port	Tri-stated	Tri-stated
Peripheral I/O	Tri-stated	Tri-stated

13.0 Specifications

13.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CLDCC	– 65	+ 150	°C
		PLDCC	– 65	+ 125	°C
	Operating Temperature	Commercial	0	+ 70	°C
		Industrial	– 40	+ 85	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection		>2000		V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

13.2 Operating Range

Type	Temperature	V_{CC}	V_{CC} Tolerance	Speed Grades Available				
				-70	-90	-15	-20	-25
Commercial	0° C to +70°C	+ 5 V	± 10%	X		X		
		+ 3 V	± 10%				X	X
Industrial	–40° C to +85°C	+ 5 V	± 10%		X			
		+ 3 V	± 10%				X	

13.3 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5.0	5.5	V
V_{CC}	Supply Voltage	ZPSD4XXV Versions Only, All Speeds	2.7	3.0	5.5	V

Specifications
(cont.)

13.4 AC/DC Parameters

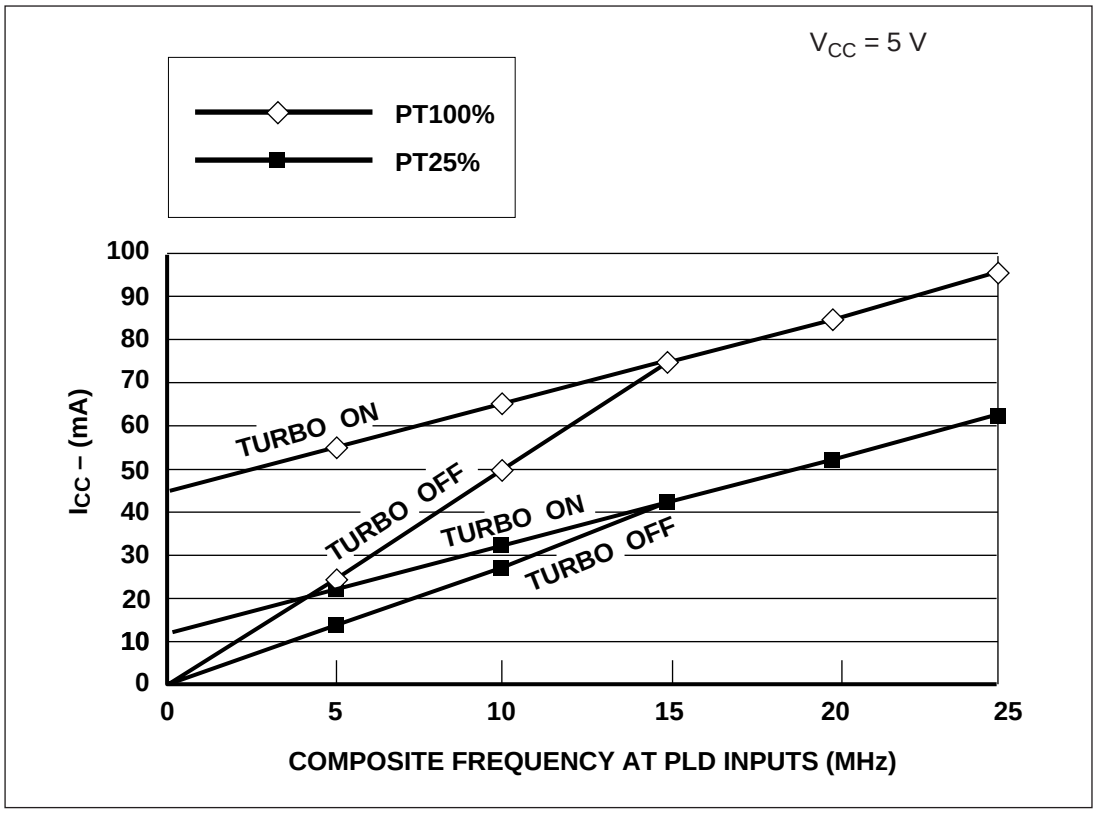
The following tables describe the AD/DC parameters of the PSD4XX family:

- ❏ DC Electrical Specification
- ❏ AC Timing Specification
  - ZPLD Timing
    - – Combinatorial Delays
    - – Synchronous Clock Mode
    - – Asynchronous Clock Mode
  - Microcontroller Timing
    - – Read Timing
    - – Write Timing
    - – Peripheral Mode Timing
    - – Power Down and Reset Timing

Following are some issues concerning the parameters presented:

- ❏ In the DC specification the Supply Current is given for different modes of operation. Before calculating the total power consumption, determine the percentage of time that the PSD4XX is in each mode. Also the supply power is considerably different if the ZPLD_TURBO bit is "OFF" and EPROM_CMISER is "ON".
- ❏ The AC power component gives the ZPLD, EPROM, and SRAM mA/MHz specification. Figure 38 shows the ZPLD mA/MHz as a function of the number of Product Terms (PT) used.
- ❏ In the ZPLD timing parameters add the required delay when ZPLD_TURBO is "OFF".
- ❏ In the MCU timing specification add the required time delay when EPROM_CMISER is "ON".

Figure 38a. Typical I_{CC}/Frequency Consumption (PSD4XXA1 and ZPSD4XXA1 Versions)



Specifications
(cont.)

Figure 38b. Typical I_{CC}/Frequency Consumption (PSD4XXA2 and ZPSD4XXA2 Versions)

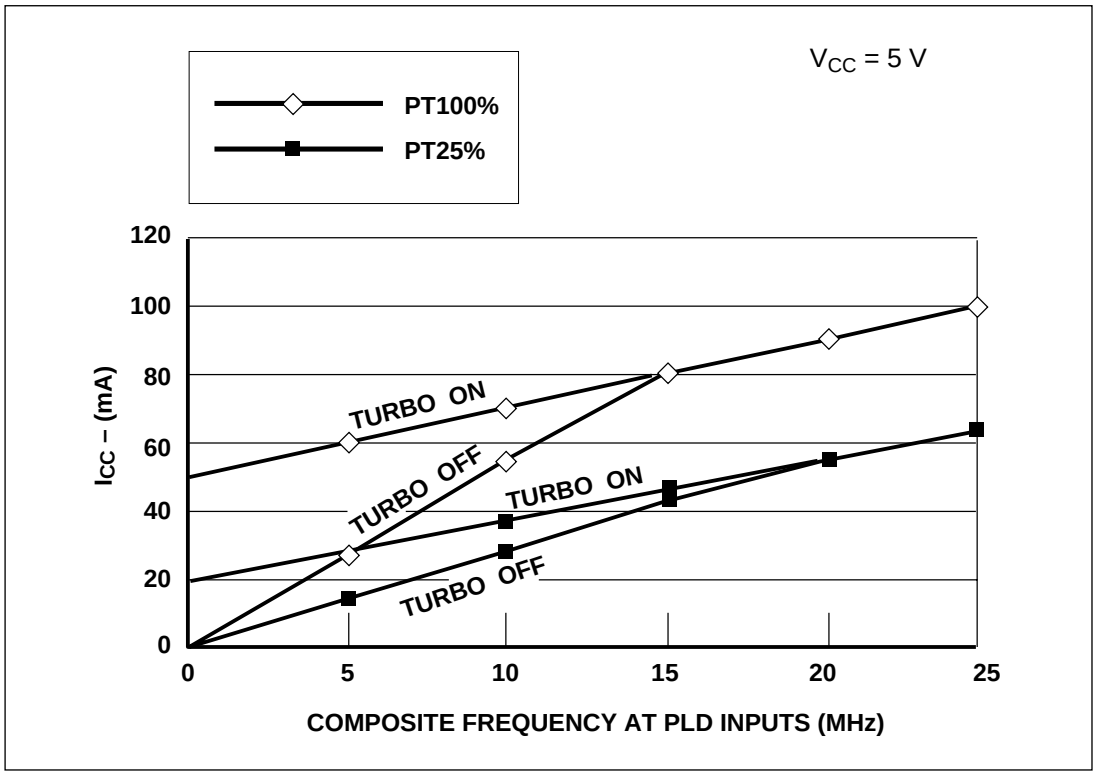
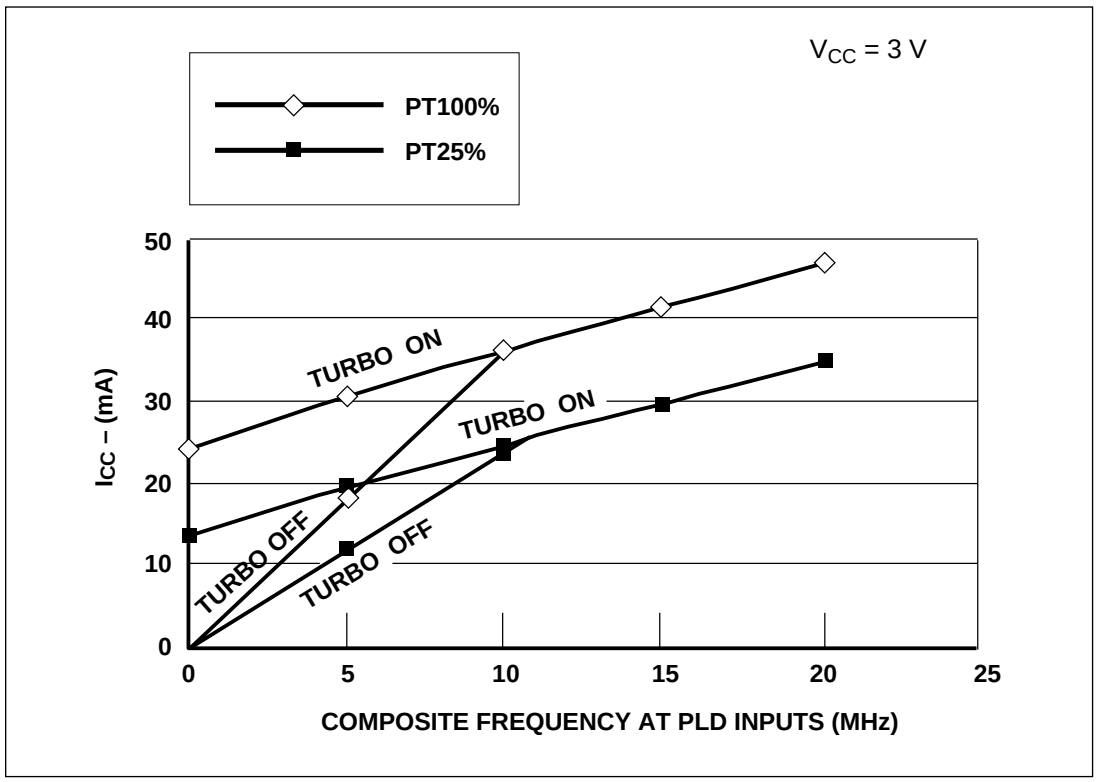


Figure 38c. Typical I_{CC}/Frequency Consumption (PSD4XXA1V and ZPSD4XXA2V Versions)



Specifications
(cont.)

13.5 Example of ZPSD4XX Typical Power Calculation at V_{CC} = 5.0 V

Conditions	
Composite PLD input frequency (Freq PLD)	= 8 MHz
MCU ALE frequency (Freq ALE)	= 4 MHz
% EPROM Access	= 80%
% SRAM access	= 15%
% I/O access	= 5% (no additional power above base)
Operational Modes	
% Normal	= 10%
% Sleep	= 90%
Number of product terms used (from fitter report)	= 29 PT
% of total product terms	= 29/118 = 24.6%
Turbo = off	
CMiser = on	
8-bit bus mode	

Calculation (typical numbers used)

I_{CC} total = Isleep x %sleep + %normal x (I_{CC} (ac) + I_{CC} (dc))
= Isleep x %sleep + %normal x (%EPROM x 0.8 mA/MHz x Freq ALE
+ %SRAM x 1.4 mA/MHz x Freq ALE
+ %PLD x 2.5 mA/MHz x Freq PLD + #PT x 400 µA/PT)
= 10 µA x 0.90 + 0.1 x (0.8 x 0.8 mA/MHz x 4 MHz
+ 0.15 x 1.4 mA/MHz x 4 MHz + 0.95 x 2.5 x 8 + 29 x 0.4 mA/PT)
= 0.9 µA + 0.1 x (2.56 + 0.84 + 19 + 11.6 mA)
= 0.9 µA + 0.1 x 34
= 0.9 µA + 3.4 mA
= 3.4 mA

Notes: Standby current consumption is handled similarly to Sleep Mode shown above. Calculation assumes I_{OUT} = 0 mA.

13.6 DC Characteristics (5 V ± 10% Versions)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		All Speeds	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		4.5 V < V_{CC} < 5.5 V	2		V_{CC} + 0.5	V
V_{IL}	Low Level Input Voltage		4.5 V < V_{CC} < 5.5 V	–0.5		0.8	V
V_{IH1}	Reset High Level Input Voltage		(Note 1)	0.8 V_{CC}		V_{CC} + 0.5	V
V_{IL1}	Reset Low Level Input Voltage		(Note 1)	–0.5		0.2 V_{CC} –0.1	V
V_{HYS}	Reset Pin Hysteresis			0.3			V
V_{OL}	Output Low Voltage		I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
			I_{OL} = 8 mA, V_{CC} = 4.5 V		0.15	0.45	V
V_{OH}	Output High Voltage		I_{OH} = –20 µA, V_{CC} = 4.5 V	4.4	4.49		V
			I_{OH} = –2 mA, V_{CC} = 4.5 V	2.4	3.9		V
V_{SBY}	SRAM Standby Voltage			2.7		V_{CC}	V
I_{SBY}	SRAM Standby Current		V_{CC} = 0 V		0.5	1	µA
I_{IDLE}	Idle Current (V_{STDBY} Pin)		V_{CC} > V_{SBY}	–0.1		0.1	µA
V_{DF}	SRAM Data Retention Voltage		Only on V_{STBY}	2			V
I_{SB1} (PSD4XX)	Standby Supply Current	Power Down Mode	$\overline{CSI}$ >V_{CC} –0.3 V (Note 2)		50	100	µA
		Sleep Mode	$\overline{CSI}$ >V_{CC} –0.3 V (Note 3)		30	40	µA
I_{SB2} (ZPSD4XX)	Standby Supply Current	Power Down Mode	CSI >V_{CC} –0.3 V (Note 2)		25	50	µA
		Sleep Mode	CSI >V_{CC} –0.3 V (Note 3)		10	20	µA
I_{LI}	Input Leakage Current		V_{SS} < V_{IN} < V_{CC}	–1	±0.1	1	µA
I_{LO}	Output Leakage Current		0.45 < V_{IN} < V_{CC}	–10	±5	10	µA
I_{CC} (DC) (Note 4a)	Operating Supply Current	ZPLD Adder	ZPLD_TURBO = OFF, f = 0 MHz (Note 4)		See I_{SB1} and I_{SB2}		
			ZPLD_TURBO = ON, f = 0 MHz		400	700	µA/PT
		EPROM Adder	f = 0 MHz		0		mA
		SRAM Adder	f = 0 MHz		0		mA
I_{CC} (AC) (Note 4a)	ZPLD AC Adder				See Fig. 38	4	mA/MHz
	EPROM AC Adder		CMiser = ON and (8-bit bus mode)		0.8	2	mA/MHz
			All other cases		1.8	4	mA/MHz
	SRAM AC Adder		CMiser = ON and (8-bit bus mode)		1.4	2.7	mA/MHz
			CMiser = ON and (16-bit bus mode)		2	4	mA/MHz
			CMiser = OFF		3.8	7.5	mA/MHz

NOTES: 1. Reset input has hysteresis. V_{IL1} is valid at or below 0.2V_{CC} –0.1. V_{IH1} is valid at or above 0.8V_{CC}.
2. $\overline{CSI}$ is high or internal Power Down mode is active.
3. Sleep mode bit is set and internal Power Down is active.
4. See ZPLD I_{CC}/Frequency Power Consumption graph for details.
4a. I_{OUT} = 0 mA.

13.7 AC/DC Parameters – ZPLD Timing Parameters (5 V ± 10% Versions)

Combinatorial Delays (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-70		-90**		-15		ZPLD_TURBO OFF*	Unit
			Min	Max	Min	Max	Min	Max		
t_{PD}	I/O Input or Feedback to Combinatorial Output	Port B, E		25		30		34	Add 10	ns
t_{RPD}	Registered Input to Combinatorial Output	(Note 1)		27		32		36	Add 10	ns
t_{EA}	Input to Output Enable	Any Input		25		28		32	Add 10	ns
t_{ER}	Input to Output Disable	Any Input		25		28		32	Add 10	ns
t_{ARP}	Register Clear or Preset Delay	Any Input		27		30		34	Add 10	ns
t_{ARPW}	Register Clear or Preset Pulse Width	Any Input	20		25		29			ns
t_{ARD}	Array Delay			16		18		22		ns

NOTE: 1. Port A and latched address from ADIO (A0, A1, A8 – A15).

*If ZPLD_TURBO is off and the ZPLD is operating above 15 MHz, there is no need to add 10 ns to the timing parameters.

**The -90 speed is available only on Industrial Temperature Range product.

Synchronous Clock Mode (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-15		ZPLD_TURBO OFF*	Unit
			Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Frequency External Feedback	$1/(t_S + t_{CO})$		30.30		27.03		23.81		MHz
	Maximum Frequency Internal Feedback (f_{CNT})	$1/(t_S + t_{CO} - 10)$		43.48		37.04		31.25		MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH} + t_{CL})$		50.00		41.67		33.33		MHz
t_S	Input Setup Time	Any Input	15		17		20		Add 10	ns
t_H	Input Hold Time	Any Input	0		0		0		0	ns
t_{CH}	Clock High Time	Clock Input	10		12		15		0	ns
t_{CL}	Clock Low Time	Clock Input	10		12		15		0	ns
t_{CO}	Clock to Output Delay	Clock Input		18		20		22	0	ns
t_{ARD}	Array Delay for Product Term Expansion	Any Macrocell		16		18		22	0	ns
t_{MIN}	Minimum Clock Period	$t_{CH} + t_{CL}$	20		24		29		0	ns

*If ZPLD_TURBO is off and the ZPLD is operating above 15 MHz, there is no need to add 10 ns to the timing parameters.

**The -90 speed is available only on Industrial Temperature Range product.

AC/DC Parameters – ZPLD Timing Parameters (5 V ± 10% Versions)

Asynchronous Clock Mode (5 V ± 10% , Note 1)

Symbol	Parameter	Conditions	-70		-90**		-15		ZPLD_TURBO OFF*	Unit
			Min	Max	Min	Max	Min	Max		
f_{MAXA}	Maximum Frequency External Feedback	$1/(t_{SA} + t_{COA})$		26.32		25.00		20.41		MHz
	Maximum Frequency Internal Feedback (f_{CNTA})	$1/(t_{SA}+t_{COA}–10)$ (Note 1)		35.71		33.33		25.64		MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH} + t_{CL})$		41.67		41.67		33.33		MHz
t_{SA}	Input Setup Time	Any Input	8		8		12		Add 10	ns
t_{HA}	Input Hold Time	Any Input	8		8		12		0	ns
t_{CHA}	Clock High Time	Any Input	12		12		15		0	ns
t_{CLA}	Clock Low Time	Any Input	12		12		15		0	ns
t_{COA}	Clock to Output Delay	Any Input to Port B		30		32		37	Add 10	ns
t_{ARD}	Array Delay for Product Term Expansion	Any Macrocell		16		18		22	0	ns
t_{MINA}	Minimum Clock Period	$1/f_{CNT}$	28		30		43		0	ns

NOTE: 1. Only Port B has asynchronous outputs. Clock into Macrocell Flip Flop is generated by a product term.

***** If ZPLD_TURBO is off and the ZPLD is operating above 15 MHz, there is no need to add 10 ns to the timing parameters.

****** The -90 speed is available only on Industrial Temperature Range product.

13.8 Microcontroller Interface – AC/DC Parameters (5 V ± 10% Versions)

Explanation of AC Symbols for Non ZPLD Timing.

Example: t_{AVLX} Time from Address Valid to ALE Invalid.

A – Address
C – Power Down
D– Input Data
E – E
H – Logic Level High
I – Interrupt
L – Logic Level Low or ALE
N – Reset
P – Port Signal
Q – Output Data
R – $\overline{WR}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DS}$, $\overline{IORD}$, $\overline{PSEN}$
S – Chip Select
T – R/$\overline{W}$
t – Time
V – Valid
X – No Longer a Valid Logic Level
Z – Float

Read Timing (5 V ± 10% Versions)

Symbol	*Parameter*	*Conditions*	*-70*		*-90**		*-15*		*EPROM_CMiser ON*	*Unit*
			Min	*Max*	*Min*	*Max*	*Min*	*Max*		
t_{LVLX}	ALE or AS Pulse Width		18		20		28		0	ns
t_{AVLX}	Address Setup Time	(Note 3)	5		6		10		0	ns
t_{LXAX}	Address Hold Time	(Note 3)	7		8		11		0	ns
t_{AVQV}	Address Valid to Data Valid	(Note 3)		70		90		150	Add 10	ns
t_{SLQV}	$\overline{CS}$ Valid to Data Valid			80		100		150	Add 10	ns
t_{RLQV}	$\overline{RD}$ to Data Valid 8/16-Bit Bus	(Note 1)		20		32		40	0	ns
	$\overline{RD}$ to Data Valid 8-Bit Bus, 8031 Separate Mode	(Note 2)		32		38		45	0	ns
t_{RHQX}	$\overline{RD}$ Data Hold Time	(Note 1)	0		0		0		0	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	(Note 1)	30		32		38		0	ns
t_{RHQZ}	$\overline{RD}$ to Data High-Z	(Note 1)		22		25		33	0	ns
t_{EHEL}	E Pulse Width		30		32		38		0	ns
t_{THEH}	R/$\overline{W}$ Setup Time to Enable		8		10		18		0	ns
t_{ELTL}	R/$\overline{W}$ Hold Time After Enable		0		0		0		0	ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 16-Bit Data Bus Mode (Note 9)		20		30		38	0	ns
		In 8-Bit Data Bus Mode (Note 9)		22		32		48	0	ns

NOTES: 1. $\overline{RD}$ timing has the same timing as $\overline{PSEN}$, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$ signals.
2. $\overline{RD}$ and $\overline{PSEN}$ have the same timing for 8031 mode.
3. Any input used to select an internal PSD4XX function.
4. In multiplexed mode latched address generated from ADIO delay to address output on any Port.

*****The -90 speed is available only on Industrial Temperature Range product.

Microcontroller Interface – AC/DC Parameters (5 V ± 10% Versions)

Write Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90*		-15		EPROM_CMiserON	Unit
			Min	Max	Min	Max	Min	Max		
t_{LVLX}	ALE or AS Pulse Width		18		20		28			ns
t_{AVLX}	Address Setup Time	(Note 1)	5		6		10			ns
t_{LXAX}	Address Hold Time	(Note 1)	7		8		11			ns
t_{AVWL}	Address Valid to Leading Edge of $\overline{WR}$	(Notes 1 and 3)	18		20		30			ns
t_{SLWL}	$\overline{CS}$ Valid to Leading Edge of $\overline{WR}$	(Note 3)	22		25		35			ns
t_{DVWH}	$\overline{WR}$ Data Setup Time	(Note 3)	12		15		22			ns
t_{WHDX}	$\overline{WR}$ Data Hold Time	(Note 3)	5		5		5			ns
t_{WLWH}	$\overline{WR}$ Pulse Width	(Note 3)	18		20		28			ns
t_{WHAX}	Trailing Edge of $\overline{WR}$ to Address Invalid	(Note 3)	0		0		0			ns
t_{WHPV}	Trailing Edge of $\overline{WR}$ to Port Output Valid	(Note 3)		25		30		38		ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 16-Bit Data Bus Mode (Note 2)		20		30		38		ns
		In 8-Bit Data Bus Mode (Note 2)		22		32		48		ns

NOTES: 1. Any input used to select an internal PSD4XX function.
2. In multiplexed mode latched address generated from ADIO delay to address output on any Port.
3. WR timing has the same timing as E, DS, LDS, UDS, WRL, WRH signals.

***The -90 speed is available only on Industrial Temperature Range product.

Microcontroller Interface – AC/DC Parameters (5 V ± 10% Versions)

Port A Peripheral Data Mode Read Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-15		ZPLD_TURBO OFF*	Unit
			Min	Max	Min	Max	Min	Max		
$t_{AVQV (PA)}$	Address Valid to Data Valid	(Note 3)		45		55		62	Add 10	ns
$t_{SLQV (PA)}$	$\overline{CS}$ Valid to Data Valid			55		55		62	Add 10	ns
$t_{RLQV (PA)}$	$\overline{RD}$ to Data Valid	(Notes 1 and 4)		22		26		45	0	ns
	$\overline{RD}$ to Data Valid 8031 Mode			32		38		45	0	ns
$t_{DVQV (PA)}$	Data In to Data Out Valid			22		22		26	0	ns
$t_{QXRH (PA)}$	$\overline{RD}$ Data Hold Time	(Note 1)	0		0		0		0	ns
$t_{RLRH (PA)}$	$\overline{RD}$ Pulse Width	(Note 1)	25		30		38		0	ns
$t_{RHQZ (PA)}$	$\overline{RD}$ to Data High-Z	(Note 1)		20		25		33	0	ns

Port A Peripheral Data Mode Write Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-15		ZPLD_TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max		
$t_{WLQV (PA)}$	$\overline{WR}$ to Data Propagation Delay	(Note 2)		25		27		35	0	ns
$t_{DVQV (PA)}$	Data to Port A Data Propagation Delay	(Note 5)		22		22		26	0	ns
$t_{WHQZ (PA)}$	$\overline{WR}$ Invalid to Port A Tri-state	(Note 2)		20		25		33		ns

NOTES: 1. $\overline{RD}$ timing has the same timing as $\overline{PSEN}$, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$ signals.
2. $\overline{WR}$ timing has the same timing as E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{WRL}$, $\overline{WRH}$ signals.
3. Any input used to select Port A Data Peripheral Mode.
4. Data is already stable on Port A.
5. Data stable on ADIO pins to data on Port A.

*If ZPLD_TURBO is off and the ZPLD is operating above 15 MHz, there is no need to add 10 ns to the timing parameters.

**The -90 speed is available only on Industrial Temperature Range product.

Microcontroller Interface – AC/DC Parameters (5 V ± 10% Versions)

Power Down and Reset Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90*		-15		ZPLD_TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max		
t_{LVDV}	ALE Access Time from Power Down			100		120		150	Add 10	ns
t_{LVDV1}	ALE or $\overline{CSI}$ Access Time from Sleep			120		150		200	0	ns
t_{LVDV2}	ZPLD Propagation Delay in Sleep Mode			600		600		600	0	ns
t_{LVDV3}	ZPLD Recovery Time after Sleep Mode			250		250		250	0	ns
t_{CHCL}	APD Clock High Time	Using PE7	10		12		15		0	ns
t_{CLCH}	APD Clock Low Time	Using PE7	10		12		15		0	ns
f_{MAX}	APD Maximum Frequency	Using PE7		35.00		30.00		22.00	0	MHz
t_1	RESET Active Low Time		150		200		300		0	ns
t_2	RESET High to Operational Device			150		200		300	0	ns

*The -90 speed is available only on Industrial Temperature Range product.

13.9 DC Characteristics (ZPSD4XXV Versions)

(3.0 V ± 10% Versions)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		All Speeds	2.7	3	5.5	V
V_{IH}	High Level Input Voltage		2.7 V < V_{CC} < 5.5 V	.7 V_{CC}		V_{CC} +.5	V
V_{IL}	Low Level Input Voltage		2.7 V < V_{CC} < 5.5 V	–0.5		.3 V_{CC}	V
V_{IH1}	Reset High Level Input Voltage		(Note 1)	.8 V_{CC}		V_{CC} +.5	V
V_{IL1}	Reset Low Level Input Voltage		(Note 1)	–.5		.2 V_{CC} –.1	V
V_{HYS}	Reset Pin Hysteresis			0.3			V
V_{OL}	Output Low Voltage		I_{OL} = 20 µA, V_{CC} = 2.7 V		0.01	0.1	V
			I_{OL} = 4 mA, V_{CC} = 2.7 V		0.15	0.45	V
V_{OH}	Output High Voltage		I_{OH} = –20 µA, V_{CC} = 2.7 V	2.9	2.99		V
			I_{OH} = –1 mA, V_{CC} = 2.7 V	2.4	2.6		V
V_{SBY}	SRAM Standby Voltage			2.7		V_{CC}	V
I_{SBY}	SRAM Standby Current		V_{CC} = 0 V		0.5	1	µA
I_{IDLE}	Idle Current (V_{STBY} Pin)		V_{CC} > V_{SBY}	–0.1		0.1	µA
V_{DF}	SRAM Data Retention Voltage		Only on V_{STBY}	2			V
I_{SB}	Standby Supply Current	Power Down Mode	$\overline{CSI}$ >V_{CC} –.3 V (Note 2)		5	15	µA
		Sleep Mode	$\overline{CSI}$ >V_{CC} –.3 V (Note 3)		1	5	µA
I_{LI}	Input Leakage Current		V_{SS} < V_{IN} < V_{CC}	–1	±.1	1	µA
I_{LO}	Output Leakage Current		0.45 < V_{IN} < V_{CC}	–10	±5	10	µA
I_{CC} (DC) (Note 5)	Operating Supply Current	ZPLD Only	ZPLD_TURBO = OFF, f = 0 MHz (Note 4)		See I_{SB}		µA
			ZPLD_TURBO = ON, f = 0 MHz		200	400	µA/PT
I_{CC} (AC) (Note 5)	ZPLD AC Base		(Note 4)		See Fig 38c	2.0	mA/MHz
	EPROM AC Adder		CMiser = ON (8-Bit Bus Mode)		0.4	1.0	mA/MHz
			All Other Cases		0.9	1.7	mA/MHz
	SRAM AC Adder		CMiser = ON and 8-Bit Bus Mode		0.7	1.3	mA/MHz
			CMiser = ON and 16-Bit Bus MoDe		1	2	mA/MHz
			CMiser = OFF		1.9	3.8	mA/MHz

NOTES: 1. Reset input has hysteresis. V_{IL1} is valid at or below .2V_{CC} –.1. V_{IH1} is valid at or above .8V_{CC}.
2. $\overline{CSI}$ deselected or internal PD is active.
3. Sleep mode bit is set and internal PD is active.
4. See ZPLD ICC/Frequency Power Consumption graph for details.
5. I_{OUT} = 0 mA.

13.10 AC/DC Parameters – ZPLD Timing Parameters (ZPSD4XXV Versions)

(3.0 V ± 10%)

Combinatorial Delays (3.0 V ± 10%)

Symbol	Parameter	Conditions	-20		-25		ZPLD_TURBO OFF*	Unit
			Min	Max	Min	Max		
t_{PD}	I/O Input or Feedback to Combinatorial Output	Port B, E		55		80	Add 20	ns
t_{RPD}	Registered Input to Combinatorial Output	(Note 1)		55		85	Add 20	ns
t_{EA}	Input to Output Enable	Any Input		50		80	Add 20	ns
t_{ER}	Input to Output Disable	Any Input		50		80	Add 20	ns
t_{ARP}	Register Clear or Preset Delay	Any Input		55		80	Add 20	ns
t_{ARPW}	Register Clear or Preset Pulse Width	Any Input	30		60			ns
t_{ARD}	Array Delay			33		35		ns

NOTE: 1. Port A and latched address from ADIO (A0, A1, A8 – A15).

Synchronous Clock Mode (3.0 V ± 10%)

Symbol	Parameter	Conditions	-20		-25		ZPLD_TURBO OFF*	Unit
			Min	Max	Min	Max		
f_{MAX}	Maximum Frequency External Feedback	$1/(t_S + t_{CO})$		28.57		11.11		MHz
	Maximum Frequency Internal Feedback (f_{CNT})	$1/(t_S + t_{CO} - 10)$		17.24		12.50		MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH} + t_{CL})$		31.25		18.52		MHz
t_S	Input Setup Time	Any Input	45		60		Add 20	ns
t_H	Input Hold Time	Any Input	0		0		0	ns
t_{CH}	Clock High Time	Clock Input	16		27		0	ns
t_{CL}	Clock Low Time	Clock Input	16		27		0	ns
t_{CO}	Clock to Output Delay	Clock Input		30		33	0	ns
t_{ARD}	Array Delay for Product Term Expansion	Any Macrocell		24		35	0	ns
t_{MIN}	Minimum Clock Period	$t_{CH} + t_{CL}$	30		30		0	ns

***NOTE:** If ZPLD_TURBO is off and the ZPLD is operating above 15 MHz, there is no need to add 20 ns to the timing parameters.

AC/DC Parameters – ZPLD Timing Parameters (ZPSD4XXV Versions)

(3.0 V ± 10%)

Asynchronous Clock Mode (3.0 V ± 10%, Note 1)

Symbol	Parameter	Conditions	-20		-25		ZPLD_TURBO OFF*	Unit
			Min	Max	Min	Max		
f_{MAXA}	Maximum Frequency External Feedback	$1/(t_{SA} + t_{COA})$		14.49		11.11		MHz
	Maximum Frequency Internal Feedback (f_{CNTA})	$1/(t_{SA}+t_{COA}–10)$ (Note 1)		16.95		12.50		MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH} + t_{CL})$		31.25		18.52		MHz
t_{SA}	Input Setup Time	Any Input	13		30		Add 20	ns
t_{HA}	Input Hold Time	Any Input	13		30		0	ns
t_{CHA}	Clock High Time	Any Input	25		27		0	ns
t_{CLA}	Clock Low Time	Any Input	16		27		0	ns
t_{COA}	Clock to Output Delay	Any Input to Port B		56		60	Add 20	ns
t_{ARD}	Array Delay for Product Term Expansion	Any Macrocell	33			35	0	ns
t_{MINA}	Minimum Clock Period	$1/f_{CNT}$	59		80		0	ns

NOTE: 1. Only Port B has asynchronous outputs. Clock into macrocell Flip Flop is generated by a product term.

*If ZPLD_TURBO is off and the ZPLD is operating above 15 MHz, there is no need to add 20 ns to the timing parameters.

13.11 Microcontroller Interface – AC/DC Parameters (ZPSD4XXV Versions)

(3.0 V ± 10%)

Explanation of AC Symbols for Non ZPLD Timing.

Example: t_{AVLX} Time from Address Valid to ALE Invalid.

A – Address
C – Power Down
D– Input Data
E – E
H – Logic Level High
I – Interrupt
L – Logic Level Low or ALE
N – Reset
P – Port Signal
Q – Output Data
R – $\overline{WR}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DS}$, $\overline{IORD}$, $\overline{PSEN}$
S – Chip Select
T – R/$\overline{W}$
t – Time
V – Valid
X – No Longer a Valid Logic Level
Z – Float

Read Timing (3.0 V ± 10%)

Symbol	Parameter	Conditions	-20		-25		EPROM_CMiser ON	Unit
			Min	Max	Min	Max		
t_{LVLX}	ALE or AS Pulse Width		30		30		0	ns
t_{AVLX}	Address Setup Time	(Note 3)	12		15		0	ns
t_{LXAX}	Address Hold Time	(Note 3)	12		17		0	ns
t_{AVQV}	Address Valid to Data Valid	(Note 3)		200		250	Add 20	ns
t_{SLQV}	$\overline{CS}$ Valid to Data Valid			200		275	Add 20	ns
t_{RLQV}	$\overline{RD}$ to Data Valid 8/16-Bit Bus	(Note 1)		50		80	0	ns
	$\overline{RD}$ to Data Valid 8-Bit Bus, 8031 Separate Mode	(Note 2)		57		90	0	ns
t_{RHQX}	$\overline{RD}$ Data Hold Time	(Note 1)	0		0		0	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	(Note 1)	40		70		0	ns
t_{RHQZ}	$\overline{RD}$ to Data High-Z	(Note 1)		45		45	0	ns
t_{EHEL}	E Pulse Width		40		70		0	ns
t_{THEH}	R/$\overline{W}$ Setup Time to Enable		20		15		0	ns
t_{ELTL}	R/$\overline{W}$ Hold Time After Enable		0		0		0	ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 16-Bit Data Bus Mode (Note 4)		40		60	0	ns
		In 8-Bit Data Bus Mode (Note 4)		50		60	0	ns

NOTES: 1. $\overline{RD}$ timing has the same timing as $\overline{PSEN}$, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$ signals.
2. $\overline{RD}$ and $\overline{PSEN}$ have the same timing for 8031 mode.
3. Any input used to select an internal PSD4XX function.
4. In multiplexed mode latched address generated from ADIO delay to address output on any Port.

Microcontroller Interface – AC/DC Parameters (ZPSD4XXV Versions)

(3.0 V ± 10%)

Write Timing (3.0 V ± 10%)

Symbol	Parameter	Conditions	-20		-25		EPROM_CMiser ON	Unit
			Min	Max	Min	Max		
t_{LVLX}	ALE or AS Pulse Width		30		30			ns
t_{AVLX}	Address Setup Time	(Note 1)	12		15			ns
t_{LXAX}	Address Hold Time	(Note 1)	12		17			ns
t_{AVWL}	Address Valid to Leading Edge of $\overline{WR}$	(Notes 1 and 3)	35		50			ns
t_{SLWL}	$\overline{CS}$ Valid to Leading Edge of $\overline{WR}$	(Note 3)	40		60			ns
t_{DVWH}	$\overline{WR}$ Data Setup Time	(Note 3)	25		35			ns
t_{WHDX}	$\overline{WR}$ Data Hold Time	(Note 3)	5		10			ns
t_{WLWH}	$\overline{WR}$ Pulse Width	(Note 3)	30		30			ns
t_{WHAX}	Trailing Edge of $\overline{WR}$ to Address Invalid	(Note 3)	0		0			ns
t_{WHPV}	Trailing Edge of $\overline{WR}$ to Port Output Valid	(Note 3)		50		60		ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 16-Bit Data Bus Mode (Note 2)		40		60		ns
		In 8-Bit Data Bus Mode (Note 2)		50		60		ns

NOTES: 1. Any input used to select an internal PSD4XX function.
2. In multiplexed mode latched address generated from ADIO delay to address output on any Port.
3. $\overline{WR}$ timing has the same timing as E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{WRL}$, $\overline{WRH}$ signals.

Microcontroller Interface – AC/DC Parameters (ZPSD4XXV Versions)

(3.0 V ± 10%)

Port A Peripheral Data Mode Read Timing (3.0 V ± 10%)

Symbol	Parameter	Conditions	-20		-25		ZPLD_TURBO OFF	Unit
			Min	Max	Min	Max		
$t_{AVQV\ (PA)}$	Address Valid to Data Valid	(Note 3)		95		120	Add 20	ns
$t_{SLQV\ (PA)}$	$\overline{CS}$ Valid to Data Valid			100		120	Add 20	ns
$t_{RLQV\ (PA)}$	$\overline{RD}$ to Data Valid	(Notes 1 and 4)		50		90	0	ns
$t_{DVQV\ (PA)}$	Data In to Data Out Valid			35		50	0	ns
$t_{QXRH\ (PA)}$	$\overline{RD}$ Data Hold Time	(Note 1)	0		0		0	ns
$t_{RLRH\ (PA)}$	$\overline{RD}$ Pulse Width	(Note 1)	40		70		0	ns
$t_{RHQZ\ (PA)}$	$\overline{RD}$ to Data High-Z	(Note 1)		35		60	0	ns

Port A Peripheral Data Mode Write Timing (3.0 V ± 10%)

Symbol	Parameter	Conditions	-20		-25		ZPLD_TURBO OFF	Unit
			Min	Max	Min	Max		
$t_{WLQV\ (PA)}$	$\overline{WR}$ to Data Propagation Delay	(Note 2)		60		60	0	ns
$t_{DVQV\ (PA)}$	Data to Port A Data Propagation Delay	(Note 5)		40		50	0	ns
$t_{WHQZ\ (PA)}$	$\overline{WR}$ Invalid to Port A Tri-state	(Note 2)		35		60	0	ns

NOTES: 1. $\overline{RD}$ timing has the same timing as $\overline{PSEN}$, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$ signals.
2. $\overline{WR}$ timing has the same timing as E, DS, LDS, UDS, WRL, WRH signals.
3. Any input used to select Port A Data Peripheral Mode.
4. Data is already stable on Port A.
5. Data stable on ADIO pins to data on Port A.

Microcontroller Interface – AC/DC Parameters

(3.0 V ± 10%)

Power Down and Reset Timing (3.0 V ± 10%)

Symbol	Parameter	Conditions	-20		-25		ZPLD_TURBO OFF	Unit
			Min	Max	Min	Max		
t_{LVDV}	ALE Access Time from Power Down			170		250	Add 20	ns
t_{LVDV1}	ALE or $\overline{CSI}$ Access Time from Sleep			200		250	0	ns
t_{LVDV2}	ZPLD Propagation Delay in Sleep Mode			600		900	0	ns
t_{LVDV3}	ZPLD Recovery Time after Sleep Mode			250		400	0	ns
t_{CHCL}	APD Clock High Time	Using PE7	16		27		0	ns
t_{CLCH}	APD Clock Low Time	Using PE7	16		27		0	ns
f_{MAX}	APD Maximum Frequency	Using PE7		20.00		18.52	0	MHz
t_1	RESET Active Low Time		300		400		0	ns
t_2	RESET High to Operational Device			300		400	0	ns

14.0 Timing Diagrams

Figure 39. Read Timing

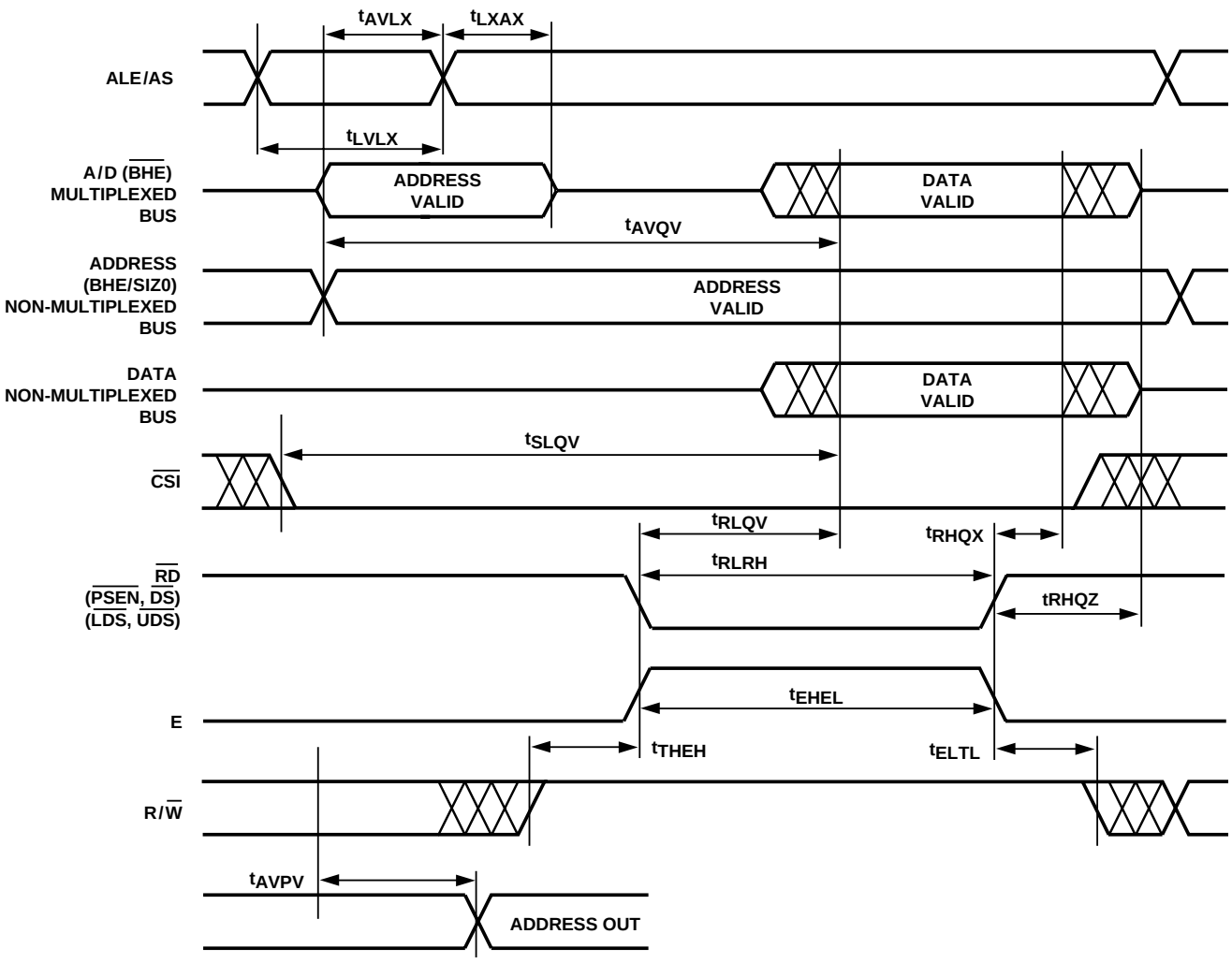


Figure 40. Write Timing

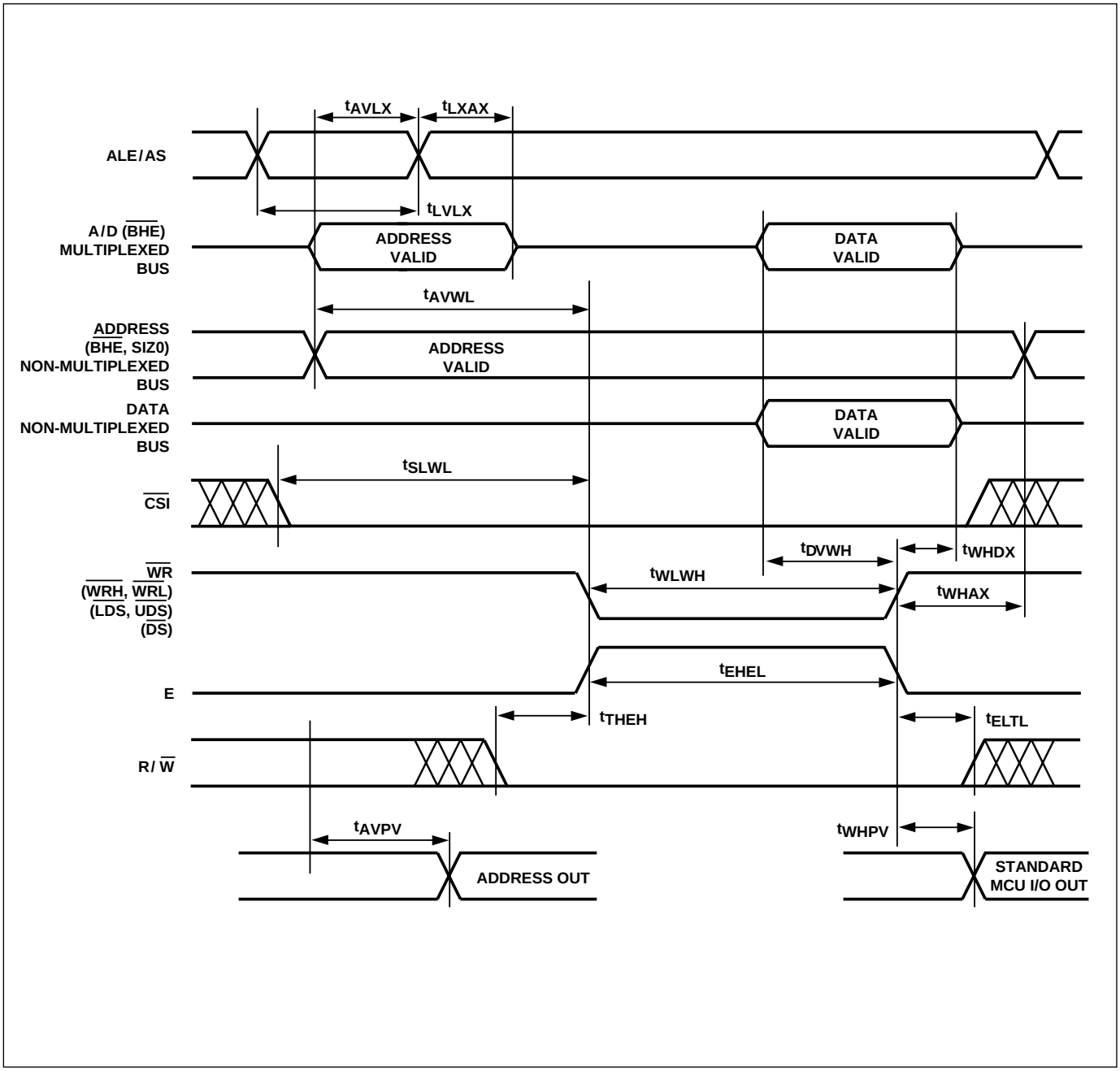


Figure 41. Peripheral I/O Read Timing

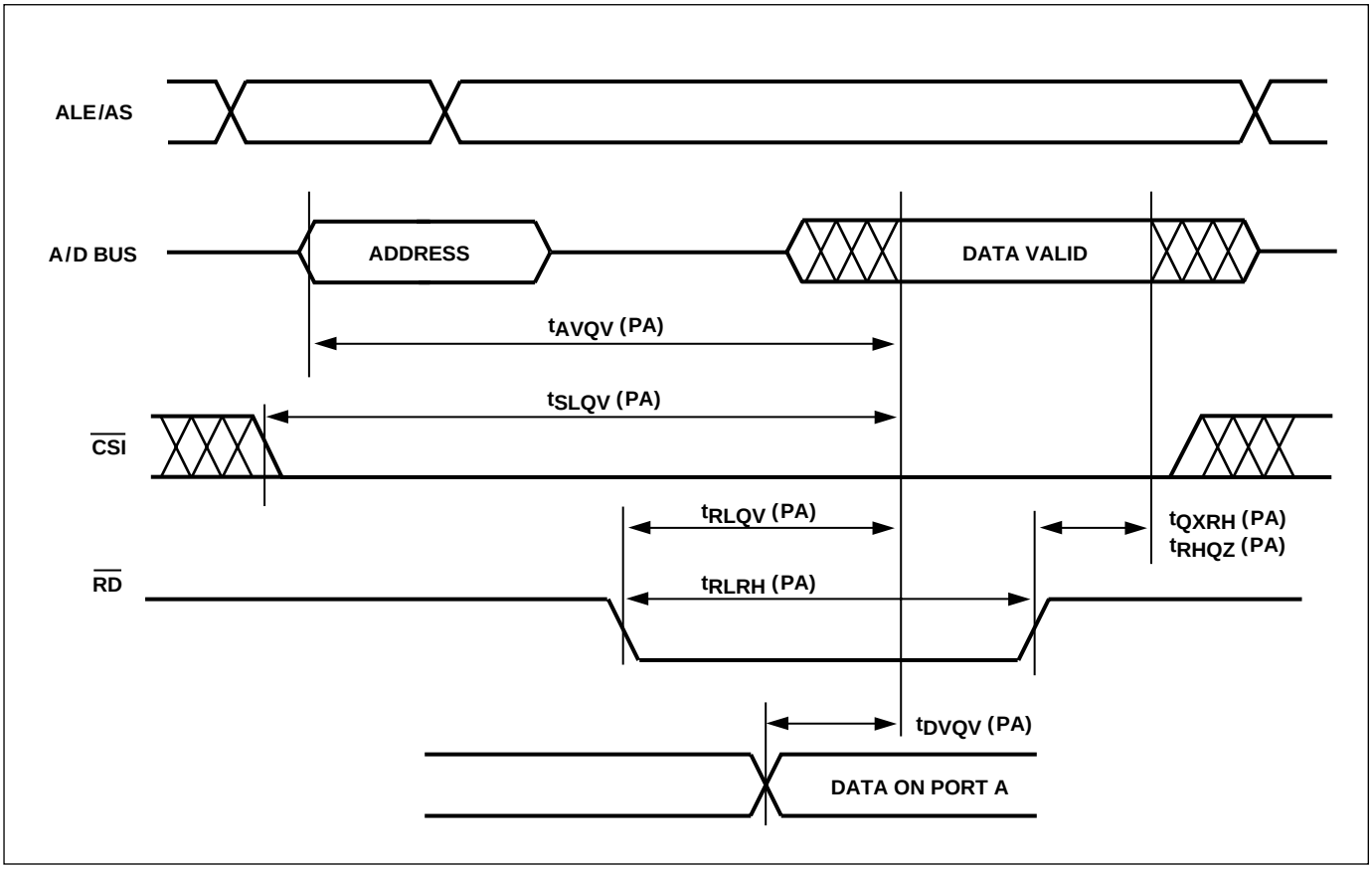


Figure 42. Peripheral I/O Write Timing

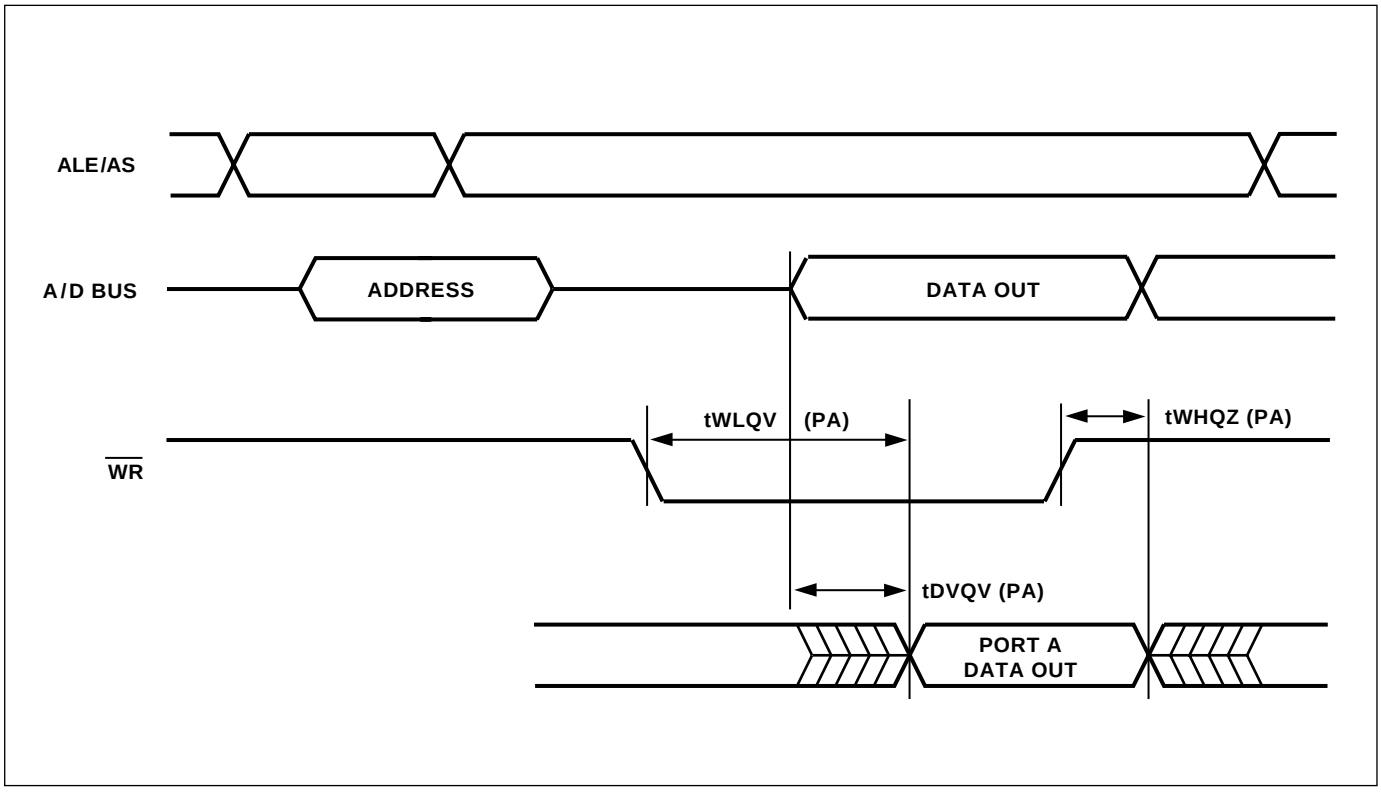


Figure 43. Combinatorial Timing – ZPLD

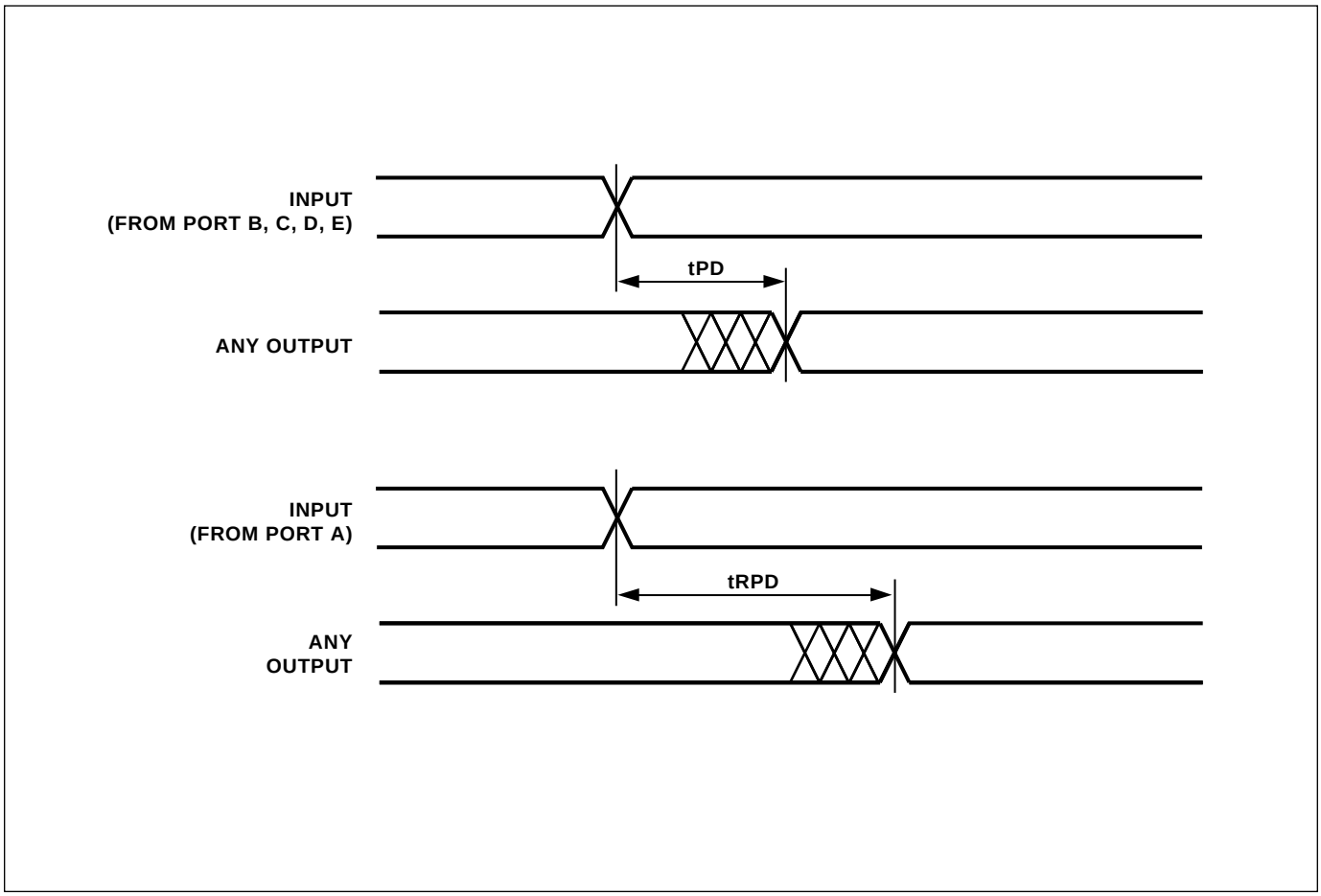


Figure 44. Synchronous Clock Mode Timing – ZPLD

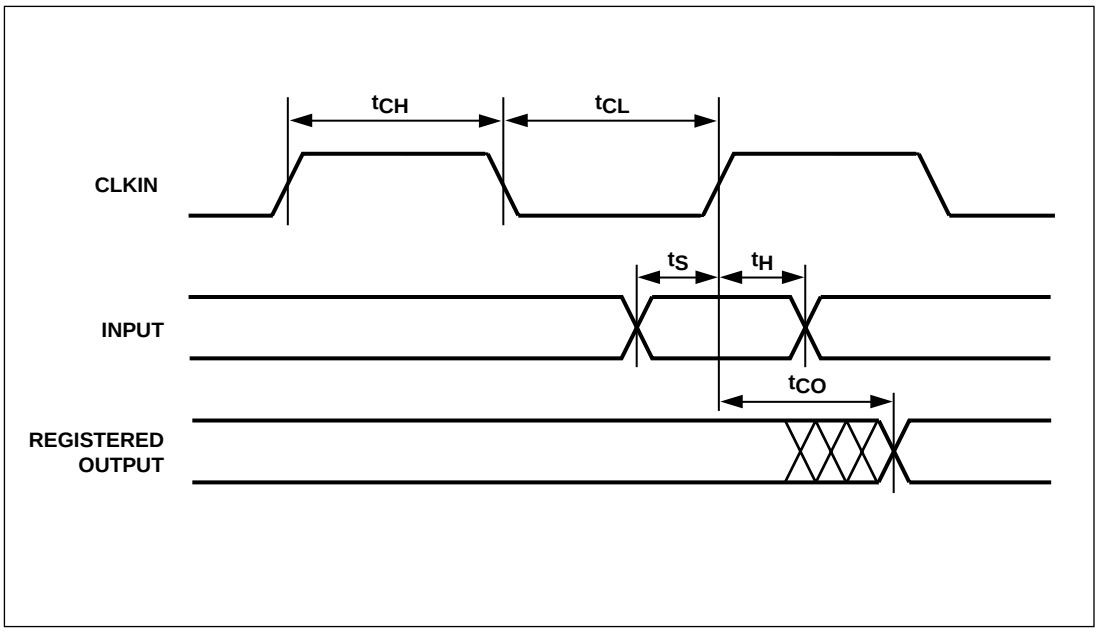


Figure 45. Asynchronous Clock Mode Timing (Product-Term Clock, PB MacrocelI 0nly)

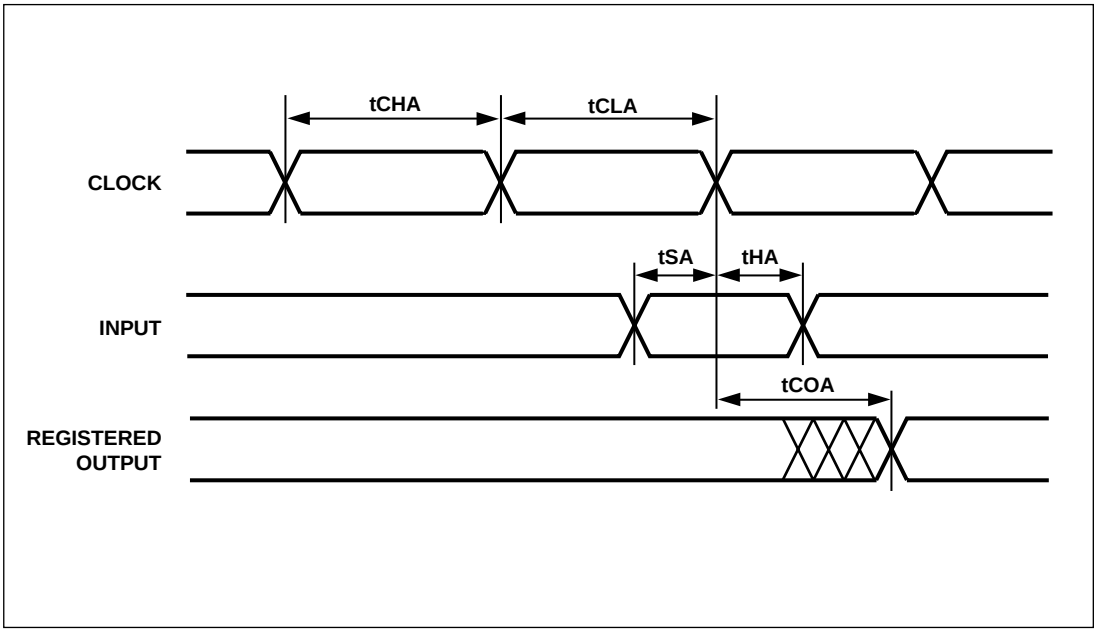


Figure 46. Input to Output Disable/Enable

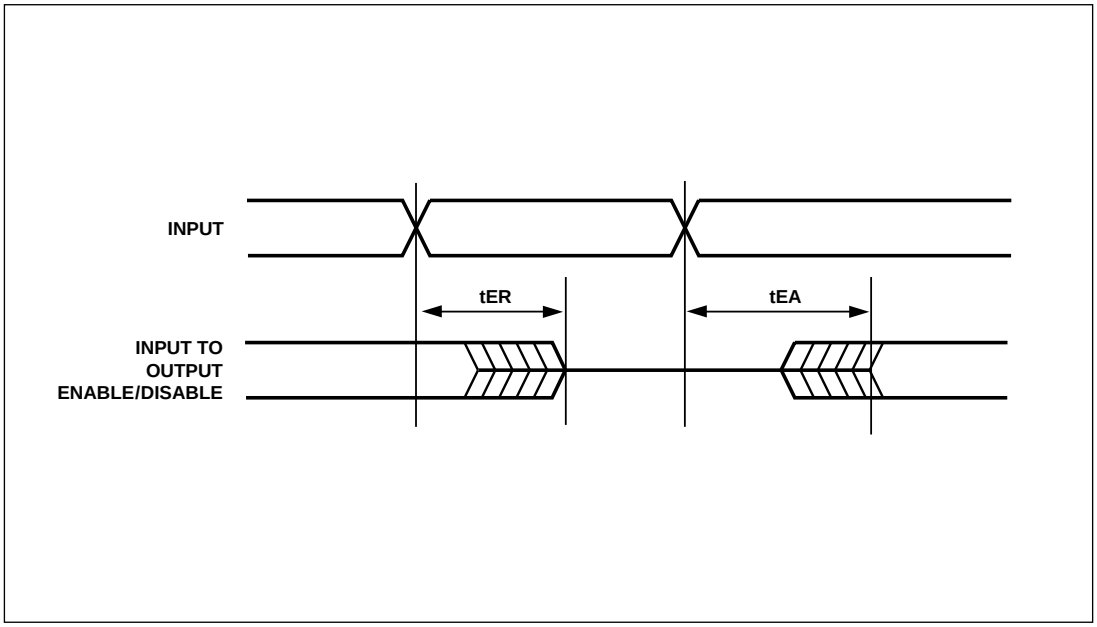


Figure 47. Asynchronous Reset/Preset

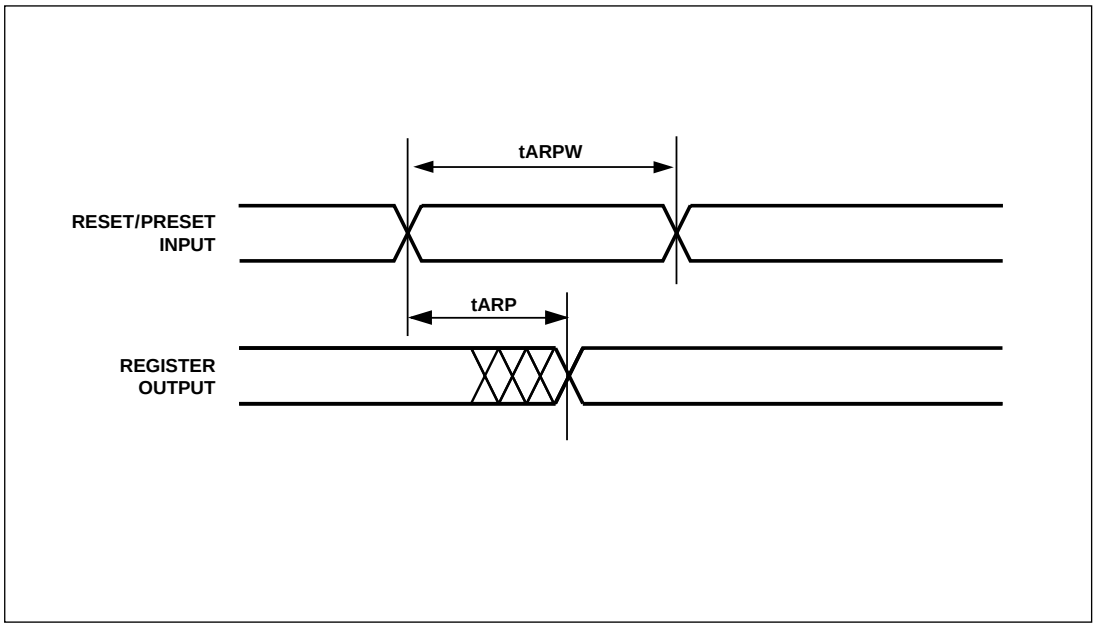


Figure 48. Reset Timing

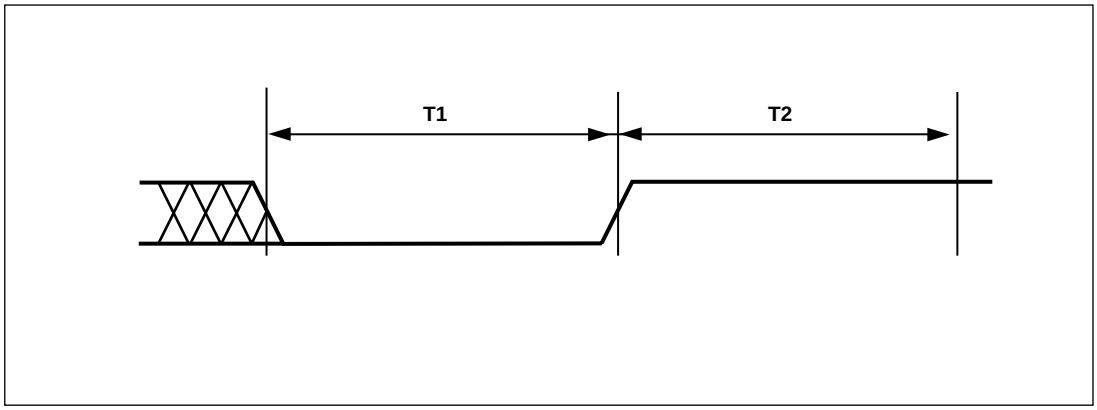
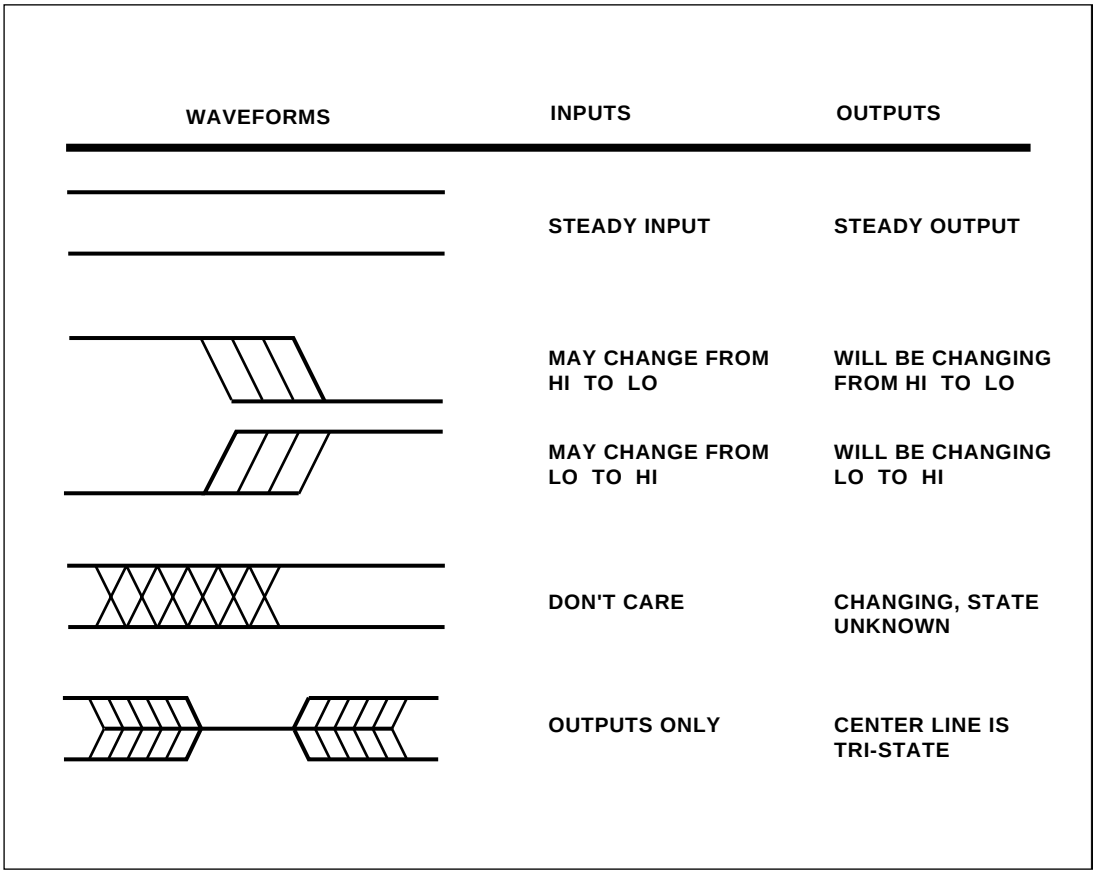


Figure 49. Key to Switching Waveforms



15.0 Pin Capacitance

T_A = 25 °C, f = 1 MHz

Symbol	Parameter[14]	Conditions	Typical[15]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 14. These parameters are only sampled and are not 100% tested.
15. Typical values are for T_A = 25°C and nominal supply voltages.

16.0 AC Testing

Figure 50. AC Testing Input/Output Waveform

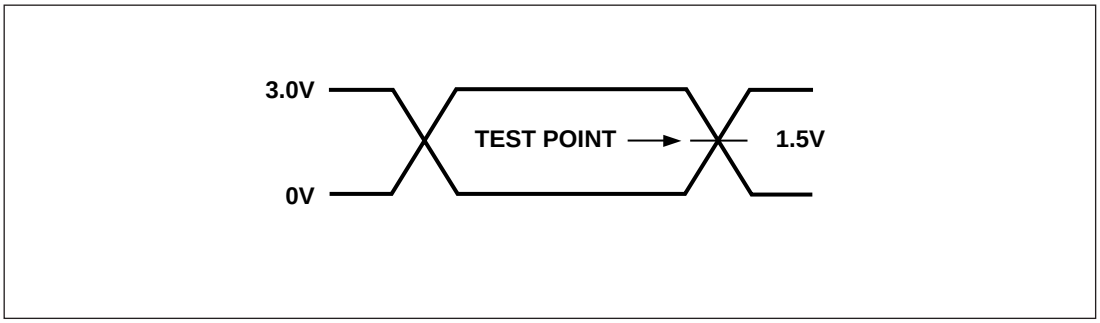
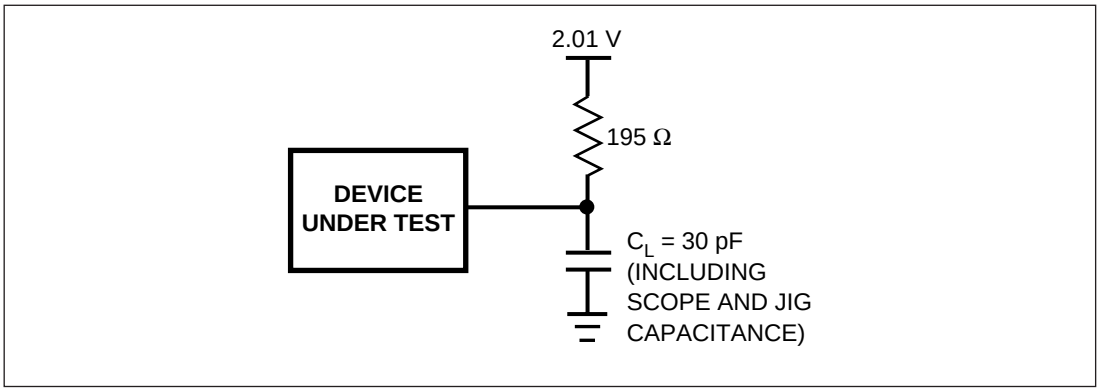


Figure 51. AC Testing Load Circuit



17.0 Erasure and Programming

To clear all locations of their programmed contents, expose the window packaged device to an ultra-violet light source. A dosage of 30 W second/cm^2 is required (40 W second/cm^2 for ZPSD4XXV versions). This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm^2 for 40 to 45 minutes (55 to 60 minutes for ZPSD4XXV versions). The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD4XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from ST, or after each erasure, the PSD4XX device has all bits in the PAD and EPROM in the “1” or high state. The configuration bits are in the “0” or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from ST. Please contact your local sales representative.

18.0 PSD4XX Pin Assignments

Pin No.	68-Pin PLDCC/CLDCC Package	Pin No.	68-Pin PLDCC/CLDCC Package
1	GND	35	GND
2	ADIO_7	36	PE2
3	ADIO_6	37	PE1
4	ADIO_5	38	PE0
5	ADIO_4	39	CSI
6	ADIO_3	40	RESET
7	ADIO_2	41	RD
8	ADIO_1	42	CLKIN
9	ADIO_0	43	PB7
10	PC7	44	PB6
11	PC6	45	PB5
12	PC5	46	PB4
13	PC4	47	PB3
14	PC3	48	PB2
15	PC2	49	PB1
16	PC1	50	PB0
17	PC0	51	GND
18	VCC	52	VCC
19	GND	53	PD7
20	PA7	54	PD6
21	PA6	55	PD5
22	PA5	56	PD4
23	PA4	57	PD3
24	PA3	58	PD2
25	PA2	59	PD1
26	PA1	60	PD0
27	PA0	61	ADIO_15
28	Vstdby	62	ADIO_14
29	WR	63	ADIO_13
30	PE7	64	ADIO_12
31	PE6	65	ADIO_11
32	PE5	66	ADIO_10
33	PE4	67	ADIO_9
34	PE3	68	ADIO_8

PSD4XX Pin Assignments

Pin No.	80-Pin TQFP Package	Pin No.	80-Pin TQFP Package
1	PC7	41	PB7
2	PC6	42	PB6
3	PC5	43	PB5
4	PC4	44	PB4
5	PC3	45	PB3
6	PC2	46	PB2
7	PC1	47	PB1
8	PC0	48	PB0
9	V_{CC}	49	GND
10	V_{CC}	59	GND
11	GND	51	V_{CC}
12	GND	52	V_{CC}
13	PA7	53	PD7
14	PA6	54	PD6
15	PA5	55	PD5
16	PA4	56	PD4
17	PA3	57	PD3
18	PA2	58	PD2
19	PA1	59	PD1
20	PA0	60	PD0
21	NC	61	NC
22	NC	62	ADIO_15
23	Vstdby	63	ADIO_14
24	WR	64	ADIO_13
25	PE7	65	ADIO_12
26	PE6	66	ADIO_11
27	PE5	67	ADIO_10
28	PE4	68	ADIO_9
29	PE3	69	ADIO_8
30	GND	70	GND
31	GND	71	GND
32	PE2	72	ADIO_7
33	PE1	73	ADIO_6
34	PE0	74	ADIO_5
35	CSI	75	ADIO_4
36	RESET	76	ADIO_3
37	RD	77	ADIO_2
38	CLKIN	78	ADIO_1
39	NC	79	ADIO_0
40	NC	80	NC

19.0 Package Information

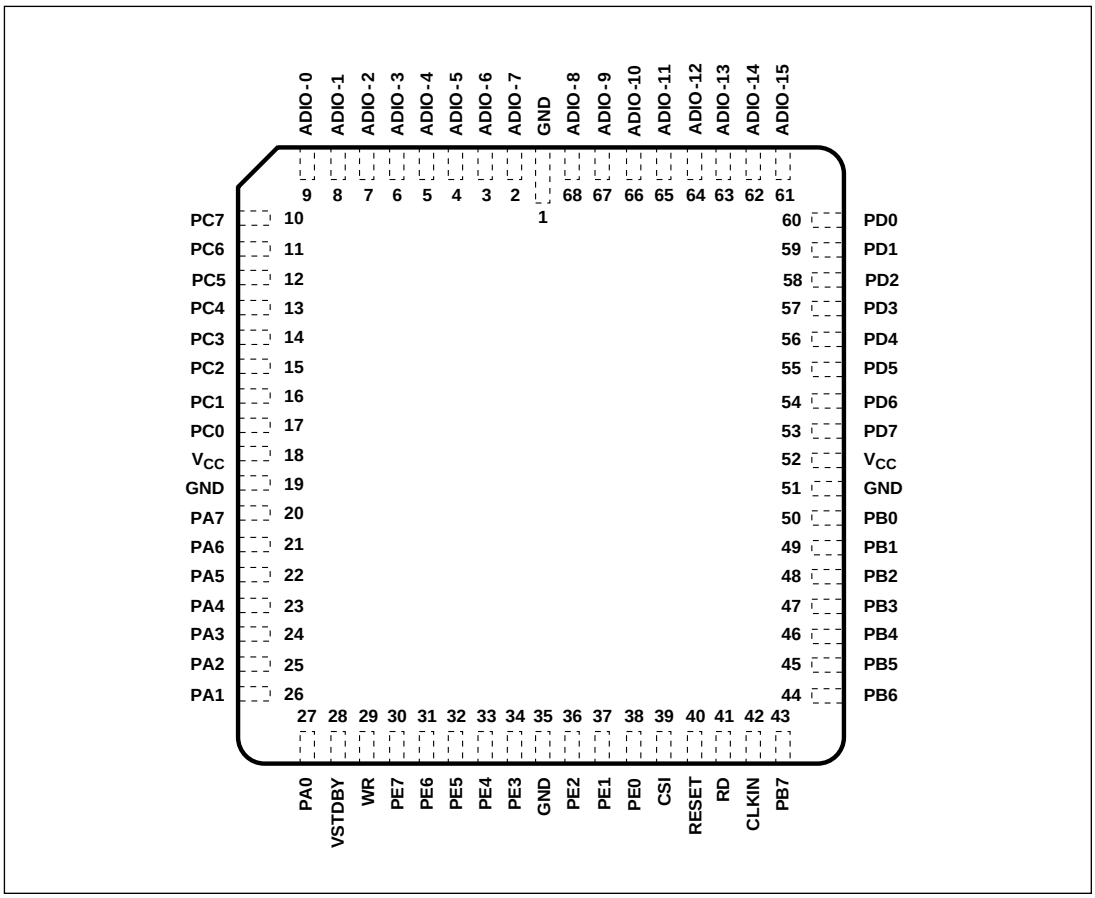


Figure 52. Drawing J5 – 68-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

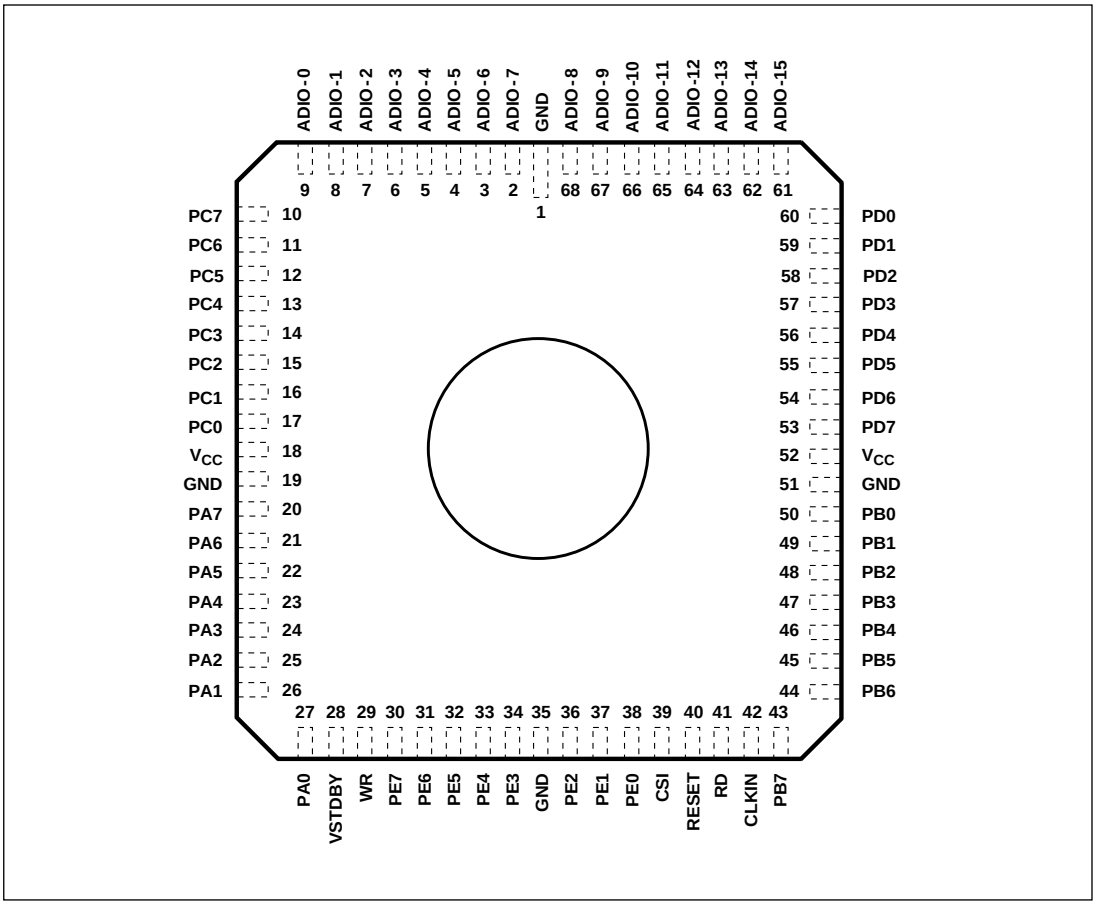
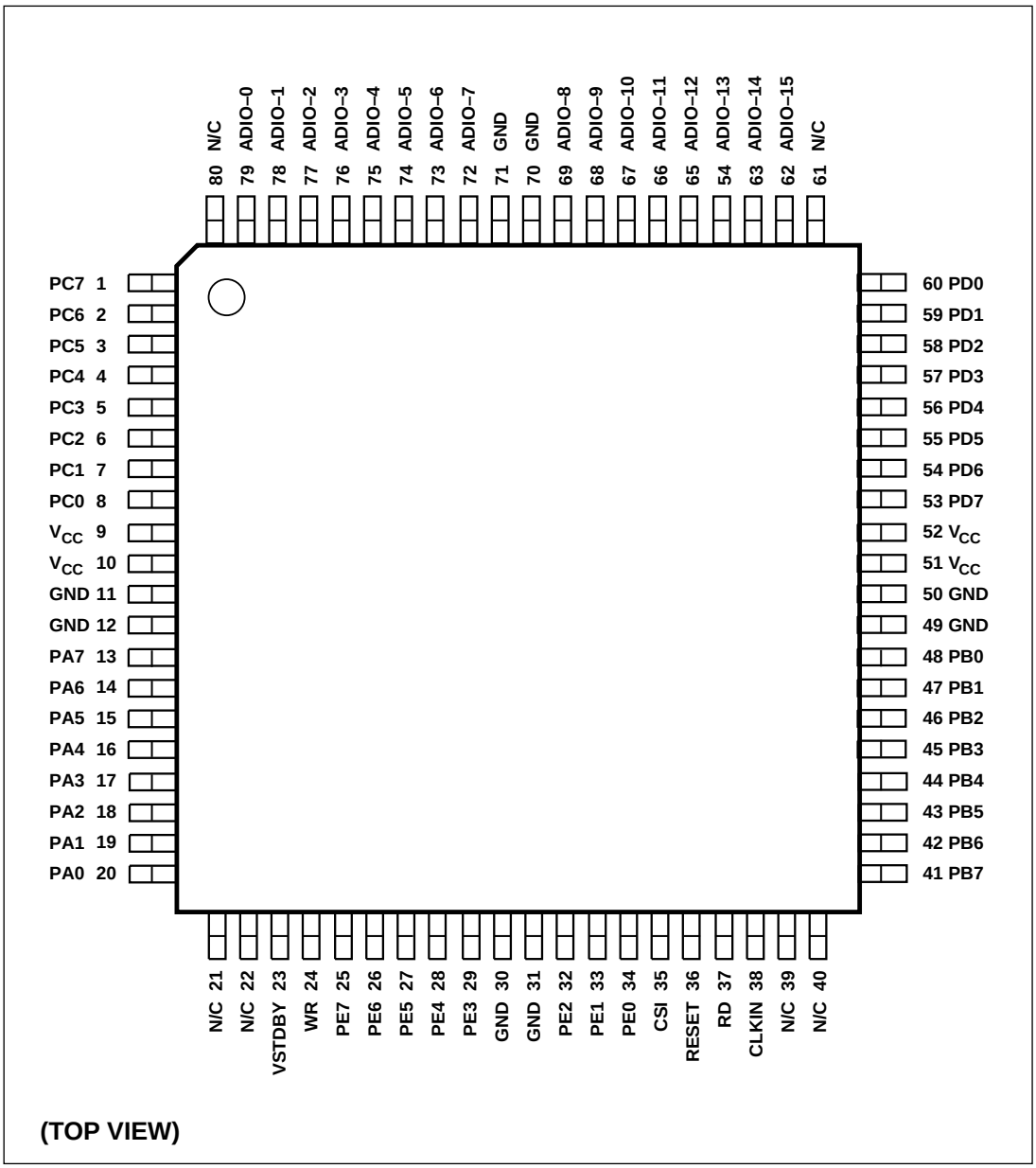
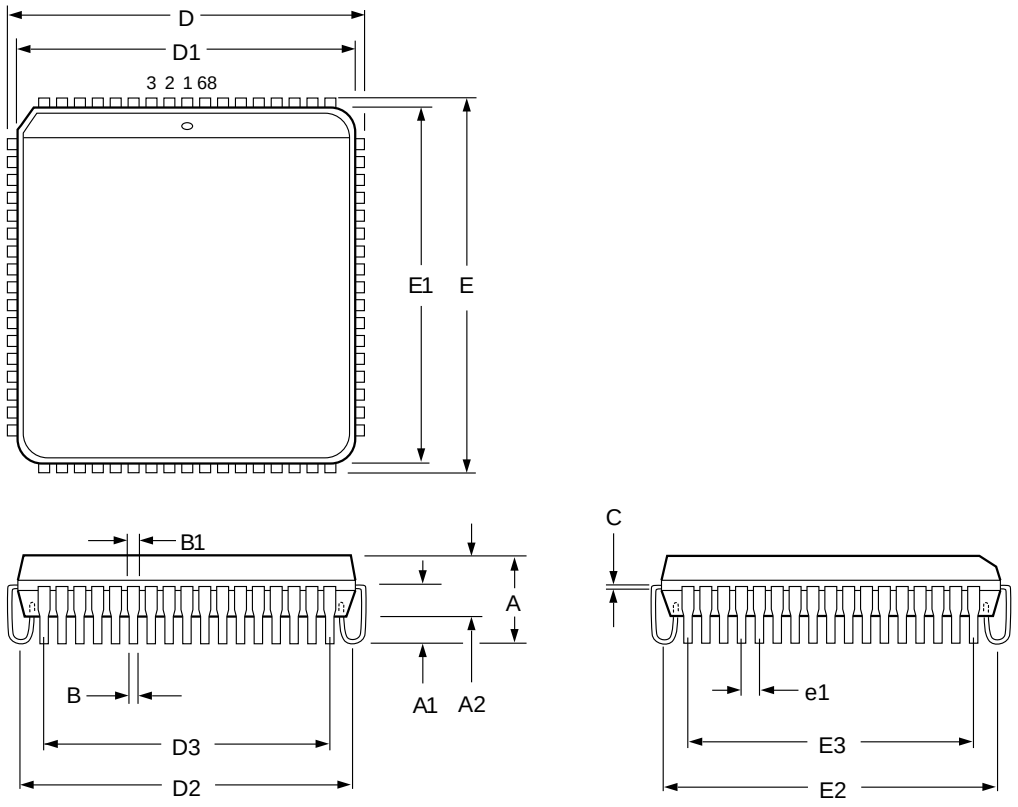


Figure 53. Drawing L5 – 68-Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

Figure 54. Drawing U2 – 80-Pin Plastic Thin Quad Flatpack (TQFP) (Package Type U)



Drawing J5 – 68-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



Family: Plastic Leaded Chip Carrier

	Millimeters			*Inches*		
Symbol	*Min*	*Max*	*Notes*	*Min*	*Max*	*Notes*
A	4.19	4.57		0.165	0.180	
A1	2.41	3.00		0.095	0.118	
A2	3.71	3.91		0.146	0.154	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.196	0.262		0.0077	0.0083	
D	25.02	25.27		0.985	0.995	
D1	24.13	24.23		0.950	0.954	
D2	22.61	23.62		0.890	0.930	
D3	20.32		Reference	0.800		Reference
E	25.02	25.27		0.985	0.995	
E1	24.13	24.23		0.950	0.954	
E2	22.61	23.62		0.890	0.930	
E3	20.32		Reference	0.800		Reference
e1	1.27		Reference	0.050		Reference
N	68			68		

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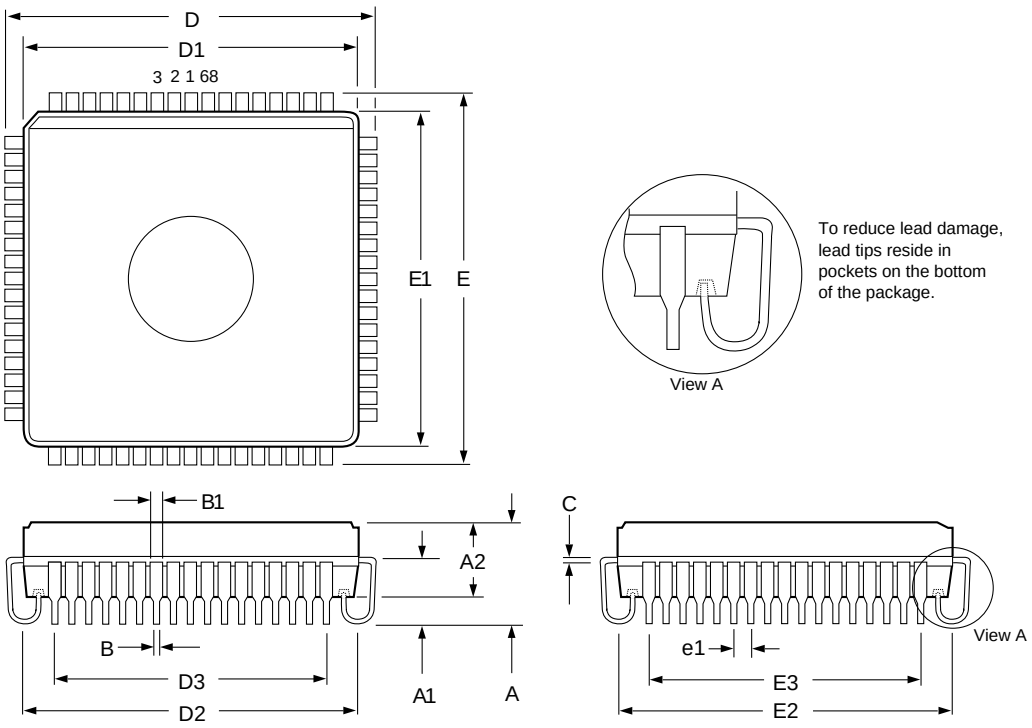
Drawing L5 – 68-Pin Pocketed Ceramic Leaded Chip Carrier (CLDCC) – CERQUAD (Package Type L)



Family: Ceramic Leaded Chip Carrier – CERQUAD

	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.94	4.57		0.155	0.180	
A1	2.29	2.92		0.090	0.115	
A2	3.05	3.68		0.120	0.145	
B	0.43	0.53		0.017	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.15	0.25		0.006	0.010	
D	25.02	25.27		0.985	0.995	
D1	23.93	24.28		0.942	0.956	
D2	22.35	23.88		0.880	0.940	
D3	20.32		Reference	0.800		Reference
E	25.02	25.27		0.985	0.995	
E1	23.93	24.28		0.942	0.956	
E2	22.35	23.88		0.880	0.940	
E3	20.32		Reference	0.800		Reference
e1	1.27		Reference	0.050		Reference
N	68			68		

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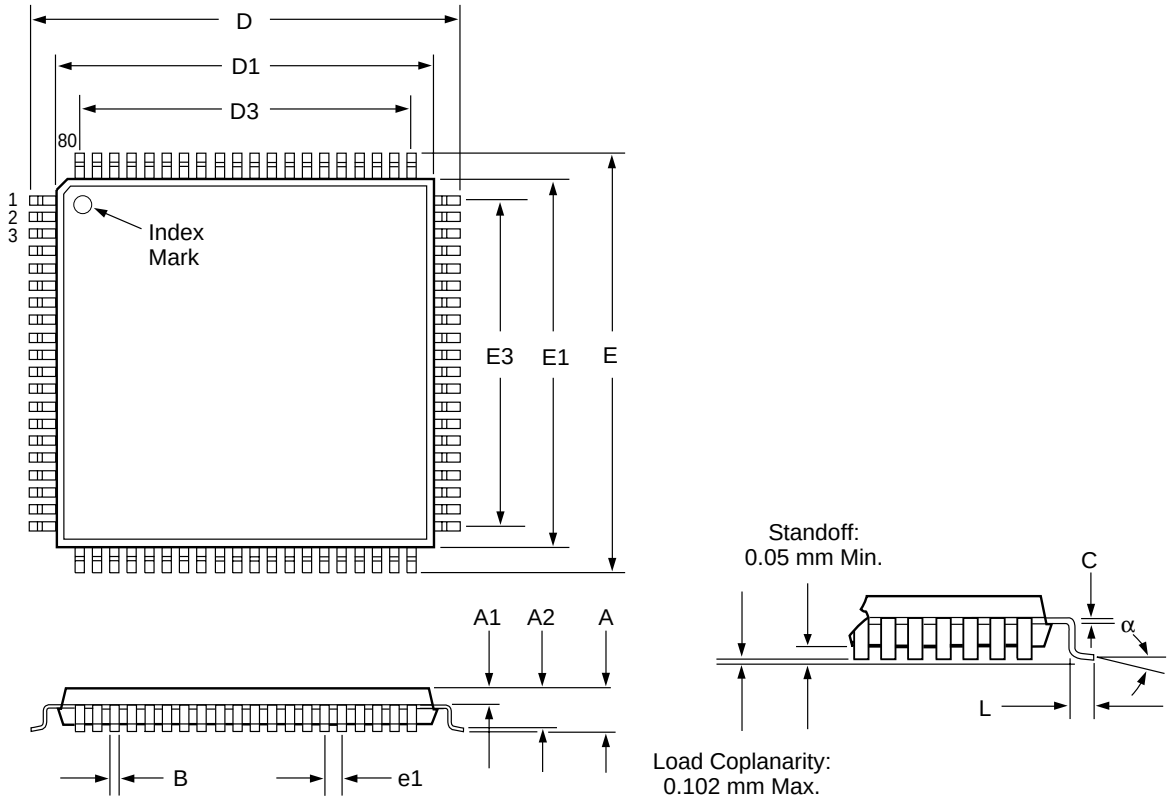
Drawing U2 – 80-Pin Plastic Thin Quad Flatpack (TQFP) (Package Type U)



Family: Plastic Thin Quad Flatpack (TQFP)

	Millimeters			*Inches*		
Symbol	*Min*	*Max*	*Notes*	*Min*	*Max*	*Notes*
α	0°	8°		0°	8°	
A	–	1.60		–	0.063	
A1	0.54	0.74		0.021	0.029	
A2	1.15	1.55		0.045	0.061	
B	0.30		Reference	0.012		Reference
C	0.09	0.20		0.004	0.008	
D	15.75	16.25		0.620	0.640	
D1	13.90	14.10		0.547	0.555	
D3	12.35		Reference	0.486		Reference
E	15.75	16.25		0.620	0.640	
E1	13.90	14.10		0.547	0.555	
E3	12.35		Reference	0.486		Reference
e1	0.65		Reference	0.026		Reference
L	0.35	0.75		0.014	0.030	
N	80			80		

030195R1

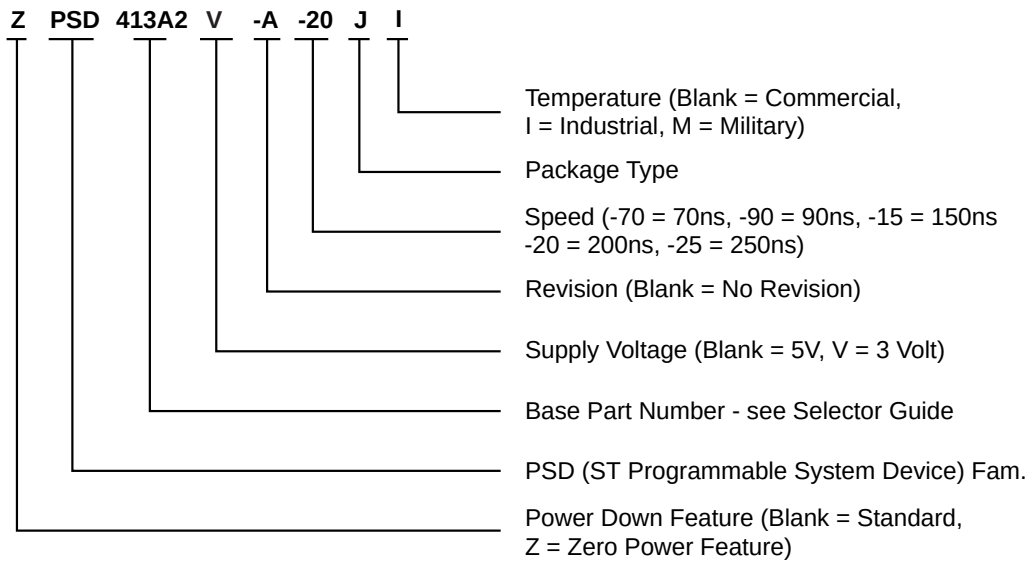
20.0 PSD4XX Product Ordering Information

20.1 PSD4XX Family – Selector Guide

Part #			MCU		PLDs/Decoders						I/O	Memory		Other					
PSD	ZPSD	ZPSDV	Data Path	Interface	Inputs	Product Terms	Input Micro⇔Cells	Output Micro⇔Cells	Outputs	Page Reg.	Ports	EPROM	SRAM (w/BB)	Four 16-Bit Timer/Counters	WatchDog (16-Bit)	Inter. Contr.	Periph. Mode	Security	APD
PSD411A1	ZPSD411A1	ZPSD411A1V	8	PLUS1	37	113		8	16	X	40	256Kb	16Kb				X	X	X
PSD401A1	ZPSD401A1	ZPSD401A1V	16/8	PLUS1	37	113		8	16	X	40	256Kb	16Kb				X	X	X
	ZPSD412A0		8	PLUS1	37	113		8	16	X	40	512Kb	16Kb				X	X	X
PSD412A1	ZPSD412A1	ZPSD412A1V	8	PLUS1	37	113		8	16	X	40	512Kb	16Kb				X	X	X
PSD402A1	ZPSD402A1	ZPSD402A1V	16/8	PLUS1	37	113		8	16	X	40	512Kb	16Kb				X	X	X
PSD413A1	ZPSD413A1	ZPSD413A1V	8	PLUS1	37	113		8	16	X	40	1024Kb	16Kb				X	X	X
PSD403A1	ZPSD403A1	ZPSD403A1V	16/8	PLUS1	37	113		8	16	X	40	1024Kb	16Kb				X	X	X
PSD411A2	ZPSD411A2	ZPSD411A2V	8	PLUS1	59	126		24	24	X	40	256Kb	16Kb				X	X	X
PSD401A2	ZPSD401A2	ZPSD401A2V	16/8	PLUS1	59	126		24	24	X	40	256Kb	16Kb				X	X	X
PSD412A2	ZPSD412A2	ZPSD412A2V	8	PLUS1	59	126		24	24	X	40	512Kb	16Kb				X	X	X
PSD402A2	ZPSD402A2	ZPSD402A2V	16/8	PLUS1	59	126		24	24	X	40	512Kb	16Kb				X	X	X
PSD413A2	ZPSD413A2	ZPSD413A2V	8	PLUS1	59	126		24	24	X	40	1024Kb	16Kb				X	X	X
PSD403A2	ZPSD403A2	ZPSD403A2V	16/8	PLUS1	59	126		24	24	X	40	1024Kb	16Kb				X	X	X

PSD4XX Product Ordering Information (cont.)

20.2 Part Number Construction



20.3 Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
PSD401A1-C-70J	70	68 Pin PLDCC	Comm'l
PSD401A1-C-70L	70	68 Pin CLDCC	Comm'l
PSD401A1-C-70U	70	68 Pin TQFP	Comm'l
PSD401A1-C-90JI	90	68 Pin PLDCC	Industrial
PSD401A1-C-90UI	90	68 Pin TQFP	Industrial
PSD401A1-C-12J	120	68 Pin PLDCC	Comm'l
PSD401A1-C-15J	150	68 Pin PLDCC	Comm'l
PSD401A1-C-15L	150	68 Pin CLDCC	Comm'l
PSD401A1-C-15U	150	68 Pin TQFP	Comm'l
PSD401A2-C-70J	70	68 Pin PLDCC	Comm'l
PSD401A2-C-70L	70	68 Pin CLDCC	Comm'l
PSD401A2-C-70U	70	68 Pin TQFP	Comm'l
PSD401A2-C-90JI	90	68 Pin PLDCC	Industrial
PSD401A2-C-90UI	90	68 Pin TQFP	Industrial
PSD401A2-C-15J	150	68 Pin PLDCC	Comm'l
PSD401A2-C-15L	150	68 Pin CLDCC	Comm'l
PSD401A2-C-15U	150	68 Pin TQFP	Comm'l

PSD4XX Product Ordering Information (cont.)

Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
PSD402A1-C-70J	70	68 Pin PLDCC	Comm'l
PSD402A1-C-70L	70	68 Pin CLDCC	Comm'l
PSD402A1-C-70U	70	68 Pin TQFP	Comm'l
PSD402A1-C-90JI	90	68 Pin PLDCC	Industrial
PSD402A1-C-90UI	90	68 Pin TQFP	Industrial
PSD402A1-C-15J	150	68 Pin PLDCC	Comm'l
PSD402A1-C-15L	150	68 Pin CLDCC	Comm'l
PSD402A1-C-15U	150	68 Pin TQFP	Comm'l
PSD402A2-C-70J	70	68 Pin PLDCC	Comm'l
PSD402A2-C-70L	70	68 Pin CLDCC	Comm'l
PSD402A2-C-70U	70	68 Pin TQFP	Comm'l
PSD402A2-C-90JI	90	68 Pin PLDCC	Industrial
PSD402A2-C-90UI	90	68 Pin TQFP	Industrial
PSD402A2-C-15J	150	68 Pin PLDCC	Comm'l
PSD402A2-C-15L	150	68 Pin CLDCC	Comm'l
PSD402A2-C-15U	150	68 Pin TQFP	Comm'l
PSD403A1-C-70J	70	68 Pin PLDCC	Comm'l
PSD403A1-C-70L	70	68 Pin CLDCC	Comm'l
PSD403A1-C-70U	70	68 Pin TQFP	Comm'l
PSD403A1-C-90JI	90	68 Pin PLDCC	Industrial
PSD403A1-C-90UI	90	68 Pin TQFP	Industrial
PSD403A1-C-15J	150	68 Pin PLDCC	Comm'l
PSD403A1-C-15L	150	68 Pin CLDCC	Comm'l
PSD403A1-C-15U	150	68 Pin TQFP	Comm'l
PSD403A2-C-70J	70	68 Pin PLDCC	Comm'l
PSD403A2-C-70L	70	68 Pin CLDCC	Comm'l
PSD403A2-C-70U	70	68 Pin TQFP	Comm'l
PSD403A2-C-90JI	90	68 Pin PLDCC	Industrial
PSD403A2-C-90UI	90	68 Pin TQFP	Industrial
PSD403A2-C-15J	150	68 Pin PLDCC	Comm'l
PSD403A2-C-15L	150	68 Pin CLDCC	Comm'l
PSD403A2-C-15U	150	68 Pin TQFP	Comm'l
PSD411A1-C-70J	70	68 Pin PLDCC	Comm'l
PSD411A1-C-70L	70	68 Pin CLDCC	Comm'l
PSD411A1-C-70U	70	68 Pin TQFP	Comm'l
PSD411A1-C-90JI	90	68 Pin PLDCC	Industrial
PSD411A1-C-90UI	90	68 Pin TQFP	Industrial
PSD411A1-C-15J	150	68 Pin PLDCC	Comm'l
PSD411A1-C-15L	150	68 Pin CLDCC	Comm'l
PSD411A1-C-15U	150	68 Pin TQFP	Comm'l

PSD4XX Product Ordering Information (cont.)

Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
PSD411A2-C-70J	70	68 Pin PLDCC	Comm'l
PSD411A2-C-70L	70	68 Pin CLDCC	Comm'l
PSD411A2-C-70U	70	68 Pin TQFP	Comm'l
PSD411A2-C-90JI	90	68 Pin PLDCC	Industrial
PSD411A2-C-90UI	90	68 Pin TQFP	Industrial
PSD411A2-C-15J	150	68 Pin PLDCC	Comm'l
PSD411A2-C-15L	150	68 Pin CLDCC	Comm'l
PSD411A2-C-15U	150	68 Pin TQFP	Comm'l
PSD412A1-C-70J	70	68 Pin PLDCC	Comm'l
PSD412A1-C-70L	70	68 Pin CLDCC	Comm'l
PSD412A1-C-70U	70	68 Pin TQFP	Comm'l
PSD412A1-C-90JI	90	68 Pin PLDCC	Industrial
PSD412A1-C-90UI	90	68 Pin TQFP	Industrial
PSD412A1-C-15J	150	68 Pin PLDCC	Comm'l
PSD412A1-C-15L	150	68 Pin CLDCC	Comm'l
PSD412A1-C-15U	150	68 Pin TQFP	Comm'l
PSD412A2-C-70J	70	68 Pin PLDCC	Comm'l
PSD412A2-C-70L	70	68 Pin CLDCC	Comm'l
PSD412A2-C-70U	70	68 Pin TQFP	Comm'l
PSD412A2-C-90JI	90	68 Pin PLDCC	Industrial
PSD412A2-C-90UI	90	68 Pin TQFP	Industrial
PSD412A2-C-15J	150	68 Pin PLDCC	Comm'l
PSD412A2-C-15L	150	68 Pin CLDCC	Comm'l
PSD412A2-C-15U	150	68 Pin TQFP	Comm'l
PSD413A1-C-70J	70	68 Pin PLDCC	Comm'l
PSD413A1-C-70L	70	68 Pin CLDCC	Comm'l
PSD413A1-C-70U	70	68 Pin TQFP	Comm'l
PSD413A1-C-90JI	90	68 Pin PLDCC	Industrial
PSD413A1-C-90UI	90	68 Pin TQFP	Industrial
PSD413A1-C-15J	150	68 Pin PLDCC	Comm'l
PSD413A1-C-15L	150	68 Pin CLDCC	Comm'l
PSD413A1-C-15U	150	68 Pin TQFP	Comm'l
PSD413A2-C-70J	70	68 Pin PLDCC	Comm'l
PSD413A2-C-70L	70	68 Pin CLDCC	Comm'l
PSD413A2-C-70U	70	68 Pin TQFP	Comm'l
PSD413A2-C-90JI	90	68 Pin PLDCC	Industrial
PSD413A2-C-90UI	90	68 Pin TQFP	Industrial
PSD413A2-C-15J	150	68 Pin PLDCC	Comm'l
PSD413A2-C-15L	150	68 Pin CLDCC	Comm'l
PSD413A2-C-15U	150	68 Pin TQFP	Comm'l

PSD4XX Product Ordering Information (cont.)

Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
ZPSD401A1-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD401A1-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD401A1-C-70U	70	80 Pin TQFP	Comm'l
ZPSD401A1-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD401A1-C-90UI	90	80 Pin TQFP	Industrial
ZPSD401A1-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD401A1-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD401A1-C-15U	150	80 Pin TQFP	Comm'l
ZPSD401A1V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD401A1V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD401A1V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD401A1V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD401A1V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD401A1V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD401A1V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD401A1V-C-25U	250	80 Pin TQFP	Comm'l
ZPSD401A2-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD401A2-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD401A2-C-70U	70	80 Pin TQFP	Comm'l
ZPSD401A2-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD401A2-C-90UI	90	80 Pin TQFP	Industrial
ZPSD401A2-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD401A2-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD401A2-C-15U	150	80 Pin TQFP	Comm'l
ZPSD401A2V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD401A2V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD401A2V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD401A2V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD401A2V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD401A2V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD401A2V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD401A2V-C-25U	250	80 Pin TQFP	Comm'l
ZPSD402A1-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD402A1-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD402A1-C-70U	70	80 Pin TQFP	Comm'l
ZPSD402A1-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD402A1-C-90UI	90	80 Pin TQFP	Industrial
ZPSD402A1-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD402A1-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD402A1-C-15U	150	80 Pin TQFP	Comm'l

PSD4XX Product Ordering Information (cont.)

Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
ZPSD402A1V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD402A1V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD402A1V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD402A1V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD402A1V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD402A1V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD402A1V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD402A1V-C-25U	250	80 Pin TQFP	Comm'l
ZPSD402A2-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD402A2-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD402A2-C-70U	70	80 Pin TQFP	Comm'l
ZPSD402A2-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD402A2-C-90UI	90	80 Pin TQFP	Industrial
ZPSD402A2-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD402A2-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD402A2-C-15U	150	80 Pin TQFP	Comm'l
ZPSD402A2V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD402A2V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD402A2V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD402A2V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD402A2V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD402A2V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD402A2V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD402A2V-C-25U	250	80 Pin TQFP	Comm'l
ZPSD403A1-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD403A1-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD403A1-C-70U	70	80 Pin TQFP	Comm'l
ZPSD403A1-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD403A1-C-90UI	90	80 Pin TQFP	Industrial
ZPSD403A1-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD403A1-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD403A1-C-15U	150	80 Pin TQFP	Comm'l
ZPSD403A1V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD403A1V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD403A1V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD403A1V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD403A1V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD403A1V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD403A1V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD403A1V-C-25U	250	80 Pin TQFP	Comm'l

PSD4XX Product Ordering Information (cont.)

Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
ZPSD403A2-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD403A2-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD403A2-C-70U	70	80 Pin TQFP	Comm'l
ZPSD403A2-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD403A2-C-90LI	90	68 Pin CLDCC	Industrial
ZPSD403A2-C-90UI	90	80 Pin TQFP	Industrial
ZPSD403A2-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD403A2-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD403A2-C-15U	150	80 Pin TQFP	Comm'l
ZPSD403A2V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD403A2V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD403A2V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD403A2V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD403A2V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD403A2V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD403A2V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD403A2V-C-25U	250	80 Pin TQFP	Comm'l
ZPSD411A1-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD411A1-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD411A1-C-70U	70	80 Pin TQFP	Comm'l
ZPSD411A1-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD411A1-C-90UI	90	80 Pin TQFP	Industrial
ZPSD411A1-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD411A1-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD411A1-C-15U	150	80 Pin TQFP	Comm'l
ZPSD411A1V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD411A1V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD411A1V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD411A1V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD411A1V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD411A1V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD411A1V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD411A1V-C-25U	250	80 Pin TQFP	Comm'l
ZPSD411A2-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD411A2-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD411A2-C-70U	70	80 Pin TQFP	Comm'l
ZPSD411A2-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD411A2-C-90UI	90	80 Pin TQFP	Industrial
ZPSD411A2-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD411A2-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD411A2-C-15U	150	80 Pin TQFP	Comm'l

PSD4XX Product Ordering Information (cont.)

Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
ZPSD411A2V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD411A2V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD411A2V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD411A2V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD411A2V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD411A2V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD411A2V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD411A2V-C-25U	250	80 Pin TQFP	Comm'l
ZPSD412A0-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD412A0-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD412A0-C-70U	70	80 Pin TQFP	Comm'l
ZPSD412A0-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD412A0-C-90UI	90	80 Pin TQFP	Industrial
ZPSD412A0-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD412A0-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD412A0-C-15U	150	80 Pin TQFP	Comm'l
ZPSD412A1-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD412A1-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD412A1-C-70U	70	80 Pin TQFP	Comm'l
ZPSD412A1-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD412A1-C-90UI	90	80 Pin TQFP	Industrial
ZPSD412A1-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD412A1-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD412A1-C-15U	150	80 Pin TQFP	Comm'l
ZPSD412A1V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD412A1V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD412A1V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD412A1V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD412A1V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD412A1V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD412A1V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD412A1V-C-25U	250	80 Pin TQFP	Comm'l
ZPSD412A2-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD412A2-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD412A2-C-70U	70	80 Pin TQFP	Comm'l
ZPSD412A2-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD412A2-C-90UI	90	80 Pin TQFP	Industrial
ZPSD412A2-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD412A2-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD412A2-C-15U	150	80 Pin TQFP	Comm'l

PSD4XX Product Ordering Information (cont.)

Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
ZPSD412A2V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD412A2V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD412A2V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD412A2V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD412A2V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD412A2V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD412A2V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD412A2V-C-25U	250	80 Pin TQFP	Comm'l
ZPSD413A1-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD413A1-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD413A1-C-70U	70	80 Pin TQFP	Comm'l
ZPSD413A1-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD413A1-C-90UI	90	80 Pin TQFP	Industrial
ZPSD413A1-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD413A1-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD413A1-C-15U	150	80 Pin TQFP	Comm'l
ZPSD413A1V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD413A1V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD413A1V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD413A1V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD413A1V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD413A1V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD413A1V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD413A1V-C-25U	250	80 Pin TQFP	Comm'l
ZPSD413A2-C-70J	70	68 Pin PLDCC	Comm'l
ZPSD413A2-C-70L	70	68 Pin CLDCC	Comm'l
ZPSD413A2-C-70U	70	80 Pin TQFP	Comm'l
ZPSD413A2-C-90JI	90	68 Pin PLDCC	Industrial
ZPSD413A2-C-90UI	90	80 Pin TQFP	Industrial
ZPSD413A2-C-15J	150	68 Pin PLDCC	Comm'l
ZPSD413A2-C-15L	150	68 Pin CLDCC	Comm'l
ZPSD413A2-C-15U	150	80 Pin TQFP	Comm'l
ZPSD413A2V-C-20J	200	68 Pin PLDCC	Comm'l
ZPSD413A2V-C-20JI	200	68 Pin PLDCC	Industrial
ZPSD413A2V-C-20L	200	68 Pin CLDCC	Comm'l
ZPSD413A2V-C-20U	200	80 Pin TQFP	Comm'l
ZPSD413A2V-C-20UI	200	80 Pin TQFP	Industrial
ZPSD413A2V-C-25J	250	68 Pin PLDCC	Comm'l
ZPSD413A2V-C-25L	250	68 Pin CLDCC	Comm'l
ZPSD413A2V-C-25U	250	80 Pin TQFP	Comm'l

REVISION HISTORY

Table 1. Document Revision History

Date	Rev.	Description of Revision
Jul-1993	1.0	PSD4XX: Document written in the WSI format. Initial release
Mar-1997	1.1	ZPSD4XX: Updated Specifications
May-1998	1.2	PSD4XX Updated Specifications, -12 Speed Grade Removed
Feb-1999	1.3	February, 1999 PSD4XXR, ZPSD4XXR Combined Data Sheets, Eliminated military parts, Eliminated various speed grades, Updated Specifications.
31-Jan-2002	1.4	PSD4XX, ZPSD4XX: Low Cost Field Programmable Microcontroller Peripherals Front page, and back two pages, in ST format, added to the PDF file Any references to Waferscale, WSI, EasyFLASH and PSDsoft 2000 updated to ST, ST, Flash+PSD and PSDsoft Express

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