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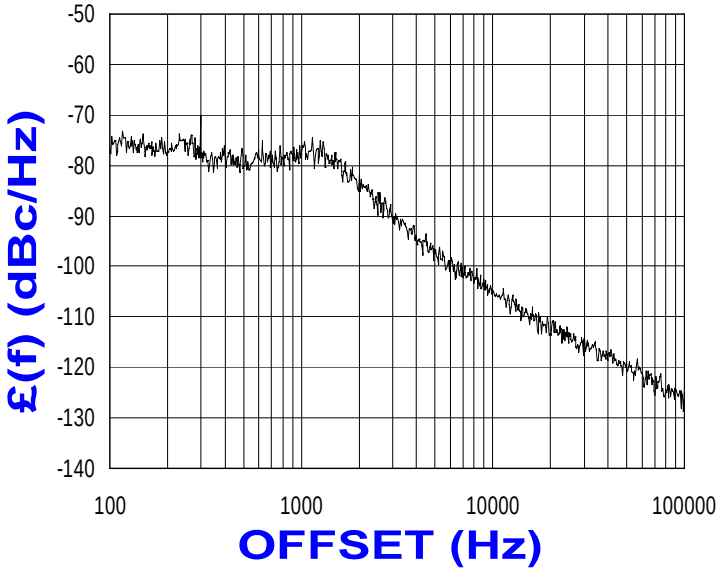
PSA1780A

PHASE LOCKED LOOP

Rev A1



PHASE NOISE (1 Hz BW, typical)



FEATURES

- Frequency Range: 1780 - 1840 MHz
- Step Size: 50 KHz
- PLL-24 - Style Package

APPLICATIONS

- Telecommunications
- Satellite
- Telemetry

PERFORMANCE SPECIFICATIONS	VALUE	UNITS
Frequency Range	1780 - 1840	MHz
Phase Noise @ 10 kHz offset (1 Hz BW, typ.)	-106	dBc/Hz
Harmonic Suppression (2nd, typ.)	-15	dBc
Sideband Spurs (typ.)	-65	dBc
Power Output	3±2	dBm
Load Impedance	50	Ω
Step Size	50	kHz
Charge Pump Output Current	3.13	µA
Switching Speed (typ., adjacent channel)	5.5	mSec
Startup Lock Time (typ.)	5	mSec
Operating Temperature Range	-40 to 85	°C
Package Style	PLL-24	
POWER SUPPLY REQUIREMENTS		
Supply Voltage (Vcc, nom.)	5	Vdc
Supply Current (Icc, typ.)	40	mA

All specifications are typical unless otherwise noted and subject to change without notice.

APPLICATION NOTES

- AN-107 : How to Solder Z-COMM VCOs / PLLs
- AN-202 : PLL Functional Description

NOTES:

Reference Oscillator Signal: 5 MHz<f_{osc}<100 MHz

Frequency Synthesizer: National Semiconductor - ADF4106

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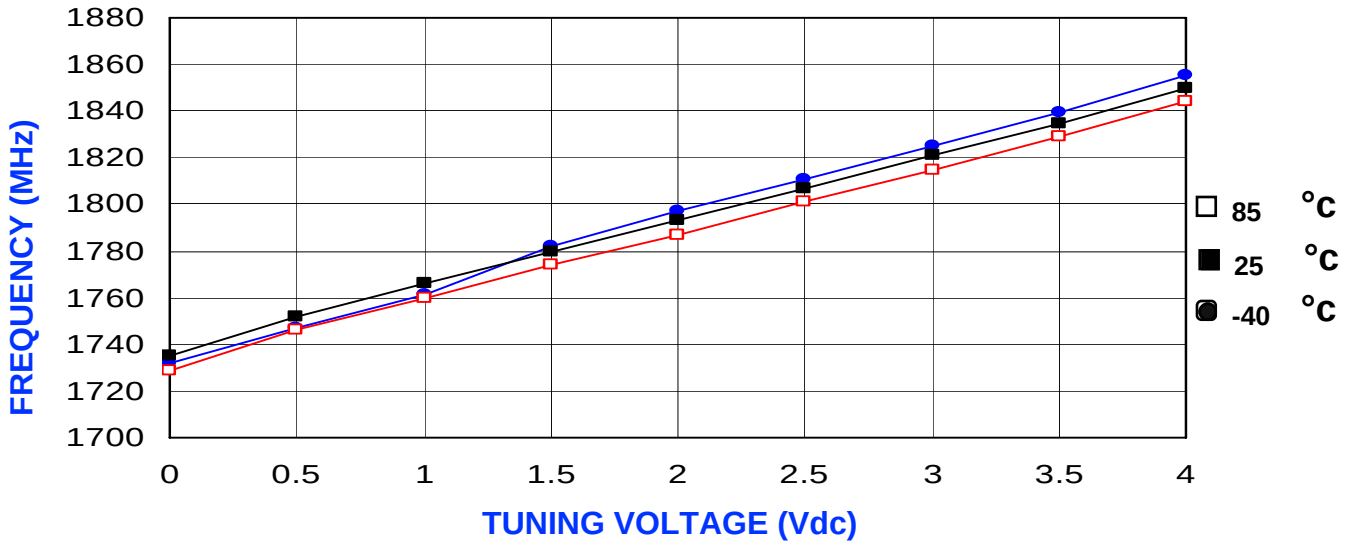
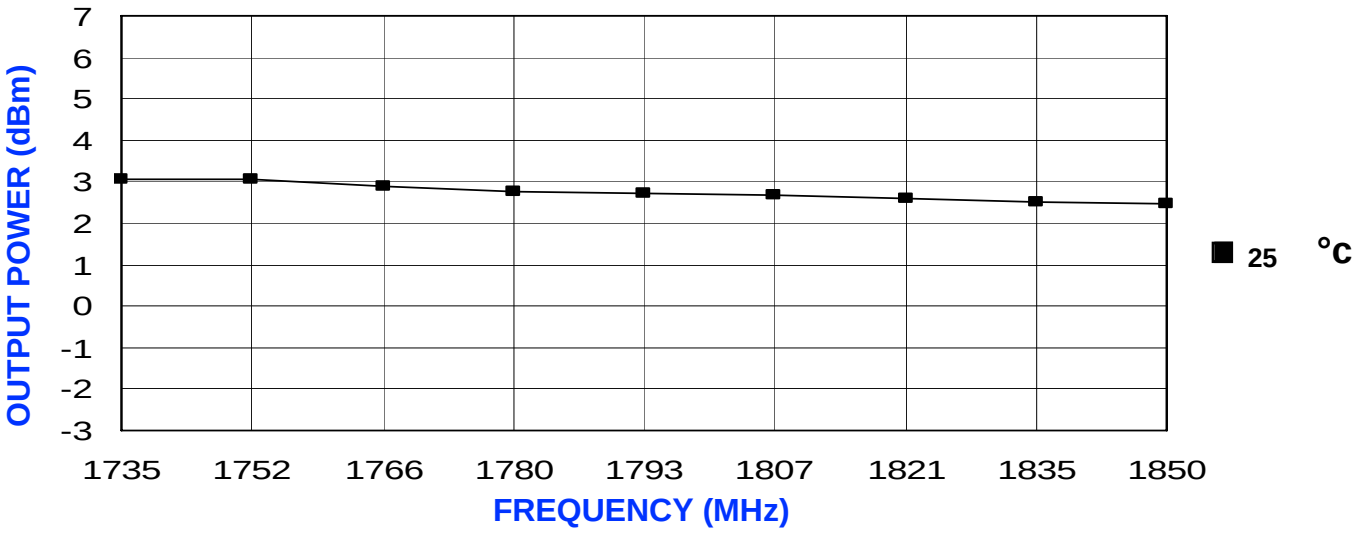
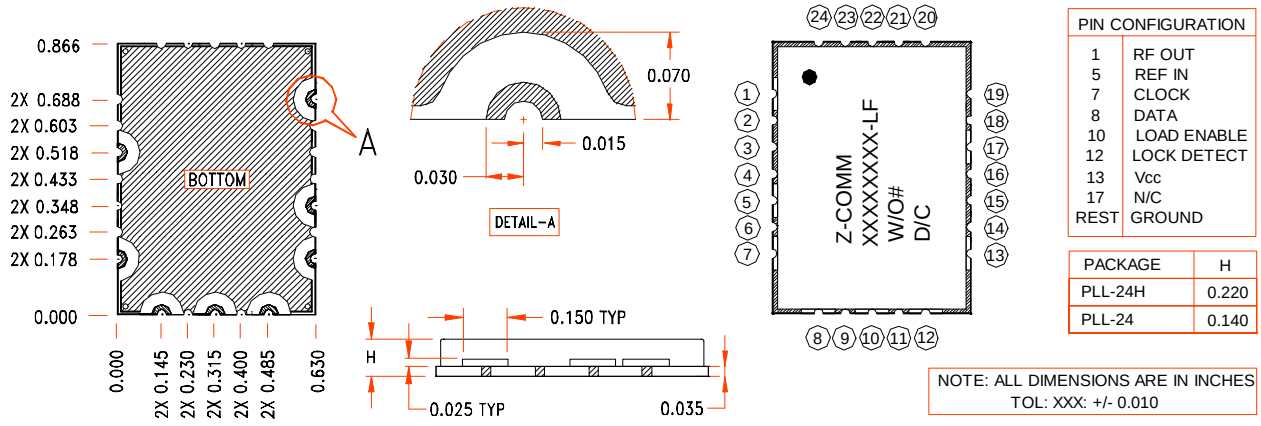
VCO TUNING CURVE, typ.



VCO POWER CURVE, typ.



PHYSICAL DIMENSIONS



PIN CONFIGURATION	
1	RF OUT
5	REF IN
7	CLOCK
8	DATA
10	LOAD ENABLE
12	LOCK DETECT
13	Vcc
17	N/C
REST	GROUND

PACKAGE	H
PLL-24H	0.220
PLL-24	0.140

NOTE: ALL DIMENSIONS ARE IN INCHES
TOL: XXX: +/- 0.010

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