Dimmable LED Driver

Features

- Compatible with
  - Leading edge dimmers
  - Trailing edge dimmers
  - Two wire digital dimmers
- Suited for isolated and nonisolated configurations
  - Flyback with dual winding transformer
  - Buck-boost with single winding inductor
- Features simple open loop controls
  - Fixed line voltage design (100/120/230V)
  - Mimics incandescent bulb behavior
  - Constant frequency, constant duty switching
  - Discontinuous current mode
  - High power factor operation
  - No frequency compensation required
  - Switches at 67 kHz
  - Resistor programmed duty / ON time
  - Duty adjusts for line voltage variation
  - Duty adjusts for inductance variation
  - LED power regulation accuracy of ± 2%
  - LED current accuracy ± 4% (typ)
  - LED current line regulation ± 3% (typ)

Applications

- General Lighting
- Dimmable Light Fixtures
- Dimmable Bulb/Tube Replacement

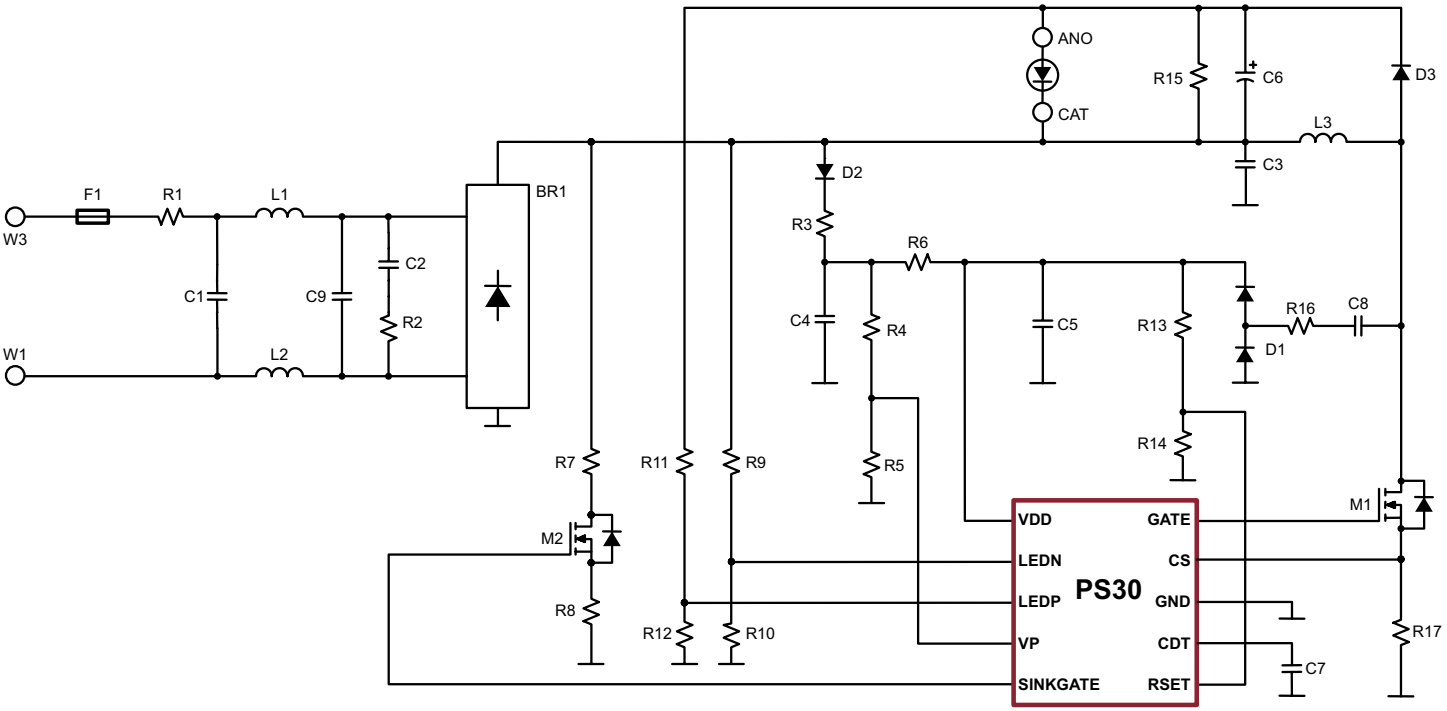
General Description

The PS30 LED driver IC provides the control functions required for a dimmable LED driver targeting LED bulbs, tubes, and similar lighting application.

The IC operates either a non-isolated buck-boost or an isolated buck-boost (flyback) topology in the discontinuous conduction mode using constant switching frequency and constant duty. Such operation of the buck-boost topology results in high power factor operation. The input which is provided to the LED load can be adjusted by choice of the switch duty and the inductance of the main magnetic component. The IC changes switch duty to compensate for line voltage variation and inductance variation of the main magnetic component.

The PS30 LED driver is compatible with all types of dimmers, including leading edge dimmers, trailing edge dimmers, and two wire dimmers with microprocessor controls. A second switch introduces additional line current draw where needed to stabilize the line current waveform and the operation of the dimmer.

Typical Application Circuit

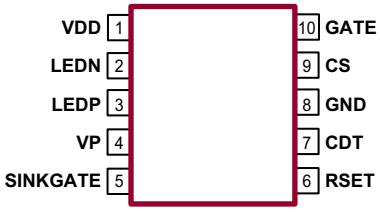


Ordering Information

Part Number	Package	Packing
PS30MG-G	10-lead MSOP	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Pin Configuration



10-lead MSOP
(top view)

Absolute Maximum Ratings

Parameter	Value
Average current into V_{DD}	10mA
Voltage applied to any pin	-0.3V to +12V
Current applied to VP, RSET, CDT, CS, SINKGATE, LEDN, LEDP, GATE	±1.0mA
Continuous power dissipation *(T_A = 25°C)*	400mW
Junction temperature	-40°C to +150°C
Storage ambient temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Package Marking

Top Marking



Bottom Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

10-lead MSOP

Typical Thermal Resistance

Package	θ_{ja}
10-lead MSOP	171°C/W

Electrical Characteristics

(V_{DD} sourced from 12V through 1.0kΩ with 0.1µF bypass V_{DD} to gnd unless noted otherwise, C_{dt} = 10nF)

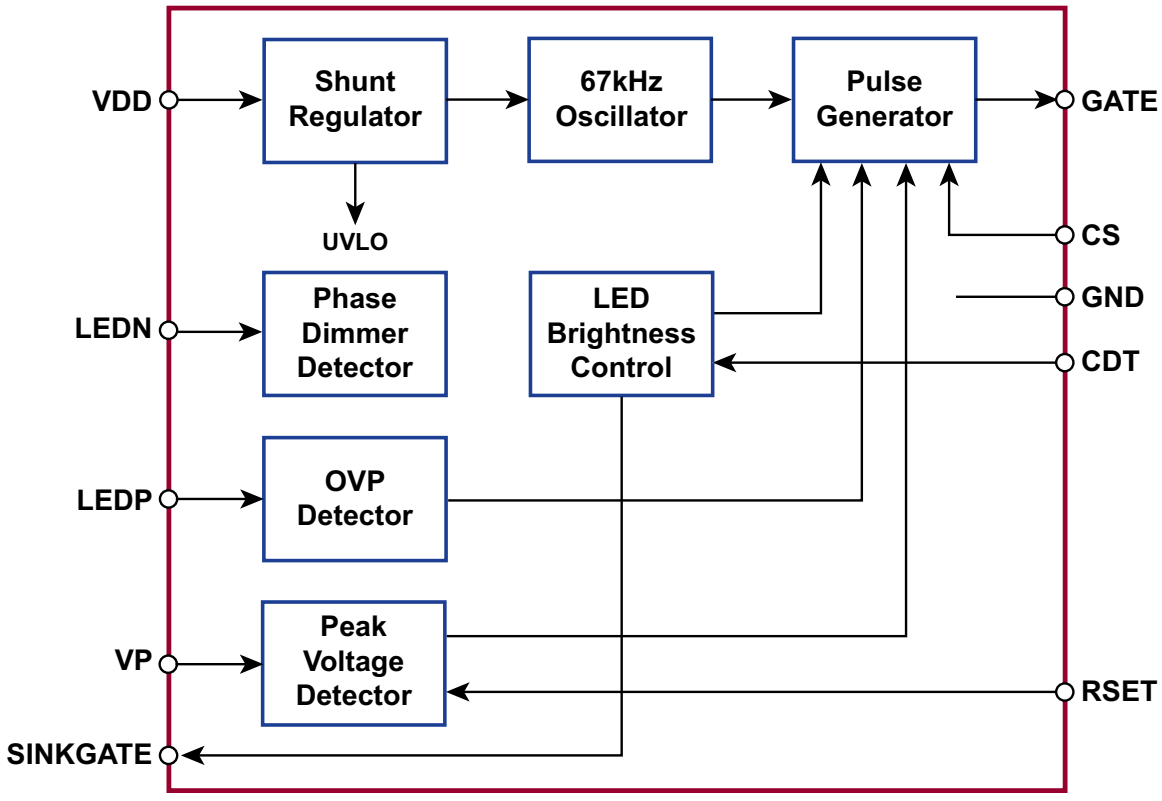
Sym	Parameter	Min	Typ	Max	Unit	Conditions
Input						
V_{DD}	Internal shunt regulator output	9.0	10	11	V	---
I_{START}	V_{DD} starting current	-	38	60	µA	V_{DD} = 7V
I_{DD}	V_{DD} running current	-	500	-	µA	V_{DD} = 9V, output running, no load
Gate Driver						
Freq	Output frequency	60	67	75	kHz	---
PW	Output pulse width PW	-	4.70	-	µs	---
$V_{GATE(LOW)}$	Gate drive Low level	0	0.02	0.10	V	No load
$V_{GATE(HIGH)}$	Gate drive High level	V_{DD} -0.2	V_{DD} -0.5	V_{DD}	V	No load
t_{RISE}	V_{GATE} rise time, 10 to 90%	-	30	55	ns	C_{GATE} = 1nF
t_{FALL}	V_{GATE} fall time, 90 to 10%	-	13	25	ns	C_{GATE} = 1nF
Line Voltage Compensation						
V_{RSET}	RSET voltage for VP nominal	4.00	4.25	4.50	V	V_P = 4.25V

Electrical Characteristics *(cont.)*

(V_{DD} sourced from 12V through 1.0kΩ with 0.1µF bypass V_{DD} to gnd unless noted otherwise, C_{dt} = 10nF)

Sym	Parameter	Min	Typ	Max	Unit	Conditions
Over Voltage Protection						
I_{LEDN}	LEDN input current	-	0	-	µA	LEDN input voltage = 1.0V
V_{LEDP} - V_{LEDN}	Difference at OVP trip point	0.9	1.0	1.1	V	---
I_{LEDP} rising	LEDP current rising threshold	15	17	19	µA	---
I_{LEDP} hysteresis falling	LEDP current falling threshold hysteresis	-5.0	-4.0	-3.0	µA	---
Current Sense						
I_{CS}	CS input current	-	0	-	µA	CS input voltage = 0V
V_{CS_MIN}	CS min voltage for pulsing	30	70	100	mV	---

Block Diagram



General Description

The PS30 is a discontinuous mode constant frequency, constant duty power converter optimized for driving off-line LED replacements for incandescent lamps.

An internal timer measures the time duration of the phase cut caused by in-line dimmers and uses this information to determine the LED operating current. This enables dimming to extinction even though the incoming AC waveform does not completely go away at the minimum brightness dimmer setting.

An auxiliary circuit with a separate high voltage FET provides additional load current for the dimmer to give better dimmer performance and compatibility. This design is compatible with the majority of phase cut dimmer types, both leading edge (LE) and trailing edge (TE) dimmer types.

The device operates from the incoming line power and rectified current provided by a charge pump connected to the high voltage switching node.

A 10V shunt regulator controls the low voltage power to the PS30 circuitry. Careful design of the control circuitry minimizes the supply current drawn when the power converter is not receiving voltage input from the dimmer circuit.

Compensation circuits adjust the output pulse width when the input AC line voltage varies over a limited range to give nearly constant load current without the use of feedback. In addition, a special timing circuit compensates for variation of the value of the power inductor used in the power converter, so that the load current varies a minimal amount for inductor value variation of up to ±10%.

When the circuit detects that a dimmer is not in use, it changes its mode of operation so that the input impedance looks resistive, giving a high power factor for that operating case.

Use of a single flyback power converter stage with a simple inductor minimizes the component count, cost, and printed circuit board size.

Operation Description

Referring to the PS30 block diagram, operation begins with the V_{DD} being regulated by a shunt regulator. When the voltage supplied to the VDD pin increases from zero due to external current charging the bypass capacitor on the VDD pin, the voltage has to increase to the regulation point of 10V before the chip will begin operation. During this time the chip draws less than 60 microamperes so that the current can rapidly charge the bypass capacitor. When the regulation point is reached, the chip begins operation, typically drawing 500 microamperes while driving the power switch FET M1.

Operation of the power switch creates current pulses in the inductor L3, with stored energy being transferred to the LED load bypass capacitor C6 through diode D3. At the same time, voltage pulses on one end of capacitor C8 transfer pulses of charge through diode D1 to the bypass capacitor C5 for V_{DD} power to the PS30. The shunt regulator then bypasses excess average current to ground to maintain a voltage at V_{DD} of 10V. Resistor R16 limits the peak current through C8 and D1 to less than 60mA for the value given. Use of too small of a value for R16 will cause excess peak current, and too large of a value will limit current available for use by the PS30.

A 67kHz nominal frequency oscillator serves as the master clock for the power converter. This oscillator's frequency is trimmed at the factory to give the desired power output properties in the application circuit. Output pulses from the oscillator then go to a pulse width timer. The pulse width is generated using a combination of pulse information based on the current flow in the inductor and an internally generated timing ramp. The charging current for the timing ramp is controlled by external resistors to enable setting the operating pulse width and providing compensation for the incoming AC line voltage.

A peak voltage detector using D2 and C4 creates a DC voltage which is representative of the AC line voltage value. This voltage is divided by approximately 40 using R4 and R5 to give the voltage V_P applied to the PS30. When the AC line voltage varies, the voltage V_P will vary in a proportional manner about its nominal value of 3.95V. The resistor R3 is used to limit peak current in D2 during surge conditions. Resistor R6 couples current from the peak voltage detector to the VDD pin of the PS30 to provide operating current during those parts of the AC cycle when there is no input voltage from the AC line. Generally during those times the circuitry in the PS30 is quiescent so its supply current requirements are reduced to less than 200 microamperes.

The voltage at input V_P goes to a peak voltage detector, which generates a current proportional to the value of V_P impressed across an external resistor attached to the RSET pin. Proper choice of R14 will set the desired converter output power and cause it to have minimal sensitivity to the AC line voltage at the nominal input line voltage. Since the power converter load is a string of LEDs with an incrementally steep current vs voltage curve at the operating point, the LED operating current will also be constant as the AC line voltage varies.

The phase dimmer detector is a logic circuit which observes the input waveform to see if the AC line voltage has a phase cut portion, indicating the presence of a dimmer. Most consumer dimmers use leading edge (LE) phase cut with triac devices, but some use trailing edge (TE) phase cut with MOSFET switch devices. The phase dimmer detector

determines whether a dimmer is present, and also whether it is an LE or a TE dimmer. If a dimmer is not present, the power converter operating mode is changed so that it has a resistive input impedance to give a high power factor for the AC input current. When a dimmer is present, the circuit needs to determine the amount of dimmer phase cut and properly control the LED average current by controlling when the power converter operates.

The LED brightness control block is a timing circuit using the external capacitor C7 to measure the proportion of the AC half cycle which is being cut by the in-line phase cut dimmer. If a dimmer is present, the timer measures the amount of time that the dimmer cuts off the AC input, and then computes an amount of time to run the power converter to give the desired LED brightness. For dimmer angle cuts of less than 40 degrees, the power converter runs for all available time, and as the dimmer angle cut increases to 140 degrees, the power converter run time is proportionally reduced to dim the LED to zero brightness. For cut angles of more than 140 degrees, the power converter will not run, and the LED has no current. If the dimmer is a TE dimmer, the angle values are altered to compensate for the additional AC input pulse width caused by energy storage in the EMI filter network. Special techniques are used so that the absolute value of C7 is not critical, with 10nF ±10% being suitable for 60Hz operation, and 12nF being a good choice for 50Hz operation. Excessive variation of C7 will cause problems with not being able to dim to extinction at the maximum dimmer phase cut setting.

A problem which occurs with the power converter not running all the time that the AC line voltage is present is that current will not be drawn from the dimmer itself. This can result in the dimmer turning off prematurely in the case of LE dimmers which use triacs, causing flickering and other brightness control problems. Prevention of this problem is done by the auxiliary current sink circuit using M2. This circuit is turned on whenever the AC line voltage is present, but the power converter is not being operated. Resistor R8 limits the current in the switch at high line voltages, and resistor R7 helps to reduce the dissipation of transistor M2. An alternative construction would be to use a higher value power resistor for R7 and omit R8, so that M2 would operate more as a switch. The design as shown gives better compatibility with the majority of dimmers. M2 must be mounted so that it can dissipate up to 1.5 Watts of heat.

Overvoltage protection is performed by a comparator which measures samples of the voltage on each end of the LED string. Matched resistor dividers using R9 through R12 divide the voltages by 40 to the inputs LEDN and LEDP. A differential voltage threshold is created by 17µA of current drawn by the LEDP pin, and an internal comparator with an input voltage threshold of 1.0V. The sum of these two effects creates a nominal 120V over voltage threshold for protection of the LED string and C6 from over voltage conditions. When an excess differential voltage is detected across C6, the power converter is prevented from operating. Hysteresis in the 17µA current creates a typical voltage hysteresis in the OVP detector of about 20V. If the LED string becomes disconnected or open, the OVP circuit will cause the voltage on C6 to have a sawtooth oscillation between the trip points of 120V and 100V, and the circuit is protected against destruction of C6 or other parts.

Component choice

Input fuse and rectifier

The input AC line goes first to a safety fuse so that any component failure in the lamp will not result in an overheating situation with resultant safety concerns. The line voltage is then converted to full wave rectified DC by a small bridge rectifier. If the best operating reliability is desired in environments where there are surge events, the input to the bridge rectifier should be shunted by an MOV transient suppressor.

EMI filter

In the 120V application circuit, the components R1, R2, L1, L2, C1, and C2 constitute an EMI filter with additional characteristics for good operation of LE dimmers. Resistor R1 introduces loss to damp out ringing of the LC noise filter present in most triac dimmers, and together with C1, C2, and R2, produces current impulses which cause the triac in the dimmer to latch in a conducting state without oscillating. L1 and L2 prevent flow of high frequency noise to the incoming AC line in conjunction with C1 and C3. Other values or arrangements may be chosen for these components, but these have been found to give the best compatibility.

In a 230V system, the capacitor values will need to be reduced and the inductors increased in value. Capacitor C3 provides the instantaneous current drawn by the power converter inductor L3 during operation.

Peak rectifier and OVP

Diode D2 can be any general purposes diode with a breakdown voltage of 400V or more for 120V operation. Resistors R4, R9, and R11 are chosen to be high values to minimize overall power loss in the power converter. R5 is equal to R4 divided by 39 to make a ratio of 40 voltage divider, and likewise R10 and R12 are equal to R9 and R11 divided by 39. These divider resistors are all 1% tolerance to give best current setting and OVP accuracy.

V_{DD} and LED circuits

The V_{DD} decoupling capacitor C5 bypassing VDD to ground is a 1µF capacitor because of the large current pulses drawn by the gate driver for the power converter FET M1. The value of 220kΩ for R6 gives adequate current for operation of the PS30 during the quiescent times when the phase dimmer cut

angle is occurring, so that the voltage on VDD holds up for even large dimmer cut angles.

Capacitor C6 across the LEDs smooths out the current pulses from the power converter, so that when no dimmer is in use, the typical peak to peak current ripple of the LEDs is approximately 40% of the average current value. Ripple amplitude is strongly affected by the LED characteristics. C6 can be reduced if greater ripple is acceptable, and increased to reduce ripple. Note that if C6 is too small, the voltage ripple across C6 may cause the OVP circuit to trigger, interrupting operation of the power converter. R15 is provided so that the voltage on C6 will discharge quickly when the incoming AC line is turned off. If R15 is omitted, virtually all of the charge stored in capacitor C6 will have to discharge through the LEDs, and the light will be observed in a dark room to glow for a long time. Use of R15 will cause the LEDs to extinguish within a few seconds. In addition, R15 provides a minimum load on the power converter, so that the LEDs can extinguish in some cases where there may still be a small amount of energy being transferred by the inductor due to the MOSFET switching slowly. This prevents occasional random flashes when the dimmer is supposed to be at a minimum brightness value.

Power converter

In a 120V system D3 needs to be a fast recovery diode with adequate high voltage breakdown of 500V minimum. To achieve the best efficiency, switching FET M1 needs to have an ON-resistance of 8Ω or less for a power level of 6.5W, and a typical breakdown voltage of 500V. Use of a MOSFET which is too large will cause problems with low efficiency due to energy lost charging device capacitance, and one which is too small will cause low efficiency due to resistive power loss during the conduction times. A number of devices of suitable size are available, the part number cited was chosen due to its common availability. Any equivalent device may be used.

Resistor R13 improves the output current regulation. The value of R13 is experimentally determined. Resistor R14 controls the gate pulse width. The PS30 is trimmed to work with an R14 value of 1.13MΩ.

Gate resistor R17 in conjunction with inductor L3 sets the output power capability. The values given are for 120V and 6.5W of DC output. The nominal values of R17 and L3 are inversely proportional to the output power. L3 needs to be high quality, with a saturation current proportional to the power and at least 700mA for the 6.5W power level. R17 is chosen to be a 1% tolerance resistor since it sets the converter peak current, and therefore the output power. R17 could be made up of two resistors in parallel for convenient power setting. Although the circuit tolerates variation of L3 well, the nominal value should be chosen according to the criteria above.

The charge pump capacitor C8 value of 100pF given is adequate to provide a V_{DD} current of 1.8mA for the PS30 when the power converter is running. This will power the gate drive of the size of MOSFET used here, but if MOSFETs with a larger C_{GS} are used, C8 should be proportionally increased in size. If C8 is too small, the V_{DD} voltage will be observed to fail to regulate at 10V when the power converter is running. All dimmer cut angles must be checked for this situation.

Sink circuit

The current sink circuit uses M2 in conjunction with R7 and R8. The arrangement here gives a value of sink current limited to 80mA when the voltage on the top end of R7 is more than about 16V. In that case, the power dissipated in the circuit for large instantaneous AC voltage inputs is mostly dissipated in M2. The average power in M2 can be as much as 1.5W depending on the dimmer cut angle. R7 also helps to prevent high frequency parasitic oscillations in M2 in some cases.

The limit value of the current is set by $(V_{DD} – V_{TN})/R8$, where V_{TN} is the threshold voltage of M2. In this demo circuit, the same devices are used for M1 and M2 as a convenience, although their requirements are different. M2 does not have to handle large currents or have low R_{ON}, but it must be able to dissipate the power required.

Equations for 120V:

$R4 / R5 = R9 / R10 = R11 / R12 = 39$

$R6 <= ((VAC \cdot 1.34) – 10) / (240\mu A)$

$R6 \cdot C4 >= 0.1s$

$R15 = V_{LED} / (I_{LED} \cdot 0.004)$

$R14 = 1.13M\Omega$

$R16 \cdot C8 \sim 500ns$

$L3 = (6.5W / P_{OUT})\ mH$

$$V_{OVP} = \frac{R11 + R12}{R12} + (R11 \cdot 17\mu A)$$

$R17 = (6.5W / P_{OUT})\ \Omega$

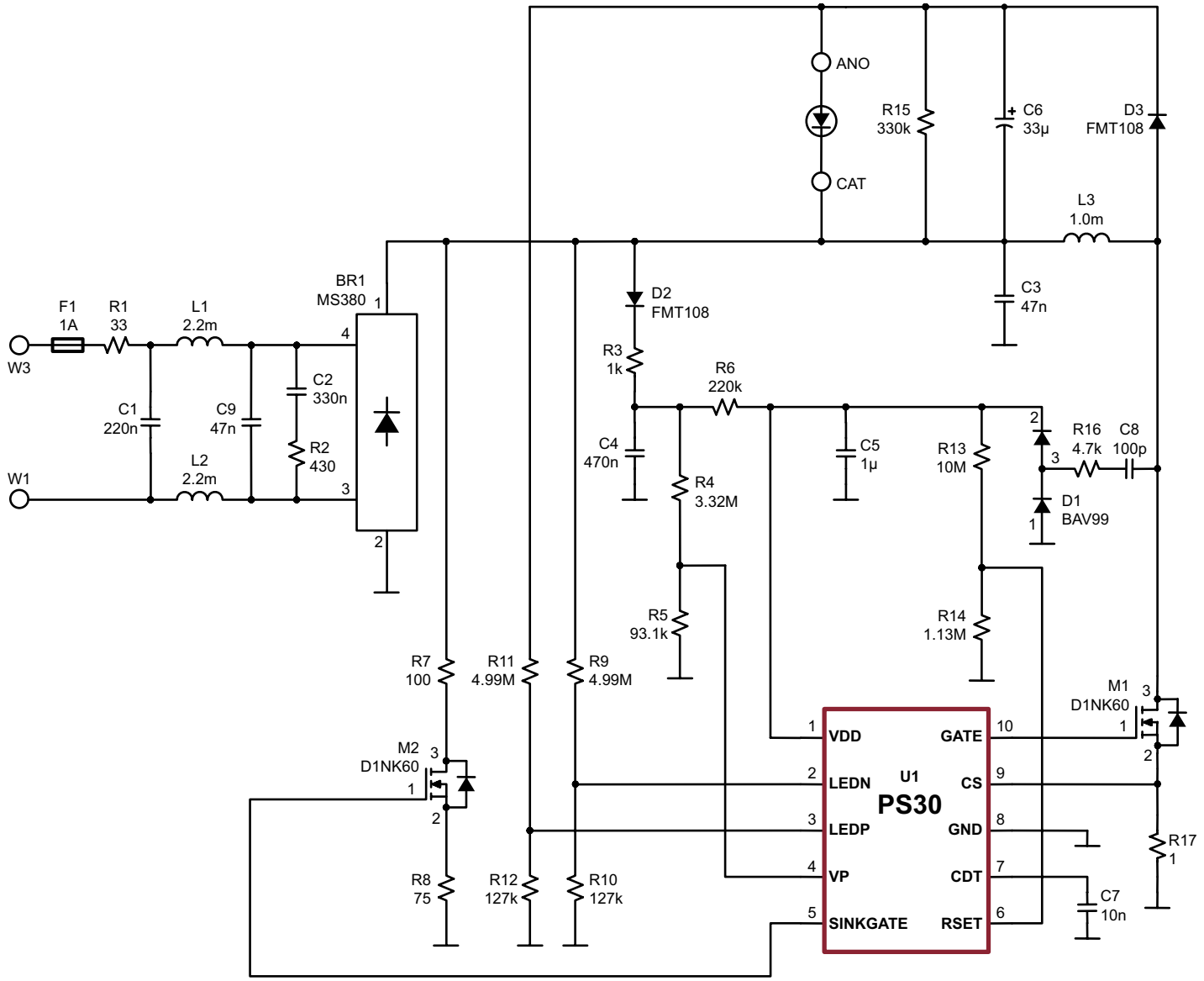
$C7 = (600 / f_{LINE})nF$

$R8 = (V_{DD} – V_{TN}) / I_{SINK}(max)$

$C6 = 33\mu F \cdot (40 / (\%P\text{-}P\ ripple))$

$R13 = 10.0M\Omega$

Typical Application Circuit (Detailed)

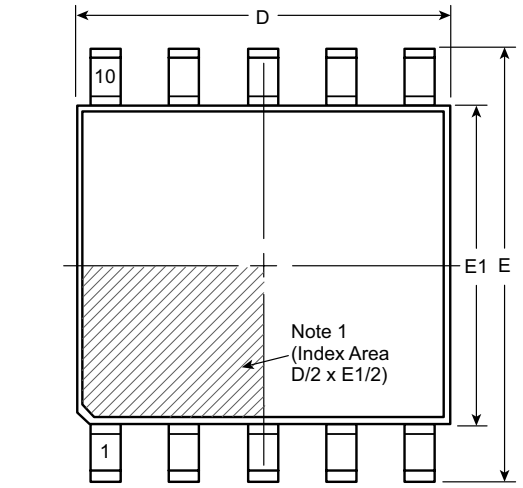


Pin Configuration

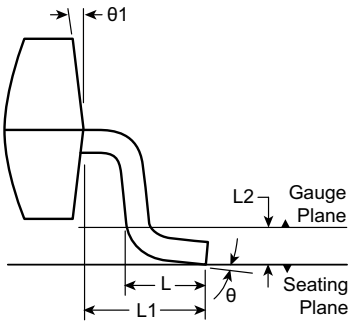
Pin #	Pin Name	Description
1	**VDD**	VDD power input and internal shunt regulator connection
2	**LEDN**	OVP reference from LED load negative side through divider
3	**LEDP**	OVP detection from LED load positive side through divider
4	**VP**	Optional peak voltage detection input
5	**SINKGATE**	Output to control current sink for dimming power control
6	**RSET**	Resistor to ground to set output pulse width and converter output power
7	**CDT**	Capacitor to ground for phase dimmer function timing
8	**GND**	Ground return
9	**CS**	Switch current sense voltage input
10	**GATE**	Switch gate driver output

10-Lead MSOP Package Outline

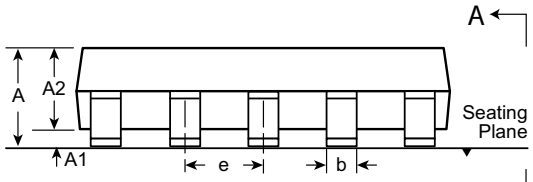
3.00x3.00mm body, 1.10mm height (max), 0.50mm pitch



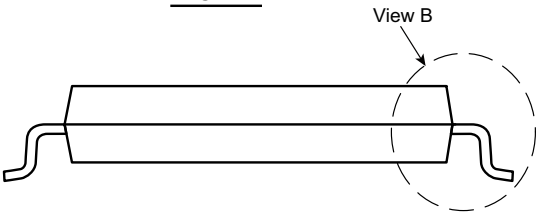
Top View



View B



Side View



View A-A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
Dimen-sion (mm)	MIN	0.75*	0.00	0.75	0.17	2.80*	4.65*	2.80*	0.50 BSC	0.40	0.95 REF	0.25 BSC	0°	5°
	NOM	-	-	0.85	-	3.00	4.90	3.00		0.60			-	-
	MAX	1.10	0.15	0.95	0.33	3.20*	5.15*	3.20*		0.80			8°	15°

JEDEC Registration MO-187, Variation BA, Issue E, Dec. 2004.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-10MSOPMG, Version F041309*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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