PS-AT7909E

revision A

MICROCIRCUIT, DIGITAL, CMOS, MONOLITHIC SILICON

SINGLE CHIP TELEMETRY AND TELECOMMAND

AT7909E

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DOCUMENTATION CHANGE NOTICE

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1 GENERAL

1.1 Scope

This specification details the ratings, physical and electrical characteristics, tests and inspection data of the Single Chip telemetry and Telecommand named AT7909E. It also defines the specific requirement for space and military applications with high reliability.

1.2 Identification

Description	Case	Application
AT7909EKA-MQ	Flat pack 256 leads	Military application
AT7909EKA-SV	Flat pack 256 leads	Space application

1.3 Absolute maximum ratings

Supply voltage range (V_{DD}) ..... -0.5V to 4V dc
Input voltage range (V_{IN}) ..... -0.5V dc to 6V dc
Input current per power pin ..... +/- 60 mA
Input current par signal pin ..... +/- 10 mA
Storage temperature ..... -65°C to 150°C
Maximum junction temperature (T_J) ..... 175°C
Lead temperature (soldering @ 1/16 in, 10 s) ..... 300°C
Thermal resistance junction to case (Rjc) ..... 3.5 K/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}) ..... 3 V dc to 3.6 V dc
Ambient operating temperature (T_A) ..... -55°C to 125°C
Storage temperature ..... 30°C, 20 to 65% RH, dust free, original packing

1.5 Radiation features

Tested up to a total dose (dose rate 0.1 rad/s) ..... 100 kRads (Si)

1.6 Handling precautions

These components are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, shipment and any handling.
ESD..... >4000 V

2 APPLICABLE DOCUMENTS

MIL-PRF-38535 ..... Integrated Circuits, Manufacturing, General Specification for.
MIL-STD-883 ..... Test Method Standard Microcircuits.

In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence.

3 REQUIREMENTS

3.1 Design, construction, and physical dimensions.

The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.1.1 Package type.

The package shall be a flat pack, 256 leads (figure1). The case shall be hermetically sealed and have a ceramic body. Lid shall be connected to ground.

3.1.2 Terminal connections.

The terminal connections shall be as specified on figure 2.

3.1.3 Block diagram.

The block diagram shall be as specified on figure 3.

3.2 Marking

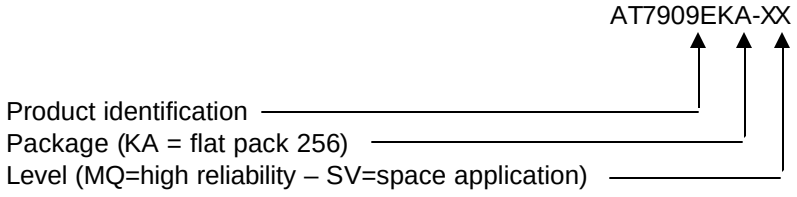
Each component shall be marked in respect of :
(a) Lead Identification
(b) Component Number
(c) Traceability Information
(d) Manufacturer's Component Number

3.2.1 Lead Identification

An index shall be located at the top of the package in the position defined in Figure 1.

3.2.2 Component Number

Each component shall bear the component number which shall be constituted and marked as follows:



3.2.3 Traceability Information

Each component shall be marked in respect of traceability information: lot number and date code.

3.3 Electrical characteristics

The parameters to be measured with respect of electrical characteristics are scheduled in Table 1. The measurements shall be performed at T_{amb}=25 ± 3°C, T_{high}=125 (+0/-5)°C and T_{low} = -55 (+5/-0)°C respectively.

3.4 Burn-in test

3.4.1 Electrical circuit

Circuit for use in performing the power burn-in is shown in figure 4, in accordance with the intent specified in test method 1015 of MIL-STD-883.

3.4.2 Parameters drift value

For space application, the parameter drift values applicable to burn-in are specified in Table 2 of this specification. Unless otherwise stated, measurements shall be performed at + 25 ± 3 ° C. The parameter drift values (Δ), applicable to the parameters scheduled, shall not be exceeded.

In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 1 shall not be exceeded.

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3.5 Environmental and Endurance Tests

3.5.1 Electrical Circuit for Operating LifeTest

The circuit for operating life testing shall be as specified for power burn in (figure 4).

3.5.2 Electrical Measurements at Completion of Environmental and endurance tests

The parameters to be measured are scheduled in Table 1. Unless otherwise stated, the measurements shall be performed at t_{amb} = 25±3°C.

3.5.3 Conditions for Operating LifeTest

The conditions for operating life testing shall be as specified for power burn in.

4 QUALITY ASSURANCE PROVISIONS

4.1 Wafer lot acceptance test

For space application, Wafer Lot Acceptance shall be performed according to mil-std-883 method 5007.

4.2 Sampling and inspection.

Sampling and inspection procedures shall be in accordance with MIL-PRF-38535.

4.3 Screening.

Screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection

- The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in accordance with MIL-PRF-38535.
- Additional screening for space application devices shall be as specified in MIL-PRF-38535, appendix B.

4.4 Quality conformance inspection

Qualification inspection for high reliability and space applications devices shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections.

4.4.1 Group A inspection.

- Tests shall be as specified in table 1 herein.
- Subgroups 5 and 6 of table I of method 5005 of MIL STD 883 shall be omitted.
- Subgroups 7 and 8 of table I of method 5005 of MIL STD 883 shall include verifying the functionality of the device.

- O/V (latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device.
- Capacitance measurement shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failure, and all input and output terminals tested.

4.4.2 Group C inspection.

The group C inspection end-point electrical parameters shall be as specified in table 1 herein.

4.4.3 Group D inspection.

The group D inspection end-point electrical parameters shall be as specified in table 1 herein.

4.5 Delta measurements

Delta measurements, as specified in table 2, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table 2 The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7 and 9.

5 PACKAGING

5.1 Packaging requirements

The requirements for packaging shall be in accordance with MIL-PRF-38535.

TABLE 1. Electrical Parameters

Test	Symbol	Test method Mil-Std-883	Conditions -55°C ≤ T_C ≤ +125°C +3 V ≤ V_{DD} ≤ +3.6 V unless otherwise specified	Limits		Unit
				Min	Max	
High level input voltage	V_{IH}	3013	V_{DD}=3.6V	2.0		V
Low level input voltage	V_{IL}	3013	V_{DD}=3.0V		0.8	V
Threshold Schmitt trigger input voltage	VT+	3013	Note 1	1.40	2.08	V
Threshold Schmitt trigger input voltage	VT-	3013	Note 1	0.99	1.51	V
Hysteresis	V_{HYS}	-	Note 1	0.37		V
High level output voltage	V_{OH}	3006		2.4		V
Low level output voltage	V_{OL}	3007			0.4	V
Low level input current	I_{IL}	3009	V_{in}=GND, V_{DD}=V_{DD}(max)	-1	1	µA
High level input current	I_{IH}	3010	V_{in}=V_{DD}=V_{DD}(max)	-1	1	µA µA
High level input current, pull-down input	I_{IHP}	3010	V_{in}=V_{DD}=V_{DD}(max)	5	70	µA
Output leakage current	I_{OZ}	-	Outputs disabled, GND < V_{out} < V_{DD}	-1	1	µA
Output leakage current, pull-down output	I_{OZHP}	-	Outputs disabled, V_{out} = V_{DD}	5	70	µA
Input pin capacitance	C_{IN}	3012	Note 1		3	pF
I/O pin capacitance	C_{IO}	3012	Note 1		7	pF
Standby supply current for array	I_{DDSBA}	3005	Static mode		4.5	mA
Operating current for array	I_{DDOP}	3005	V_{DD}=3.6V		80	mA
Setup time SpwIfSel to SysClk	Ts1	3003	VDD = 3.6 V Note 2		0	ns
Setup time MemD[15:0] to SysClk MemDcc[5:0] to SysClk	Ts2	3003	VDD = 3.6 V Note 2		0	ns
Propagation Delay SysClk to MemA[23:0]	Tp1	3003	VDD = 3.6 V Note 2		30	ns
Propagation Delay SysClk to MemD[15:0] SysClk to MemDcc[5:0]	Tp2	3003	VDD = 3.6 V Note 2		42	ns

Propagation Delay SysClk to SpwDOut?	Tp3	3003	VDD = 3.6 V Note 2		41	ns
Propagation Delay SysClk to SpwDOut?	Tp4	3003	VDD = 3.6 V Note 2		34	ns
Propagation Delay SysClk to SpwSOut?	Tp5	3003	VDD = 3.6 V Note 2		41	ns
Propagation Delay SysClk to SpwSOut?	Tp6	3003	VDD = 3.6 V Note 2		34	ns
Propagation Delay SysClk to SeqIrq	Tp7	3003	VDD = 3.6 V Note 2		53	ns

Notes :
1/ Guaranteed but not tested
2/ Test conditions: Tester load *80 pF,* VIL = 0V, VIH = VDD, Input signals dynamic characteristics: tr,tf < 10ns, Threshold voltages: VOL = VOH = VDD/2

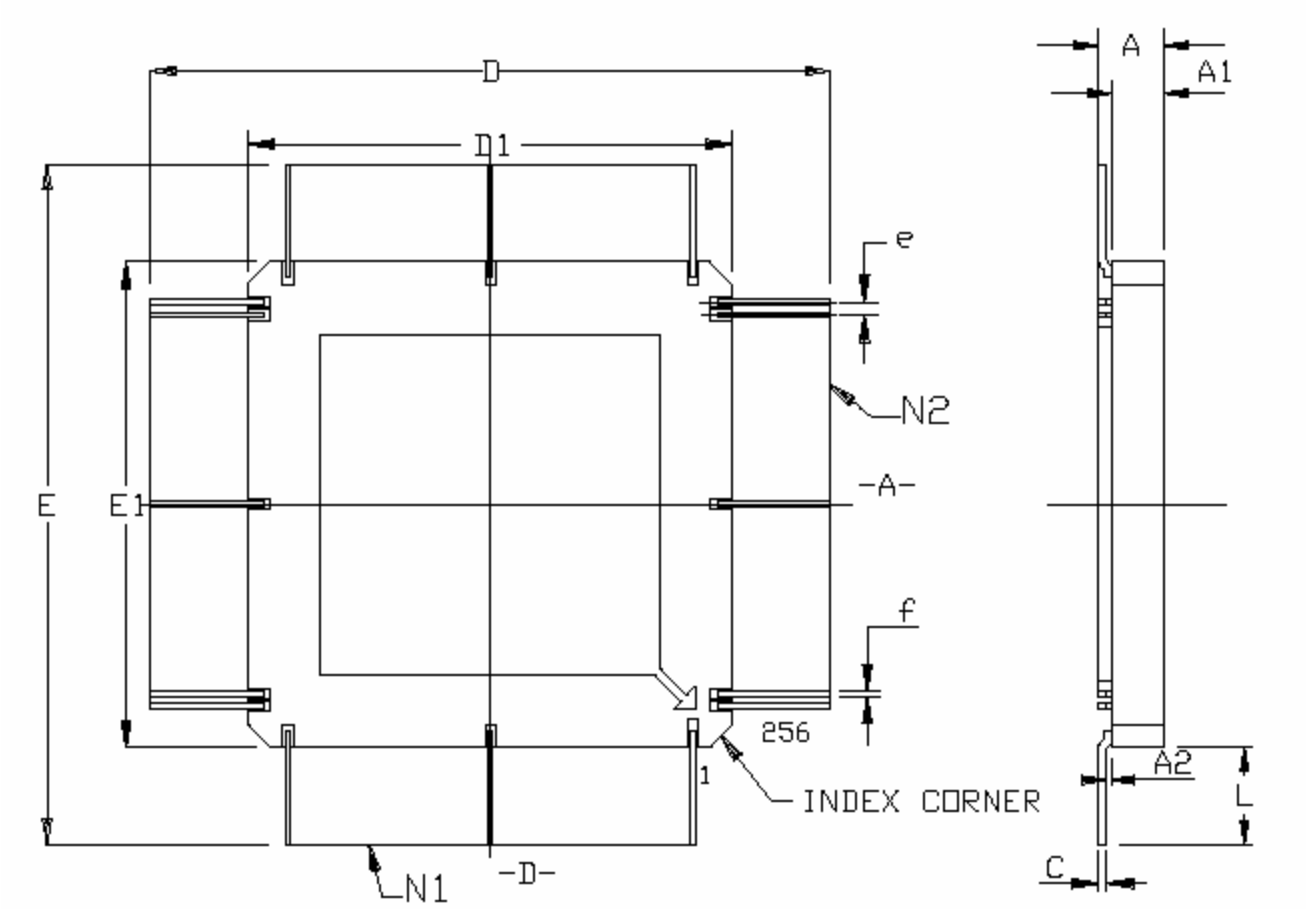
TABLE 2. Parameter drift values

Test	Symbol	Test method Mil-Std-883	Conditions	Drift limits	Unit
Low Level Input Current	IIL	3009	as per Table 1	±0.1	µA
High Level Input Current	IIH	3010	as per Table 1	±0.1	µA
Output Leakage Low Current	IOZL	-	as per Table 1	±0.1	µA
Output Leakage High Current	IOZH	-	as per Table 1	±0.1	µA
Supply Current Stand-by for Array	IDDSBA	3005	as per Table 1	430	µA
Low Level Output Voltage BUF2	VOL	3007	as per Table 1	±100	mV
High Level Output Voltage BUF2	VOH	3006	as per Table 1	±100	mV

Note : the above parameter shall be recorded before and after burn-in and life test to determine the delta.

FIGURE 1. Case outline.

The package is a 256-pin MQFP with 0.02 mil pin spacing and lid connected to ground.



	mm		inch	
A	2.41	3.18	0.095	0.125
A1	2.06	2.56	0.081	0.101
A2	0.05	0.36	0.002	0.014
C	0.10	0.20	0.004	0.008
D/E	53.23	55.74	2.095	2.195
D1/E1	36.83	37.34	1.450	1.470
e	0.508 BSC		0.020 BSC	
f	0.15	0.25	0.006	0.010
L	8.20	9.20	0.323	0.362
N1	64			
N2	64			

FIGURE 2. Terminal connections.

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
1	*Vss[8]*	51	*Vdd[2]*	101	*TestSignalIn[2]*	151	*PdecClcwSamp[0]*
2	*MemD[12]*	52	*MemA[4]*	102	*TestSignalIn[3]*	152	*TmeSIn[E]*
3	*MemD[11]*	53	*MemA[3]*	103	*TmClk1*	153	*PdecClcwClk[0]*
4	*MemD[10]*	54	*MemA[2]*	104	*TmClk2*	154	*TmeSClk[E]*
5	*Vdd[8]*	55	*Vss[1]*	105	*SysClk*	155	*TmeSRdy[E]*
6	*MemD[9]*	56	*MemA[1]*	106	*PoResetN*	156	*TmeSRdy[D]*
7	*Vss[18]*	57	*Vss[19]*	107	*PdecTcIn[5]*	157	*TmeSValid[D]*
8	*Vdd[18]*	58	*Vdd[19]*	108	*PdecTcClk[5]*	158	*TmeSIn[D]*
9	*MemD[8]*	59	*MemA[0]*	109	*PdecTcAct[5]*	159	*TmeSClk[D]*
10	*MemD[7]*	60	*Vdd[1]*	110	*PdecTcIn[4]*	160	*Vss[14]*
11	*MemD[6]*	61	*MemSize16*	111	*PdecTcClk[4]*	161	*TmeSRdy[C]*
12	*MemD[5]*	62	*TestSignalIn[1]*	112	*PdecTcAct[4]*	162	*TmeSValid[C]*
13	*MemD[4]*	63	*TestMode*	113	*PdecTcIn[3]*	163	*TmeSIn[C]*
14	*MemD[3]*	64	*TestSE*	114	*PdecTcClk[3]*	164	*TmeSClk[C]*
15	*Vss[7]*	65	*JtagTdo*	115	*PdecTcAct[3]*	165	*ExtCpduIfAbort*
16	*TestSignalIn[6]*	66	*JtagTdi*	116	*PdecTcIn[2]*	166	*TmeSValid[B]*
17	*MemD[2]*	67	*JtagTms*	117	*PdecTcClk[2]*	167	*ExtCpduIfValid*
18	*MemD[1]*	68	*JtagTRstN*	118	*Vss[15]*	168	*ExtCpduIfRdy*
19	*Vdd[7]*	69	*JtagTck*	119	*PdecTcAct[2]*	169	*ExtCpduIfData*
20	*MemD[0]*	70	*PdecMapGenA[5]*	120	*PdecTcIn[1]*	170	*TmeSIn[B]*
21	*MemCs3N*	71	*Vss[20]*	121	*Vss[21]*	171	*ExtCpduIfClk*
22	*Vss[6]*	72	*Vdd[20]*	122	*Vdd[21]*	172	*TmeSClk[B]*
23	*PdecTcPrior*	73	*PdecMapGenA[4]*	123	*PdecTcClk[1]*	173	*TmeSRdy[B]*
24	*MemCs2N*	74	*PdecMapGenA[3]*	124	*Vdd[15]*	174	*TmeSRdy[A]*
25	*MemCs0N*	75	*PdecMapGenA[2]*	125	*PdecTcAct[1]*	175	*TmeSValid[A]*
26	*Vdd[6]*	76	*PdecMapGenA[1]*	126	*PdecTcIn[0]*	176	*TmeSIn[A]*
27	*MemOEN*	77	*PdecMapGenA[0]*	127	*PdecTcClk[0]*	177	*TmeSClk[A]*
28	*MemWEN*	78	*Vss[17]*	128	*PdecTcAct[0]*	178	*TmeEnable*
29	*Vss[5]*	79	*PdecMapDtr[5]*	129	*PdecClcwD[1]*	179	*Vdd[14]*
30	*MemA[19]*	80	*PdecMapDsr[5]*	130	*PdecClcwSamp[1]*	180	*TmeTimeStrb*
31	*MemA[18]*	81	*PdecMapDtr[4]*	131	*PdecClcwClk[1]*	181	*TmeUnEncSync*
32	*Vdd[5]*	82	*PdecMapDsr[4]*	132	*PdecMapSwitch*	182	*TmeUnEncClk*
33	*MemA[17]*	83	*Vdd[17]*	133	*TmeSValid[H]*	183	*Vss[13]*
34	*MemA[16]*	84	*PdecMapDtr[3]*	134	*PdecAuEnable*	184	*TmeUnEncOut*
35	*Vss[4]*	85	*PdecMapDsr[3]*	135	*Vss[22]*	185	*Vss[23]*
36	*MemA[15]*	86	*PdecMapDtr[2]*	136	*Vdd[22]*	186	*Vdd[23]*
37	*MemA[14]*	87	*PdecMapDsr[2]*	137	*TmeSIn[H]*	187	*Vdd[13]*
38	*Vdd[4]*	88	*PdecMapDtr[1]*	138	*TmeSClk[H]*	188	*TmeEncOut*
39	*MemA[13]*	89	*PdecMapDsr[1]*	139	*TmeSRdy[H]*	189	*TmeEncClk*
40	*MemA[12]*	90	*PdecMapDtrG*	140	*TmeSValid[G]*	190	*TmeEncIOut*
41	*MemA[11]*	91	*PdecMapDsrG*	141	*TestSignalIn[4]*	191	*TmeEncQOut*
42	*Vss[3]*	92	*PdecMapData*	142	*TmeSIn[G]*	192	*TmeEncIQClk*
43	*MemA[10]*	93	*PdecMapClk*	143	*TmeSClk[G]*	193	*Vss[12]*
44	*Vdd[3]*	94	*PdecRfAvN[3]*	144	*TmeSRdy[G]*	194	*TmeClcwSamp*
45	*MemA[9]*	95	*PdecRfAvN[2]*	145	*TmeSValid[F]*	195	*TmeClcwClk*
46	*MemA[8]*	96	*Vss[16]*	146	*TmeSIn[F]*	196	*TmeClcwD[3]*
47	*MemA[7]*	97	*PdecMapAdt*	147	*TmeSRdy[F]*	197	*TmeClcwD[2]*
48	*Vss[2]*	98	*PdecRfAvN[1]*	148	*TmeSClk[F]*	198	*TmeClcwD[1]*

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
49	*MemA[6]*	99	*Vdd[16]*	149	*TmeSValid[E]*	199	*Vss[24]*
50	*MemA[5]*	100	*PdecRfAvN[0]*	150	*PdecClcwD[0]*	200	*Vdd[24]*
201	*TmeClcwD[0]*	215	*SpwDInB*	229	*CpdmStrb*	243	*TestSignalOut[5]*
202	*ReInit*	216	*SpwIfSel*	230	*CselRmOn*	244	*TestSignalIn[5]*
203	*CiInClk*	217	*SpwSInA*	231	*CselStatusIn[2]*	245	*MemDcc[5]*
204	*CiInData*	218	*SpwDInA*	232	*CselStatusIn[1]*	246	*MemDcc[4]*
205	*Vdd[12]*	219	*SpwClk*	233	*CselStatusIn[0]*	247	*Vdd[9]*
206	*CiInRdy*	220	*Vdd[11]*	234	*Vdd[10]*	248	*MemDcc[3]*
207	*CiInValid*	221	*SpwSOut*	235	*Irq*	249	*Vss[25]*
208	*CiOutRdy*	222	*SpwDOut*	236	*CselStatusOut[2]*	250	*Vdd[25]*
209	*CiOutClk*	223	*CpdmClkAlive*	237	*CselStatusOut[1]*	251	*MemDcc[2]*
210	*CiOutData*	224	*CpdmClkToggle*	238	*CselStatusOut[0]*	252	*MemDcc[1]*
211	*Vss[11]*	225	*CpdmClk*	239	*TestSignalOut[2]*	253	*MemDcc[0]*
212	*CiOutValid*	226	*Vss[10]*	240	*TestSignalOut[3]*	254	*MemD[15]*
213	*TestSignalOut[1]*	227	*CpdmSer*	241	*Vss[9]*	255	*MemD[14]*
214	*SpwSInB*	228	*CpdmArmN*	242	*TestSignalOut[4]*	256	*MemD[13]*

Signals pins are described in AT7909E datasheet.

FIGURE 3. Block diagram

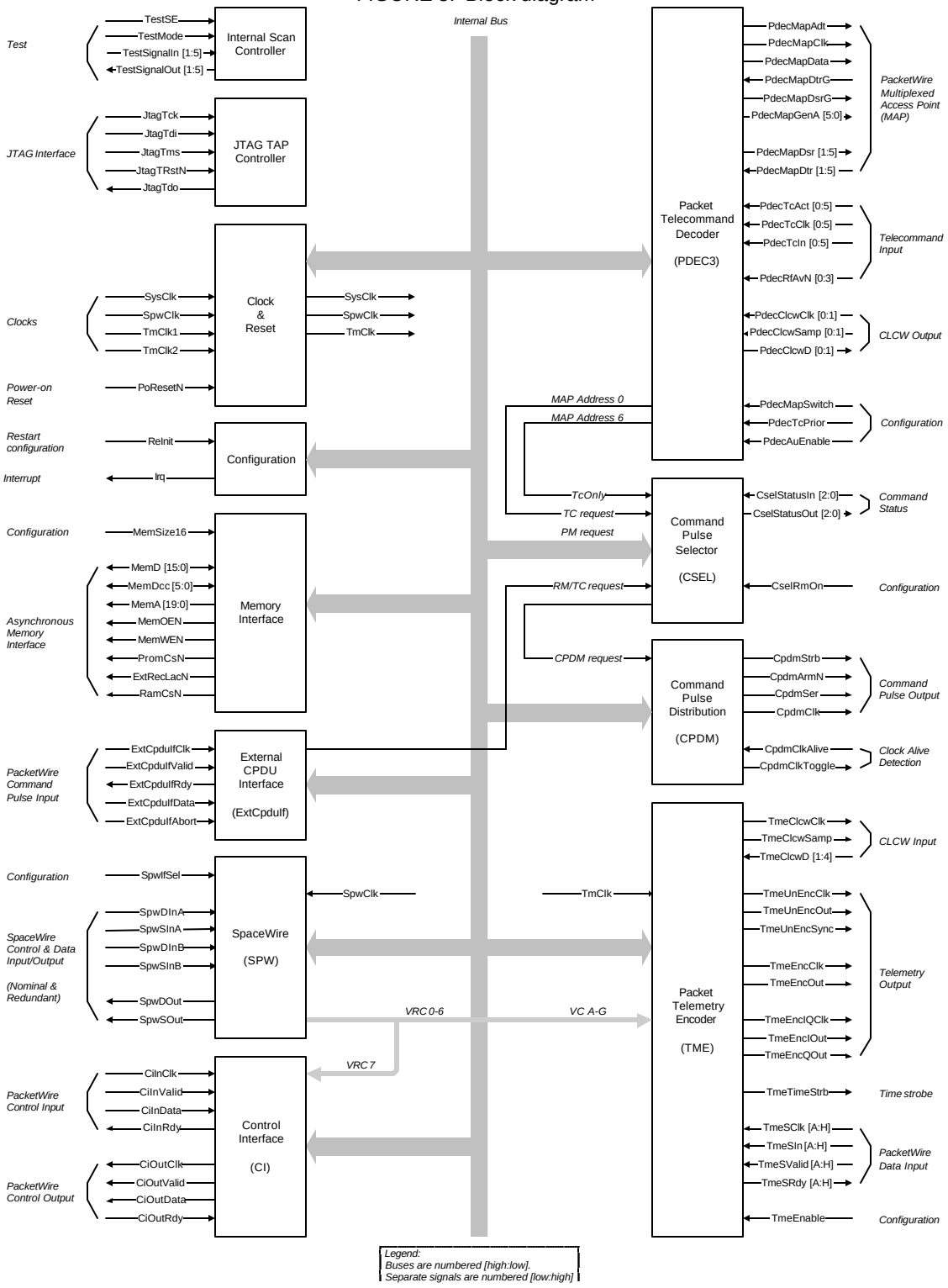


FIGURE 4. Electrical circuit for power burn-in and operating life test.

Characteristics	Symbol	Conditions	Unit
Ambient Temperature	Tamb	125 (+0/-5)	°C
Positive Supply Voltage	VCC	3.7V (+0.1 /-0.1)	V
Negative Supply Voltage	GND	0	V

Forcing inputs:

S1 = 1.65 MHz
S3 = 412.50 KHz
S6 = 51.56 KHz
S9 = 100.70 Hz
S10 = 50.30 Hz
All signals are issued from the same clock and there is no overlap on timings
- Inputs must be wired to a defined level: VCC, GND or Driver Signals
- Connecting an input to VCC 'or' GND must always be through a 2.2k serie resistor

Forcing outputs:

- Output must be wired to VCC and GND
- Connecting an output to VCC 'and' GND must always be through two 5.6k series resistors.

Forcing inputs/outputs:

- I/O must be wired as Input or Output following previous definition.
- By default I/O are considered as Input

Pin Number	Pad number	Signal	Model	Type	Pull type	Resistance	Wired
1	1	VSB28	PVSSB	VSB		0	GND
2	2	MemD_12_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
3	3	MemD_11_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
4	4	MemD_10_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
5	5	VDB26	PVDDVB	VDB		0	VCC
6	6	MemD_9_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
7	515	VSA27	PVSSA	VSA		0	GND
7	525	VSA24	PVSSA	VSA		0	GND
7	536	VSA19	PVSSA	VSA		0	GND
8	274	VDA22	PVDDA	VDA		0	VCC
8	264	VDA25	PVDDA	VDA		0	VCC
8	287	VDA16	PVDDA	VDA		0	VCC
9	7	MemD_8_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
10	8	MemD_7_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
11	9	MemD_6_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
12	10	MemD_5_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
13	11	MemD_4_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
14	12	MemD_3_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
15	13	VSB23	PVSSB	VSB		0	GND
16	14	PdecTcDyn	PICV:PRD6V	I	PD	2.2k	S6

17	15	MemD_2_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
18	16	MemD_1_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
19	17	VDB21	PVDDVB	VDB		0	VCC
20	18	MemD_0_	PICV:PO33V:PRD6	VI/O	PD	2.2k	GND
21	19	MemCSN_3_	PO66VF	O/Z		5.6k	VCC-GND
22	20	VSB20	PVSSB	VSB		0	GND
23	21	PdecTcPrior	PICV:PRD6V	I	PD	2.2k	S6
24	22	MemCSN_2_	PO66VF	O/Z		5.6k	VCC-GND
25	23	MemCSN_0_	PO66VF	O/Z		5.6k	VCC-GND
26	24	VDB18	PVDDVB	VDB		0	VCC
27	25	MemOEN	PO66VF	O/Z		5.6k	VCC-GND
28	26	MemWEN	PO66VF	O/Z		5.6k	VCC-GND
29	27	VSB17	PVSSB	VSB		0	GND
30	28	MemA_19_	PO66VF	O/Z		5.6k	VCC-GND
31	29	MemA_18_	PO66VF	O/Z		5.6k	VCC-GND
32	30	VDB15	PVDDVB	VDB		0	VCC
33	31	MemA_17_	PO66VF	O/Z		5.6k	VCC-GND
34	32	MemA_16_	PO66VF	O/Z		5.6k	VCC-GND
35	33	VSB14	PVSSB	VSB		0	GND
36	34	MemA_15_	PO66VF	O/Z		5.6k	VCC-GND
37	35	MemA_14_	PO66VF	O/Z		5.6k	VCC-GND
38	36	VDB12	PVDDVB	VDB		0	VCC
39	37	MemA_13_	PO66VF	O/Z		5.6k	VCC-GND
40	38	MemA_12_	PO66VF	O/Z		5.6k	VCC-GND
41	39	MemA_11_	PO66VF	O/Z		5.6k	VCC-GND
42	40	VSB10	PVSSB	VSB		0	GND
43	41	MemA_10_	PO66VF	O/Z		5.6k	VCC-GND
44	42	VDB9	PVDDVB	VDB		0	VCC
45	43	MemA_9_	PO66VF	O/Z		5.6k	VCC-GND
46	44	MemA_8_	PO66VF	O/Z		5.6k	VCC-GND
47	45	MemA_7_	PO66VF	O/Z		5.6k	VCC-GND
48	46	VSB7	PVSSB	VSB		0	GND
49	47	MemA_6_	PO66VF	O/Z		5.6k	VCC-GND
50	48	MemA_5_	PO66VF	O/Z		5.6k	VCC-GND
51	49	VDB6	PVDDVB	VDB		0	VCC
52	50	MemA_4_	PO66VF	O/Z		5.6k	VCC-GND
53	51	MemA_3_	PO66VF	O/Z		5.6k	VCC-GND
54	52	MemA_2_	PO66VF	O/Z		5.6k	VCC-GND
55	53	VSB4	PVSSB	VSB		0	GND
56	54	MemA_1_	PO66VF	O/Z		5.6k	VCC-GND
57	570	VSA3	PVSSA	VSA		0	GND
57	560	VSA8	PVSSA	VSA		0	GND
57	547	VSA13	PVSSA	VSA		0	GND
58	309	VDA5	PVDDA	VDA		0	VCC
58	318	VDA1	PVDDA	VDA		0	VCC
58	297	VDA11	PVDDA	VDA		0	VCC
59	55	MemA_0_	PO66VF	O/Z		5.6k	VCC-GND
60	56	VDB2	PVDDVB	VDB		0	VCC

61	57	MemSiz	PICV	I		2.2k	S6
62	58	ExtdAccess	PICV	I		2.2k	S6
63	59	TestMode	PICV:PRD6V	I	PD	2.2k	VCC
64	60	TestSE	PICV:PRD6V	I	PD	2.2k	S10
65	61	JtagTdo	PO22V	O/Z		5.6k	VCC-GND
66	62	JtagTdi	PICV:PRD6V	I	PD	2.2k	S6
67	63	JtagTms	PICV:PRD6V	I	PD	2.2k	S6
68	64	JtagTRstN	PICV:PRD6V	I	PD	2.2k	S10
69	65	JtagTck	PICV:PRD6V	I	PD	2.2k	S1
70	66	PdecMapGenA_5_	PO22V	O/Z		5.6k	VCC-GND
71	600	VSA76	PVSSA	VSA		0	GND
71	589	VSA79	PVSSA	VSA		0	GND
71	579	VSA82	PVSSA	VSA		0	GND
72	328	VDA81	PVDDA	VDA		0	VCC
72	350	VDA75	PVDDA	VDA		0	VCC
72	337	VDA78	PVDDA	VDA		0	VCC
73	67	PdecMapGenA_4_	PO22V	O/Z		5.6k	VCC-GND
74	68	PdecMapGenA_3_	PO22V	O/Z		5.6k	VCC-GND
75	69	PdecMapGenA_2_	PO22V	O/Z		5.6k	VCC-GND
76	70	PdecMapGenA_1_	PO22V	O/Z		5.6k	VCC-GND
77	71	PdecMapGenA_0_	PO22V	O/Z		5.6k	VCC-GND
78	72	VSB80	PVSSB	VSB		0	GND
79	73	PdecMapDtr_5_	PICV:PRD6V	I	PD	2.2k	S6
80	74	PdecMapDsr_5_	PO22V	O/Z		5.6k	VCC-GND
81	75	PdecMapDtr_4_	PICV:PRD6V	I	PD	2.2k	S6
82	76	PdecMapDsr_4_	PO22V	O/Z		5.6k	VCC-GND
83	77	VDB77	PVDDVB	VDB		0	VCC
84	78	PdecMapDtr_3_	PICV:PRD6V	I	PD	2.2k	S6
85	79	PdecMapDsr_3_	PO22V	O/Z		5.6k	VCC-GND
86	80	PdecMapDtr_2_	PICV:PRD6V	I	PD	2.2k	S6
87	81	PdecMapDsr_2_	PO22V	O/Z		5.6k	VCC-GND
88	82	PdecMapDtr_1_	PICV:PRD6V	I	PD	2.2k	S6
89	83	PdecMapDsr_1_	PO22V	O/Z		5.6k	VCC-GND
90	84	PdecMapDtrG	PICV:PRD6V	I	PD	2.2k	S6
91	85	PdecMapDsrG	PO22V	O/Z		5.6k	VCC-GND
92	86	PdecMapData	PO22V	O/Z		5.6k	VCC-GND
93	87	PdecMapClk	PO33V	O/Z		5.6k	VCC-GND
94	88	PdecRfAvN_3_	PICSV:PRD6V	I	PD	2.2k	S9
95	89	PdecRfAvN_2_	PICSV:PRD6V	I	PD	2.2k	S9
96	90	VSB74	PVSSB	VSB		0	GND
97	91	PdecMapAdt	PO22V	O/Z		5.6k	VCC-GND
98	92	PdecRfAvN_1_	PICSV:PRD6V	I	PD	2.2k	S6
99	93	VDB73	PVDDVB	VDB		0	VCC
100	94	PdecRfAvN_0_	PICSV:PRD6V	I	PD	2.2k	S6
101	95	M1553Clk	PICV	I		2.2k	S1
102	96	ObtSrcClk	PICV	I		2.2k	S1
103	97	TmClk1	PICV	I		2.2k	S1
104	98	TmClk2	PICV	I		2.2k	S1

105	99	SysClk	PICV	I		2.2k	S1
106	100	PoResetN	PICSV	I		2.2k	VCC
107	101	PdecTcIn_5_	PICSV:PRD6V	I	PD	2.2k	S6
108	102	PdecTcClk_5_	PICSV:PRD6V	I	PD	2.2k	S3
109	103	PdecTcAct_5_	PICSV:PRD6V	I	PD	2.2k	S6
110	104	PdecTcIn_4_	PICSV:PRD6V	I	PD	2.2k	S6
111	105	PdecTcClk_4_	PICSV:PRD6V	I	PD	2.2k	S3
112	106	PdecTcAct_4_	PICSV:PRD6V	I	PD	2.2k	S6
113	107	PdecTcIn_3_	PICSV:PRD6V	I	PD	2.2k	S6
114	108	PdecTcClk_3_	PICSV:PRD6V	I	PD	2.2k	S3
115	109	PdecTcAct_3_	PICSV:PRD6V	I	PD	2.2k	S6
116	110	PdecTcIn_2_	PICSV:PRD6V	I	PD	2.2k	S6
117	111	PdecTcClk_2_	PICSV:PRD6V	I	PD	2.2k	S3
118	112	VSB68	PVSSB	VSB		0	GND
119	113	PdecTcAct_2_	PICSV:PRD6V	I	PD	2.2k	S6
120	114	PdecTcIn_1_	PICSV:PRD6V	I	PD	2.2k	S6
121	624	VSA70	PVSSA	VSA		0	GND
121	611	VSA72	PVSSA	VSA		0	GND
121	634	VSA67	PVSSA	VSA		0	GND
122	361	VDA71	PVDDA	VDA		0	VCC
122	373	VDA69	PVDDA	VDA		0	VCC
122	382	VDA65	PVDDA	VDA		0	VCC
123	115	PdecTcClk_1_	PICSV:PRD6V	I	PD	2.2k	S3
124	116	VDB66	PVDDVB	VDB		0	VCC
125	117	PdecTcAct_1_	PICSV:PRD6V	I	PD	2.2k	S6
126	118	PdecTcIn_0_	PICSV:PRD6V	I	PD	2.2k	S6
127	119	PdecTcClk_0_	PICSV:PRD6V	I	PD	2.2k	S3
128	120	PdecTcAct_0_	PICSV:PRD6V	I	PD	2.2k	S6
129	121	PdecClcwD_1_	PO22V	O/Z		5.6k	VCC-GND
130	122	PdecClcwSamp_1_	PICSV:PRD6V	I	PD	2.2k	S6
131	123	PdecClcwClk_1_	PICSV:PRD6V	I	PD	2.2k	S3
132	124	PdecMapSwitch	PICV:PRD6V	I	PD	2.2k	S6
133	125	TmeSValidNom_7_	PICV:PRD6V	I	PD	2.2k	S6
134	126	PdecAuEnable	PICSV:PRD6V	I	PD	2.2k	S6
135	664	VSA60	PVSSA	VSA		0	GND
135	654	VSA62	PVSSA	VSA		0	GND
135	643	VSA64	PVSSA	VSA		0	GND
136	415	VDA59	PVDDA	VDA		0	VCC
136	402	VDA61	PVDDA	VDA		0	VCC
136	392	VDA63	PVDDA	VDA		0	VCC
137	127	TmeSInNom_7_	PICV:PRD6V	I	PD	2.2k	S6
138	128	TmeSClkNom_7_	PICV:PRD6V	I	PD	2.2k	S1
139	129	TmeSRdy_7_	PO22V	O/Z		5.6k	VCC-GND
140	130	TmeSValidNom_6_	PICV:PRD6V	I	PD	2.2k	S6
141	131	TmeSInRed_6_	PICV:PRD6V	I	PD	2.2k	S6
142	132	TmeSInNom_6_	PICV:PRD6V	I	PD	2.2k	S6
143	133	TmeSClkNom_6_	PICV:PRD6V	I	PD	2.2k	S1
144	134	TmeSRdy_6_	PO22V	O/Z		5.6k	VCC-GND

145	135	TmeSValidNom_5_	PICV:PRD6V	I	PD	2.2k	S6
146	136	TmeSInNom_5_	PICV:PRD6V	I	PD	2.2k	S6
147	137	TmeSRdy_5_	PO22V	O/Z		5.6k	VCC-GND
148	138	TmeSClkNom_5_	PICV:PRD6V	I	PD	2.2k	S1
149	139	TmeSValidNom_4_	PICV:PRD6V	I	PD	2.2k	S6
150	140	PdecClcwD_0_	PO22V	O/Z		5.6k	VCC-GND
151	141	PdecClcwSamp_0_	PICSV:PRD6V	I	PD	2.2k	S6
152	142	TmeSInNom_4_	PICV:PRD6V	I	PD	2.2k	S6
153	143	PdecClcwClk_0_	PICSV:PRD6V	I	PD	2.2k	S3
154	144	TmeSClkNom_4_	PICV:PRD6V	I	PD	2.2k	S1
155	145	TmeSRdy_4_	PO22V	O/Z		5.6k	VCC-GND
156	146	TmeSRdy_3_	PO22V	O/Z		5.6k	VCC-GND
157	147	TmeSValidNom_3_	PICV:PRD6V	I	PD	2.2k	S6
158	148	TmeSInNom_3_	PICV:PRD6V	I	PD	2.2k	S6
159	149	TmeSClkNom_3_	PICV:PRD6V	I	PD	2.2k	S1
160	150	VSB58	PVSSB	VSB		0	GND
161	151	TmeSRdy_2_	PO22V	O/Z		5.6k	VCC-GND
162	152	TmeSValidNom_2_	PICV:PRD6V	I	PD	2.2k	S6
163	153	TmeSInNom_2_	PICV:PRD6V	I	PD	2.2k	S6
164	154	TmeSClkNom_2_	PICV:PRD6V	I	PD	2.2k	S1
165	155	ExtCpduIfAbort	PICSV:PRD6V	I	PD	2.2k	S6
166	156	TmeSValidNom_1_	PICV:PRD6V	I	PD	2.2k	S6
167	157	ExtCpduIfValid	PICSV:PRD6V	I	PD	2.2k	S6
168	158	ExtCpduIfRdy	PO22V	O/Z		5.6k	VCC-GND
169	159	ExtCpduIfData	PICSV:PRD6V	I	PD	2.2k	S6
170	160	TmeSInNom_1_	PICV:PRD6V	I	PD	2.2k	S6
171	161	ExtCpduIfClk	PICSV:PRD6V	I	PD	2.2k	S1
172	162	TmeSClkNom_1_	PICV:PRD6V	I	PD	2.2k	S1
173	163	TmeSRdy_1_	PO22V	O/Z		5.6k	VCC-GND
174	164	TmeSRdy_0_	PO22V	O/Z		5.6k	VCC-GND
175	165	TmeSValidNom_0_	PICV:PRD6V	I	PD	2.2k	S6
176	166	TmeSInNom_0_	PICV:PRD6V	I	PD	2.2k	S6
177	167	TmeSClkNom_0_	PICV:PRD6V	I	PD	2.2k	S1
178	168	TmeEnable	PICSV:PRD6V	I	PD	2.2k	S6
179	169	VDB54	PVDDVB	VDB		0	VCC
180	170	TmeTimeStrb	PO22V	O/Z		5.6k	VCC-GND
181	171	TmeUnEncSync	PO33V	O/Z		5.6k	VCC-GND
182	172	TmeUnEncClk	PO66VF	O/Z		5.6k	VCC-GND
183	173	VSB52	PVSSB	VSB		0	GND
184	174	TmeUnEncOut	PO66VF	O/Z		5.6k	VCC-GND
185	688	VSA55	PVSSA	VSA		0	GND
185	698	VSA51	PVSSA	VSA		0	GND
185	675	VSA57	PVSSA	VSA		0	GND
186	446	VDA49	PVDDA	VDA		0	VCC
186	437	VDA53	PVDDA	VDA		0	VCC
186	425	VDA56	PVDDA	VDA		0	VCC
187	175	VDB50	PVDDVB	VDB		0	VCC
188	176	TmeEncOut	PO66VF	O/Z		5.6k	VCC-GND

189	177	TmeEncClk	PO66VF	O/Z		5.6k	VCC-GND
190	178	TmeEnc	IOut PO33V	O/Z		5.6k	VCC-GND
191	179	TmeEnc	QOut PO33V	O/Z		5.6k	VCC-GND
192	180	TmeEncIQClk	PO33V	O/Z		5.6k	VCC-GND
193	181	VSB48	PVSSB	VSB		0	GND
194	182	TmeClcwSamp	PO22V	O/Z		5.6k	VCC-GND
195	183	TmeClcwClk	PO22V	O/Z		5.6k	VCC-GND
196	184	TmeClcwD_3_	PICV:PRD6V	I	PD	2.2k	S6
197	185	TmeClcwD_2_	PICV:PRD6V	I	PD	2.2k	S6
198	186	TmeClcwD_1_	PICV:PRD6V	I	PD	2.2k	S6
199	717	VSA44	PVSSA	VSA		0	GND
199	728	VSA41	PVSSA	VSA		0	GND
199	707	VSA47	PVSSA	VSA		0	GND
200	456	VDA46	PVDDA	VDA		0	VCC
200	478	VDA39	PVDDA	VDA		0	VCC
200	465	VDA43	PVDDA	VDA		0	VCC
201	187	TmeClcwD_0_	PICV:PRD6V	I	PD	2.2k	S6
202	188	ReInit	PICSV:PRD6V	I	PD	2.2k	S6
203	189	CiInClk	PICV:PRD6V	I	PD	2.2k	S1
204	190	CiInData	PICV:PRD6V	I	PD	2.2k	S6
205	191	VDB45	PVDDVB	VDB		0	VCC-GND
206	192	CiInRdy	PO33V	O/Z		5.6k	VCC-GND
207	193	CiInValid	PICV:PRD6V	I	PD	2.2k	S6
208	194	CiOutRdy	PICV:PRD6V	I	PD	2.2k	S6
209	195	CiOutClk	PO33V	O/Z		5.6k	VCC-GND
210	196	CiOutData	PO33V	O/Z		5.6k	VCC-GND
211	197	VSB42	PVSSB	VSB		0	GND
212	198	CiOutValid	PO33V	O/Z		5.6k	VCC-GND
213	199	SpwEnA	PO22V	O/Z		5.6k	VCC-GND
214	200	SpwSInB	PICV	I		2.2k	S6
215	201	SpwDInB	PICV	I		2.2k	S6
216	202	SpwIfSel	PICSV:PRD6V	I	PD	2.2k	S6
217	203	SpwSInA	PICV	I		2.2k	S1
218	204	SpwDInA	PICV	I		2.2k	S6
219	205	SpwClk	PICV	I		2.2k	S1
220	206	VDB40	PVDDVB	VDB		0	VCC
221	207	SpwSOut	PO33V	O/Z		5.6k	VCC-GND
222	208	SpwDOut	PO33V	O/Z		5.6k	VCC-GND
223	209	CpdmClkAlive	PICSV	I		2.2k	S6
224	210	CpdmClkToggle	PO33V	O/Z		5.6k	VCC-GND
225	211	CpdmClk	PO33V	O/Z		5.6k	VCC-GND
226	212	VSB38	PVSSB			VSB	0
227	213	CpdmSer	PO33V	O/Z		5.6k	VCC-GND
228	214	CpdmArmN	PO22V	O/Z		5.6k	VCC-GND
229	215	CpdmStrb	PO22V	O/Z		5.6k	VCC-GND
230	216	CselRmOn	PICSV:PRD6V	I	PD	2.2k	S6
231	217	CselStsIn_2_	PICSV:PRD6V	I	PD	2.2k	S6
232	218	CselStsIn_1_	PICSV:PRD6V	I	PD	2.2k	S6

233	219	CselStsIn_0_	PICSV:PRD6V	I	PD	2.2k	S6
234	220	VDB35	PVDDVB	VDB		0	VCC
235	221	SeqIrq	PO22V	O/Z		5.6k	VCC-GND
236	222	CselStsOut_2_	PO22V	O/Z		5.6k	VCC-GND
237	223	CselStsOut_1_	PO22V	O/Z		5.6k	VCC-GND
238	224	CselStsOut_0_	PO22V	O/Z		5.6k	VCC-GND
239	225	TxBIhb	PO22V	O/Z		5.6k	VCC-GND
240	226	TxAIhb	PO22V	O/Z		5.6k	VCC-GND
241	227	VSB33	PVSSB	VSB		0	GND
242	228	DataOutN	PO22V	O/Z		5.6k	VCC-GND
243	229	DataOutP	PO22V	O/Z		5.6k	VCC-GND
244	230	DataInAN	PICSV:PRD6V	I	PD	2.2k	S1
245	231	MemDcc_5_	PICV:PO33V:PRD6V	I/O	PD	2.2k	GND
246	232	MemDcc_4_	PICV:PO33V:PRD6V	I/O	PD	2.2k	GND
247	233	VDB31	PVDDVB	VDB		0	VCC
248	234	MemDcc_3_	PICV:PO33V:PRD6V	I/O	PD	2.2k	GND
249	753	VSA34	PVSSA	VSA		0	GND
249	762	VSA30	PVSSA	VSA		0	GND
249	739	VSA37	PVSSA	VSA		0	GND
250	489	VDA36	PVDDA	VDA		0	VCC
250	501	VDA32	PVDDA	VDA		0	VCC
250	510	VDA29	PVDDA	VDA		0	VCC
251	235	MemDcc_2_	PICV:PO33V:PRD6V	I/O	PD	2.2k	GND
252	236	MemDcc_1_	PICV:PO33V:PRD6V	I/O	PD	2.2k	GND
253	237	MemDcc_0_	PICV:PO33V:PRD6V	I/O	PD	2.2k	GND
254	238	MemD_15_	PICV:PO33V:PRD6V	I/O	PD	2.2k	GND
255	239	MemD_14_	PICV:PO33V:PRD6V	I/O	PD	2.2k	GND
256	240	MemD_13_	PICV:PO33V:PRD6V	I/O	PD	2.2k	GND