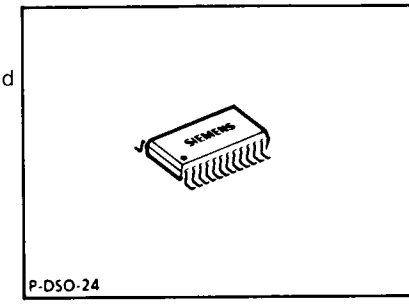
SIEMENS

GSM Receiver Circuit PMB 2400

Preliminary Data **Bipolar IC**

1 Features



- Heterodyne receiver with demodulator
- Downward mixing from 900-MHz receiver band to the base band
- Demodulation and generation of I/Q components
- Low mixer noise (about 7 dB)
- High intercept point
- Integrated phase shifter
- 60-dB AGC control range
- Field strength indication with 70-dB dynamic range
- Integrated SAW driver
- High dynamic range of more than 100 dB
- Different demodulation schemes
- Completely separated 1st mixer and IF stages with separate power-down capability
- Wide input frequency range
- Wide IF range from 45 MHz to 90 MHz
- P-DSO-24 package
- Temperature range – 25 °C to + 85 °C

Applications

- Digital mobile radio
- GSM-systems
- Various demodulation schemes, such as FM, FSR, QAM, QPSR, GMSK
- Space and power saving optimizations of existing discrete demodulator circuits.

Type	Ordering code	Package
PMB 2400	Q67000-A6024	P-DSO-24

Figure 1
Logic Symbol
PMB 2400 Logic- and Analog-Interfaces

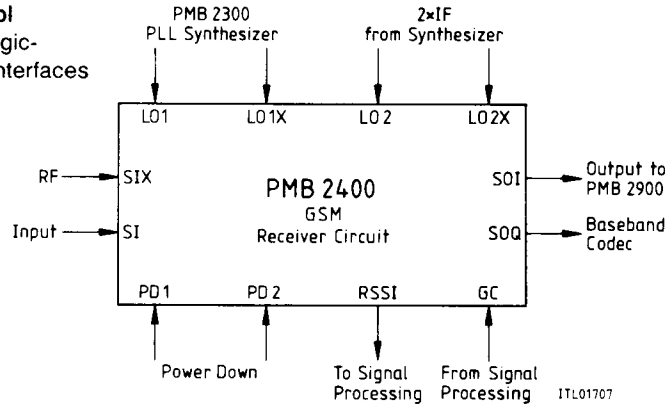
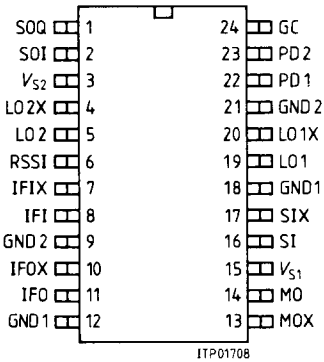


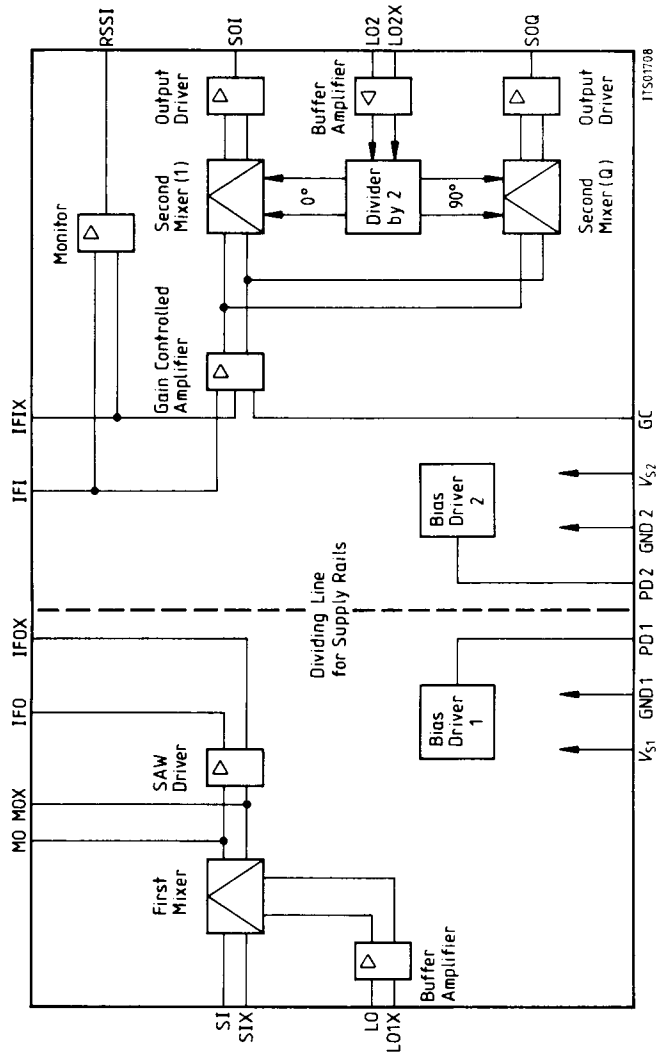
Figure 2
Pin Configuration
(top view)



Pin Definitions and Functions

Pin Number	Symbol	Function
1	SOQ	Quadrature Signal Output
2	SOI	In-Phase Signal Output
3	V_{S2}	Supply Voltage 2
4	LO2X	Inverting Input for Second Local Oscillator
5	LO2	Non-inverting Input for Second Local Oscillator
6	RSSI	Field Strength Output
7	IFI	Non-inverting IF Input
8	IFIX	Inverting IF Input
9	GND2	Ground 2
10	IFOX	Inverted IF Output
11	IFO	Non-inverted IF Output
12	GND1	Ground 1
13	MOX	Inverted Output of First Mixer
14	MO	Non-inverted Output of First Mixer
15	V_{S2}	Supply Voltage 1
16	SI	Non-inverting Signal Input
17	SIX	Inverting Signal Input
18	GND1	Ground 1
19	LO1X	Inverting Input for First Local Oscillator
20	LO1	Non-inverting Input for First Local Oscillator
21	GND2	Ground 2
22	PD1	Power Down Input 1
23	PD2	Power Down Input 2
24	GC	Gain Control Input

Figure 3
Block Diagram



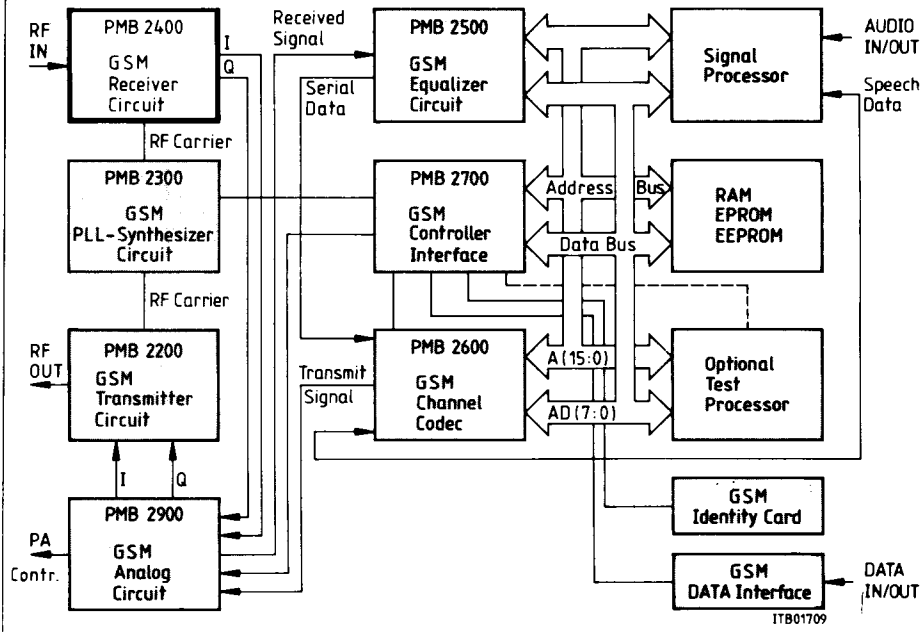
2 System Integration

The basic structure of a mobile receiver built with the Siemens GSM chip set is shown below.

The receiver chip PMB 2400 uses the incoming signal from the low noise amplifier to do the down conversion as well as the demodulation and generation of the I- and Q-signals.These signals are fed into the baseband codec PMB 2900.

Furthermore the automatic gain control stage of the PMB 2400 compensates the varying signal strength by means of a gain control signal coming from the signal processing circuitry. The evaluation logic for this loop can be fed with an RSSI signal supplied by the PMB 2400.

Figure 4
GSM Hand-Set with the PMB 2400



3 Functional Description

The input signal SI/SIX and the amplified first local oscillator signal LO1/LO1X are mixed down to an intermediate frequency (IF). The open-collector output of the mixer generates a differential current at pins MO/MOX which is filtered by an external resonant circuit. The resulting voltage drives an on-chip SAW driver, which in turn drives an external SAW filter via the IFO/IFOX output, also open-collector.

The second local oscillator signal LO2/LO2X is amplified and fed to a divider, which generates orthogonal signals at half the input frequency. The filtered IF signal reenters the chip through the IFI/IFIX input, where it is amplified and mixed down to the final output frequency with each of the orthogonal signals. The resulting in-phase and quadrature signals pass through output drivers and appear at the SOI and SOQ outputs, respectively. The amplification of the IF signal before the second mixer stage is performed by a gain-controlled amplifier, the gain being determined by the voltage at the gain control input GC. The signal amplitude (field strength) at the IFI/IFIX input is measured by the monitor circuit, which delivers a corresponding voltage at the RSSI output.

Differential signals and symmetrical circuitry are used throughout, except at the signal output. For optimum decoupling, separate ground and supply rails and separate power-down signals are provided for the circuitry before and after the SAW filter. Bias drivers generate internal temperature- and supply voltage- compensated reference voltages required by the various circuit blocks. Switching the power-down inputs PD1, PD2 from HIGH to LOW switches the circuit from its normal operating mode into a standby mode with reduced supply current.

4 Electrical Characteristics

Absolute Maximum Ratings

T_A = – 25 °C to + 85 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply Voltage 1 and 2	V_S	– 0.5	7	V	
Input/Output Voltage (any except open collector)	V_{IO}	– 0.5 – 0.5	V_S + 0.5 7.5	V V	$V_S \leq 7$ V $V_S \geq 7$ V
Open Collector Output	V_{OC}	– 0.5	V_S + 2.5	V	$V_S \leq 5.0$ V
Voltage (MO, MOX, IFO, IFOX)	V	– 0.5	7.5	V	$V_S \geq 5.0$ V
Differential Input Voltage (any differential input)	V_I	– 3	3	V	
Junction Temperature	T_j		125	°C	
Storage Temperature	T_{stg}	– 55	125	°C	
Thermal Resistance (junction to ambient)	R_{ThJA}		55	°C/W	

Operational Range

Within the operational range the IC operates as described in the circuit description. The AC/DC characteristics limits are not guaranteed.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	4.4	5.5	V
Ambient temperature	T_A	– 25	+ 85	°C

AC/DC Characteristics

V_S = 4.5 to 5.5 V; T_A = – 25 to + 85 °C; Test circuit 1

Parameter		Symbol	Limit Values		Unit
			min.	max.	
SI/SIX Input Level	1)	P_{SI}		– 17	dBm
SI/SIX Input Frequency	1)	f_{SI}		960	MHz
LO1/LO1X Input Level	1)	P_{LO1}	– 3	3	dBm
LO1/LO1X Input Frequency	1)	f_{LO1}		1050	MHz
Intermediate Frequency	1)	f_{IF}	45	90	MHz
IFI/IFIX Input Level	1)	P_{IFI}		– 21	dBm
LO2/LO2X Input Level	1)	P_{LO2}	– 20	– 10	dBm
LO2/LO2X Input Frequency	1)	f_{LO2}	90	180	MHz
SOI/SOQ Output Frequency	1)	f_{SO}	0	550	kHz
GC Input Voltage	1)	V_{GC}	0	2	V
PD1/PD2 LOW Voltage	1)	V_{PDL}	0	0.8	V
PD1/PD2 HIGH Voltage	1)	V_{PDH}	4.0	V_S	V

1) Power levels are referred to a resistance of 50 Ω.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Total Supply Current in Normal Operation 4)	I_S	21	27	33	mA	PD = HIGH
Total Supply Current when Powered Down 4)	I_{SPD}			10	µA	PD = LOW

Signal Input SI/SIX

Input Resistance	R_{SI}		25		Ω	
Input Inductance	L_{SI}		10		nH	
Max. Input Level	$P_{SI(max)}$		– 17		dBm	3 dB Compression at MO X
Intercept Point	P_{IP}		8		dBm	
Blocking Level	P_B		– 17		dBm	3 dB Attenuation of Wanted Signal at MO X
Input Interference Level at $f = f_{INT}$	P_{INT}		– 28		dBm	– 98 dBm Interference at $f = (f_{INT} \pm f_{LO1}) \times 2$ at MO X
Input Frequency	f_{SI}			960	MHz	
Noise Figure	F_{SI}		8		dB	

Notes see page 11

AC/DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input for First Local Oscillator LO1/LO1X						
Input Resistance	R_{LO1}		450		Ω	
Input Capacitance	C_{LO1}		870		fF	
Input Level	P_{LO1}	– 3		3	dBm	into 50 Ω
Input Level	V_{LO1}	445		890	mV_{PP}	
Input Frequency	f_{LO1}			1050	MHz	
Output of First Mixer (SAW Driver Input) MO/MOX (Open Collector)						
Resistance	R_{MO}		31		kΩ	
Capacitance	C_{MO}		820		fF	
Total Output Current	$I_{MO}+$ I_{MOX}		5		mA	
Power Gain from Signal Input	G_{MO}		8		dB	into 3 kΩ
Intermediate Frequency	f_{IF}	45		90	MHz	
Output (SAW Driver Output) IFO/IFOX (Open Collector)						
Output Resistance	R_{IFO}		14		kΩ	
Output Capacitance	C_{IFO}		800		fF	
Total Output Current	$I_{IFO}+$ I_{IFOX}		4.5		mA	
Power Gain from Output of First Mixer	G_{IFO}		7		dB	into 1 kΩ
IF Input IFI/FIX						
Input Resistance	R_{IFI}		50		Ω	
Input Capacitance	C_{IFI}		2		pF	
Max. Input Level	P_{IFI}		– 23		dBm	V_{GC} = 2 V, 3 dB
Max. Input Level	V_{IFI}		45		mV_{PP}	Compression at SO
Input for Second Local Oscillator LO2/LO2X						
Input Resistance	R_{LO2}		10		kΩ	
Input Capacitance	C_{LO2}		1		pF	
Input Level	P_{LO2}	– 20		– 10	dBm	into 50 kΩ
Input Level	V_{LO2}	63		200	mV_{PP}	
Input Frequency	f_{LO2}	90		182	MHz	

Notes see page 11

AC/DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Signal Outputs SOI, SOQ						
Output Resistance	R_{SO}		40		kΩ	
Output Capacitance	C_{SO}		0.7		pF	
DC Output Level	V_{SO}		2.5		V	
Power Gain from IF Input	G_{SO}	78			dB	into 50 Ω, V_{GC} = 0 V
Power Gain from IF Input	G_{SO}			14	dB	into 50 Ω, V_{GC} = 2 V
Distortion Factor	D_{SO}		30		dB	P_{IFI} = – 89 dBm, V_{GC} = 0 V
Distortion Factor	D_{SO}		30		dB	P_{IFI} = – 23 dBm, V_{GC} = 2.5 V
Field Strength Output RSSI						
Output Resistance	R_{RSSI}		6.25		kΩ	
Field Strength Factor 5)	F_{RSSI}	20	22	25	mV/dB	
Gain Control Pin GC						
GC Input Voltage	V_{GC}	0		2	V	
GC Input Current	$-I_{GC}$			1	µA	0 V ≤ V_{GC} ≤ 2 V
Gain Control Factor 6)	F_{GC}		0.03	0.1	dB/V	
Power Down Inputs PD1, PD2						
LOW Input Voltage	V_{PDL}	0		0.8	V	
LOW Input Current	I_{PDL}			0.1	µA	V_{PDL} = 0.8 V
HIGH Input Voltage	V_{PDH}	4		V_S	V	
HIGH Input Current	I_{PDH}		10	20	µA	V_{PDH} = 4 V

Notes for pages 9 to 11

1) Parameters for symmetrical inputs and outputs refer to the differential-mode signal.
2) Input and output impedances are modelled as a resistor in parallel with a capacitor.
3) The total supply current includes the current drawn by open-collector outputs.
4) F_{RRSI} = dV_{RSSI}/dP_{IFI}.
5) F_{GC} = dG_{SO}/dV_{GC}.

5 Test and Application Circuits

Figure 5
AF Test Circuit

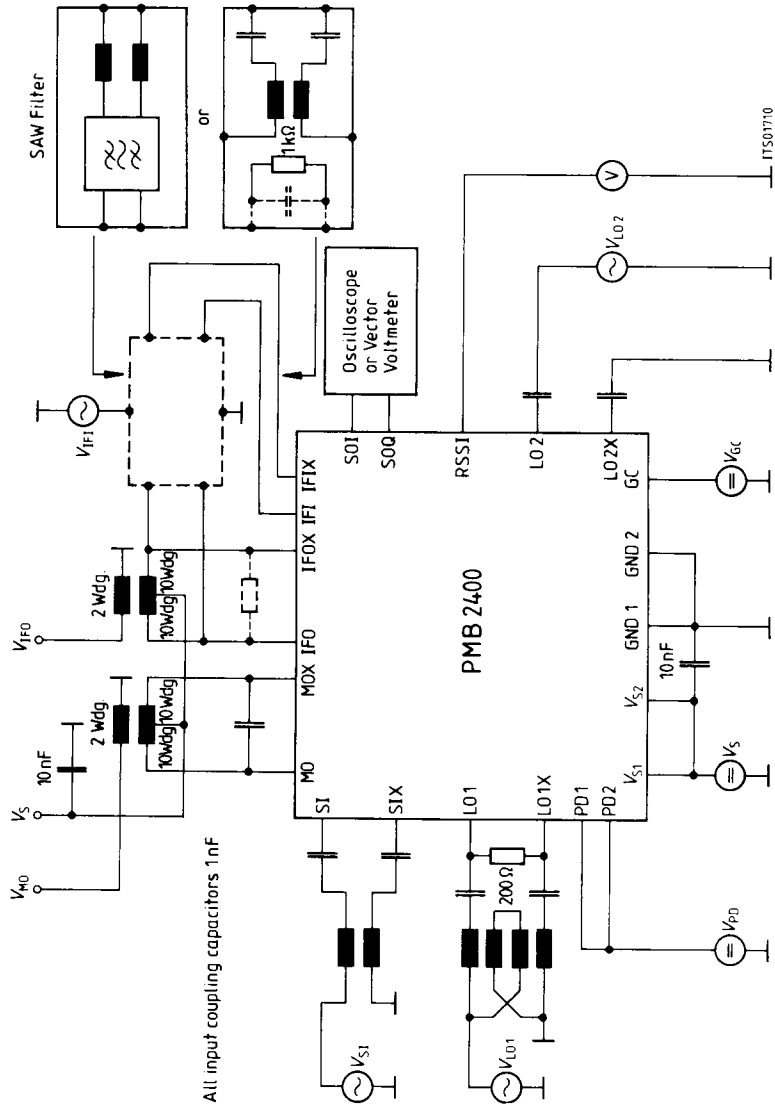


Figure 6
Application Circuit

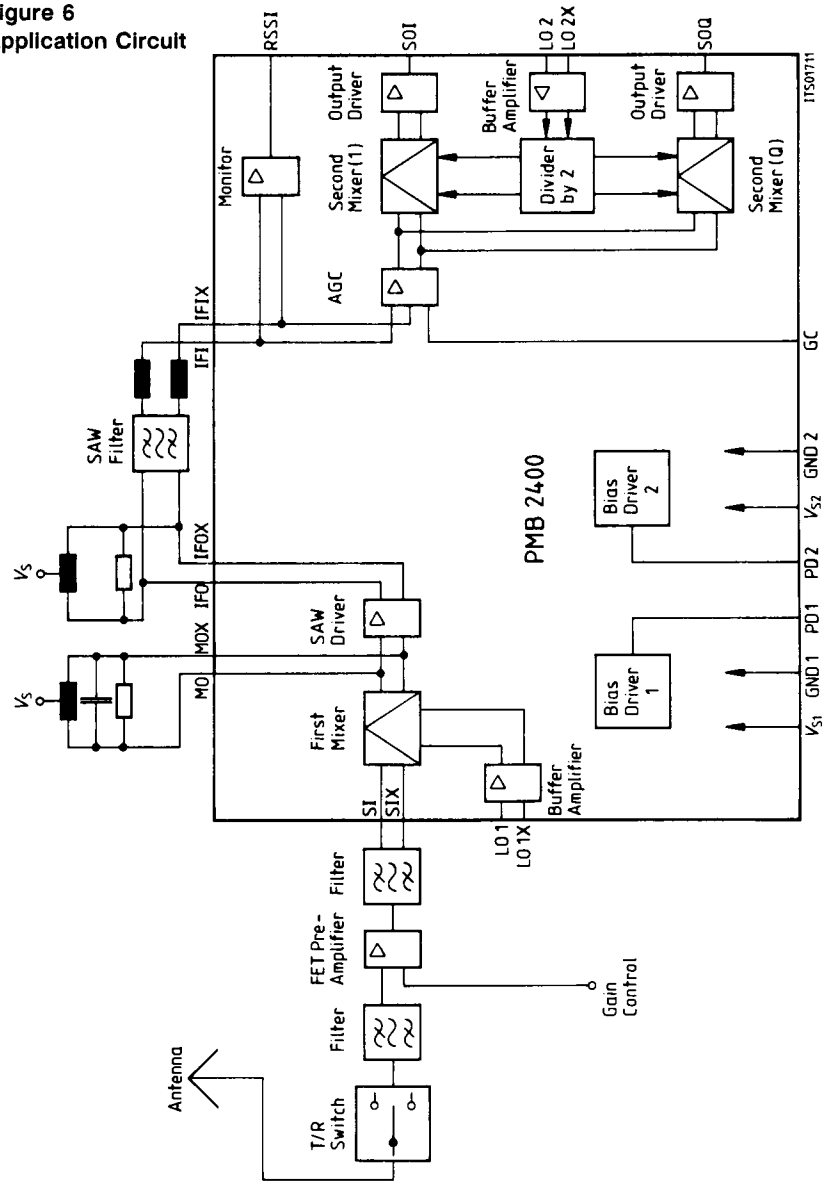


Figure 7
Gain Control Characteristic

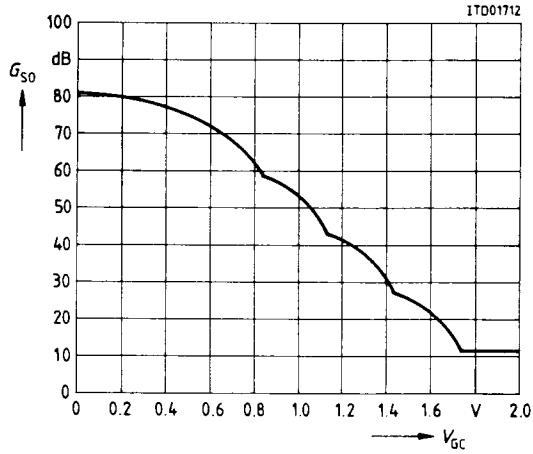


Figure 8
Monitor Characteristic

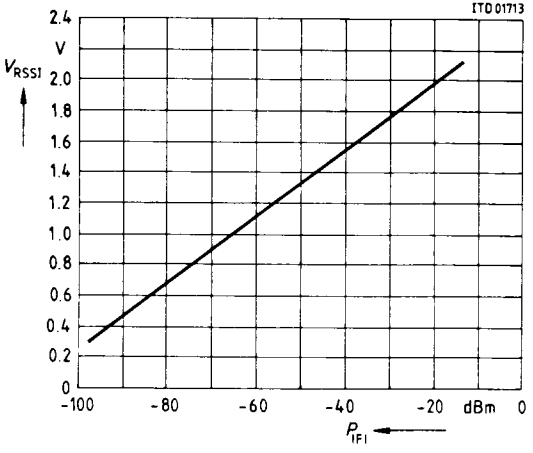
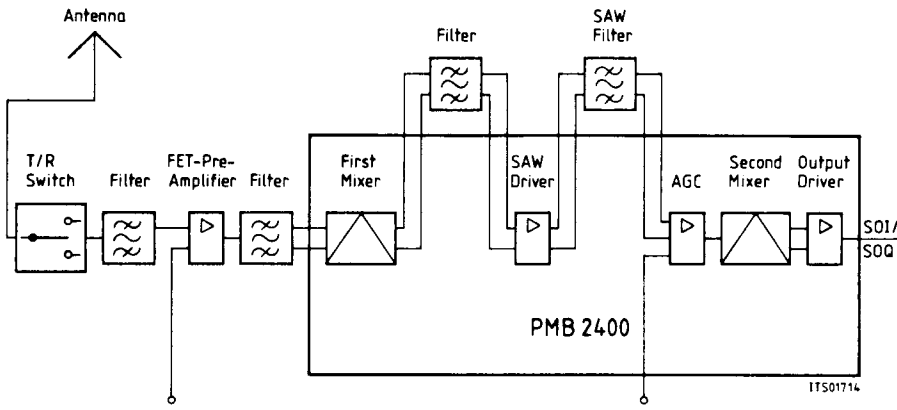


Figure 9
Worst Case Signal Levels without Blocking Level



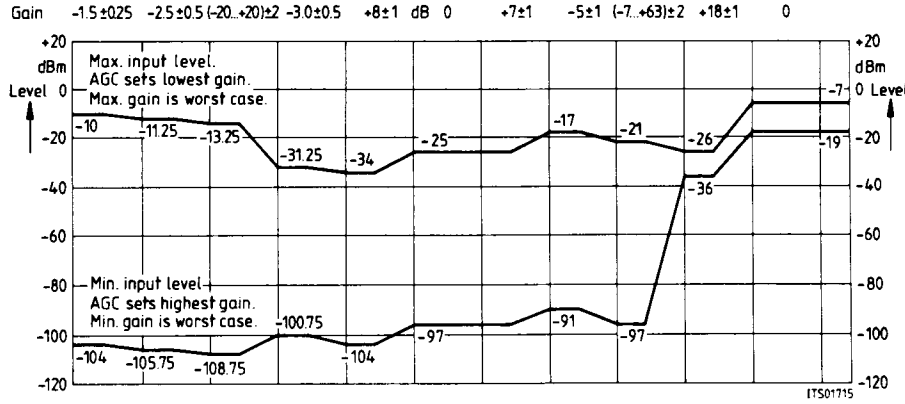
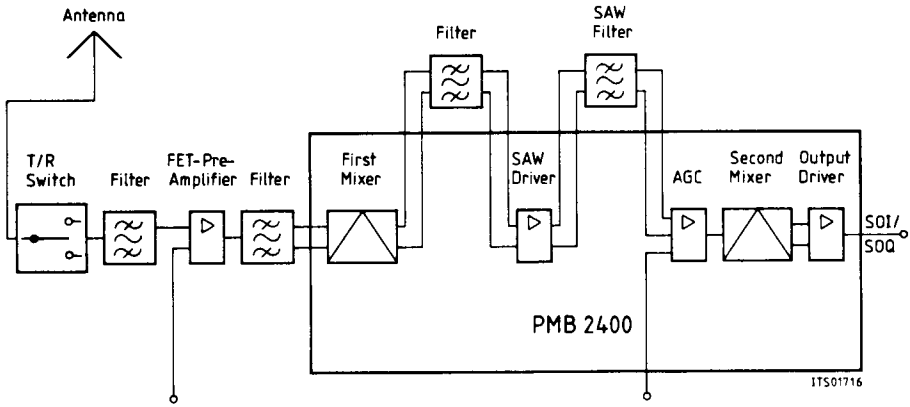
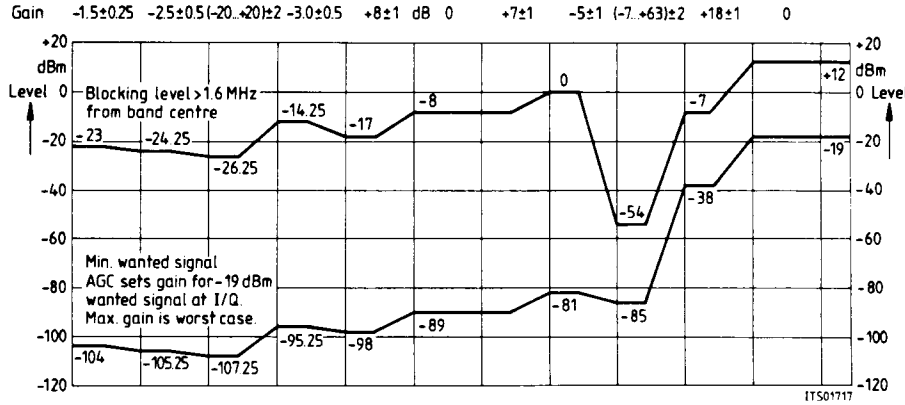


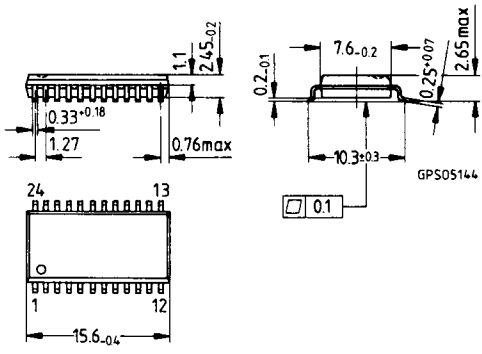
Figure 10
Worst Case Signal Levels with Blocking Level





6 Package Outlines

Miniature Plastic Dual-in-Line Package,
P-DSO-24 (SMD)
(Small Outlines)
24 B 20 DIN 41870 T17



Dimensions in mm
SMD = Surface Mounted Device