PM8903A

3 A step-down monolithic switching regulator

Datasheet – production data

Features

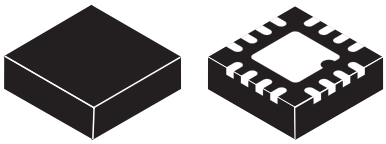
- Integrated 35 mΩ MOSFETs for high efficiency
- 3 A continuous output current
- 2.8 V to 6 V input voltage (V_{IN})
- 2.9 V to 5.5 V supply voltage (V_{CC})
- Adjustable output voltage down to 0.6 V
- 1% output voltage accuracy
- 1.1 MHz switching frequency operation
- PSKIP mode to optimize light load efficiency
- Embedded bootstrap diode
- Thermally compensated loss-less current sense across HS and LS MOSFETs
- OV/UV/OC and overtemperature protection
- Internal soft-start and soft-stop
- Interleaving synchronization (up to 2 ICs)
- Power Good output
- Shutdown function (< 15 µA quiescent current)
- VFQFPN16 3 x 3 mm compact package

Applications

- Subsystem power supply
- CPU, DSP and FPGA power supplies
- Distributed power supply
- General DC-DC converters

Description

The PM8903A is a high efficiency monolithic step-down switching regulator designed to deliver up to 3 A continuous current. The IC operates from 2.8 V to 6 V input voltage (V_{IN}).



VFQFPN16 (3 x 3 mm)

The PM8903A features low-resistance integrated nMOS and proprietary pulse-skipping mode for optimum efficiency over all the loading range.

The voltage mode control loop allows the widest range of output filters. Current sense is internally thermally compensated for optimum precision.

The integrated 0.6 V reference allows the regulation of output voltages with ±1% accuracy over temperature variations. Switching frequency is typically set to 1.1 MHz and can be programmed to 0.8 MHz or 1.0 MHz. Out of phase synchronization allows the reduction of input RMS current.

The PM8903A provides precise dual-threshold overcurrent protection as well as over/undervoltage and overtemperature protection. PGOOD output easily provides real-time information on the output voltage.

The PM8903A is available in VFQFPN16 3 x 3 mm.

Table 1. Device summary

Order codes	Package	Packaging
PM8903A	VFQFPN16 (3 x 3 mm)	Tube
PM8903ATR	VFQFPN16 (3 x 3 mm)	Tape and reel

This is information on a product in full production. www.st.com

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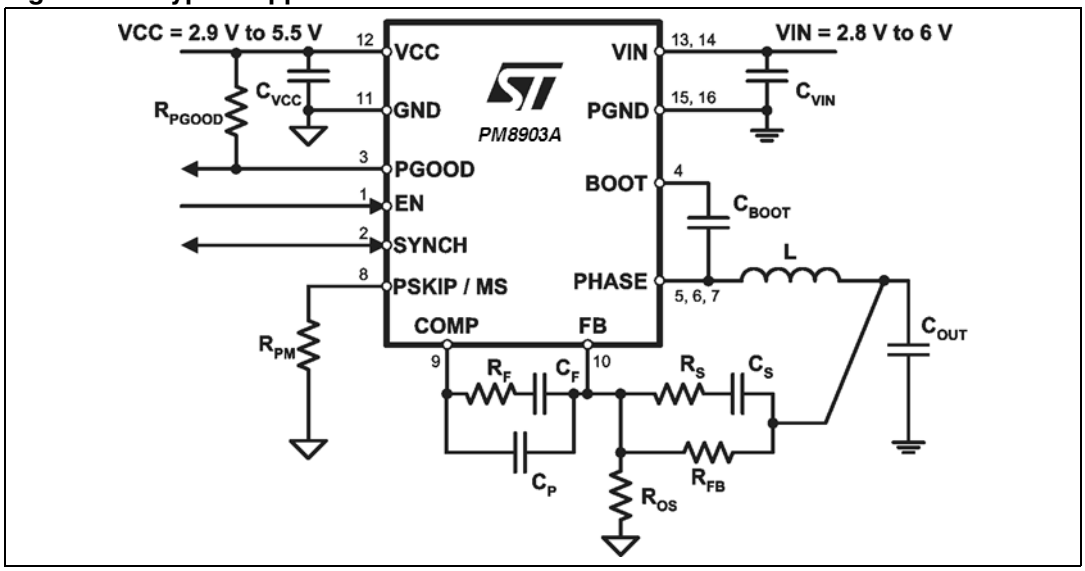
1 Typical application circuit and block diagram

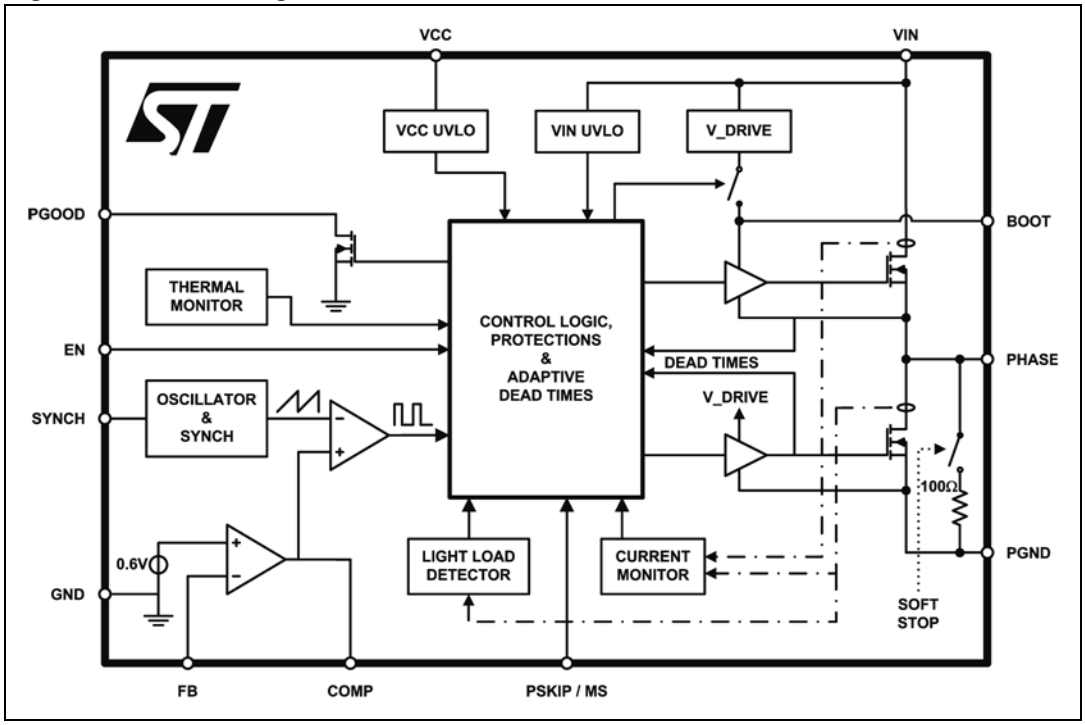
1.1 Application circuit

Figure 1. Typical application circuit



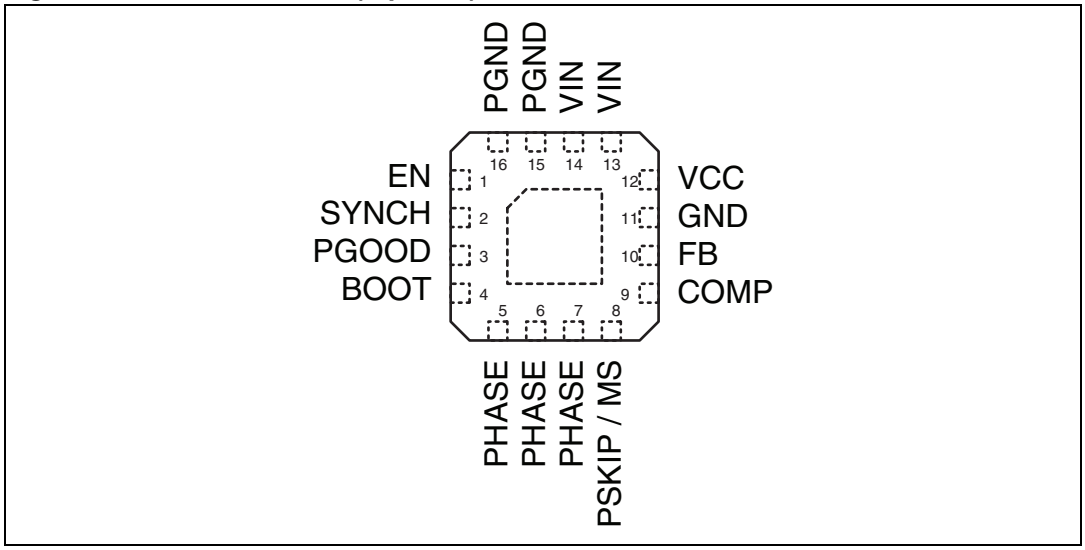
1.2 Block diagram

Figure 2. Block diagram



2 Pin description and connection diagrams

Figure 3. Pin connection (top view)



2.1 Pin description

Table 2. Pin description

Pin #	Name	Function
1	EN	Enable. Internally pulled up by 5 µA to V_{CC}. Force low to disable the device, set free or pull up above turn-on threshold to enable the converter operations.
2	SYNCH	Synchronization pin. According to PSKIP status, the IC sends the synchronization signal out of this pin when master, while accepting a synchronization signal when slave. Connect to the same SYNCH pin of a similar part when synchronizing ICs. In case of single IC operation, leave floating.
3	PGOOD	Open drain output set free after SS has finished and pulled low when V_{OUT} is out of the PGOOD window or any protection is triggered. Pull up to a voltage lower than V_{CC}, if not used it can be left floating.
4	BOOT	Bootstrap pin. It provides power supply for the floating high-side driver. Connect with 0.1 µF to PHASE. See *Figure 1*.
5 to 7	PHASE	Output inductor connection. The pins are connected to the embedded MOSFETs (high-side source and low-side drain). Connect directly to output inductor. See *Figure 1*.
8	PSKIP / MS	Pulse-skip and master/slave definition. Connect with a resistor to GND or leave it floating to define: Pulse-skip feature status; Master/slave for synchronization; Switching frequency. See *Section 5.8 on page 17*.

Table 2. Pin description (continued)

Pin #	Name	Function
9	COMP	Error amplifier output. Connect with an (R_F - C_F) // C_P to FB. See *Figure 1* The device cannot be disabled by pulling low this pin.
10	FB	Error amplifier inverting input. Connect with R_{FB} or R_{FB} // (R_S - C_S) to VSEN and with an (R_F - C_F) // C_P to COMP. A resistor R_{OS} to GND sets the output voltage ratio. See *Figure 1*
11	GND	All the internal references are referred to this pin. Connect to the PCB Signal Ground.
12	VCC	Device power supply. Operative voltage is 2.9 V - 5.5 V. Filter with at least 1 µF MLCC vs. GND.
13, 14	VIN	Power input voltage, connected to embedded high-side drain. Supply range is from 2.8 V to 6 V. Bypass VIN pins to PGND pins close to the IC package with high quality MLCC capacitors (at least 10 µF). See *Figure 1*.
15, 16	PGND	Power ground connection, connected to embedded low-side MOSFET source. Connect to PGND PCB plane. See *Figure 1*.
	Thermal pad	Thermal pad connects the silicon substrate and makes good thermal contact with the PCB. Connect to the PCB PGND plane.

3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-to-ambient (Device soldered on standard demonstration board, see *Section 7* for details)	30	°C/W
R_{thJC}	Thermal resistance junction-to-case	12	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-25 to 125	°C

4 Electrical specifications

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	to PGND, GND	-0.3 to 6	V
V_{IN}	to PGND, GND	-0.3 to 7	V
V_{BOOT}	to PGND, GND to PHASE	-0.3 to 13 -0.3 to 6	V
V_{PHASE}	to PGND, GND to PGND, GND, VIN=6 V, t<100 nsec.	-0.3 to 7 -1.7 to 7.5	V
V_{PGOOD}	to PGND, GND	-0.3 to 7	V
V_{SYNCH}, V_{EN}	to PGND, GND	-0.3 to 6	V
	All other pins to GND	-0.3 to 3.6	V

4.2 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Power supply voltage	2.8	-	6	V
V_{CC}	Signal supply voltage	2.9	-	5.5	V

4.3 Electrical characteristics

$V_{IN} = V_{CC} = 3.3$ V ± 5%, $T_J = 0$ °C to 125 °C, typical values at $T_J = 25$ °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and undervoltage lockout						
I_{IN}	VIN supply current	Switching, no inductor connected		5		mA
I_{CC}	VCC supply current	Switching, no inductor connected		1		mA
$I_{SHUTDOWN}$	VCC + VIN supply current	Shutdown, EN = 0 V		13		µA
VIN UVLO	VIN turn-ON	VIN rising			2.8	V
	Hysteresis			100		mV
	Deglitching(1)	Rising and falling edge		1		µs
VCC UVLO	VCC turn-ON	VCC rising			2.9	V
	Hysteresis			100		mV
	Deglitching(1)	Rising and falling edge		1		µs
Oscillator						
F_{SW}	Main oscillator accuracy	R_{PM}=0 Ω / 24 kΩ / 180 kΩ / 240 kΩ or PSKIP/MS pin floating	0.99	1.1	1.21	MHz
ΔV_{OSC}	PWM ramp amplitude(1)			1		V
d	Duty cycle(1)		0		100	%
T_{ON-min}	Minimum on-time(1)			80		ns
$T_{OFF-min}$	Minimum off-time(1)			80		ns
Reference and error amplifier						
	Output voltage accuracy	VOUT = 0.6 V	-1	-	1	%
A_0	DC gain(1)			120		dB
GBWP	Gain-bandwidth product(1)		14			MHz
SR	Slew-rate(1)	C_{COMP} = 20 pF		5		V/µs
Output power MOSFETS						
HS R_{DS-on}	HS drain-source on-resistance			35		mΩ
LS R_{DS-on}	LS drain-source on-resistance			35		mΩ
Overcurrent protection						
I_{OC1}	1st level overcurrent threshold	HS sourcing	4.0	4.6	5.2	A
I_{OC2}	2nd level overcurrent threshold (1)	HS sourcing	4.5	5.2	5.9	A

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Over and undervoltage protection						
OVP	OVP threshold	FB rising	0.69	0.72	0.75	V
		LS turns off, FB falling		0.30		V
UVP	UVP threshold	FB falling	0.45	0.48	0.51	V
I_{FB}	FB disconnection bias current	Sourced from FB		100		nA
Overtemperature protection						
OTP	Thermal shutdown threshold (1)			140		°C
	Thermal shutdown hysteresis (1)			40		°C
PGOOD						
PGOOD	Upper threshold	FB rising	0.69	0.72	0.75	V
	Lower threshold	FB falling	0.45	0.48	0.51	V
V_{PGOODL}	PGOOD voltage low	I_{PGOOD} = -4 mA			0.4	V
ENABLE						
EN	Input logic high	EN rising			1.5	V
	Input logic low	EN falling	0.65			V
	Hysteresis		150			mV
	Deglitching(1)	Rising and falling edge		3		µs
SS						
T_{SS}	Soft-start time	R_{PM} = 0 Ω / 24 kΩ / 180 kΩ / 240 kΩ or PSKIP/MS pin floating		0.79		ms

1. Guaranteed by design, not subject to test.

4.4 Typical operating characteristics

In the demonstration board, as described in *Section 7.1*, R_{PM} = 0 Ω, V_{IN} = V_{CC} = 3.3 V, VOUT=1V5, T_J = 25 °C, unless otherwise specified.

Figure 4. Efficiency vs. output current - V_{IN} = 3.3 V, R_{PM} = 240 kΩ

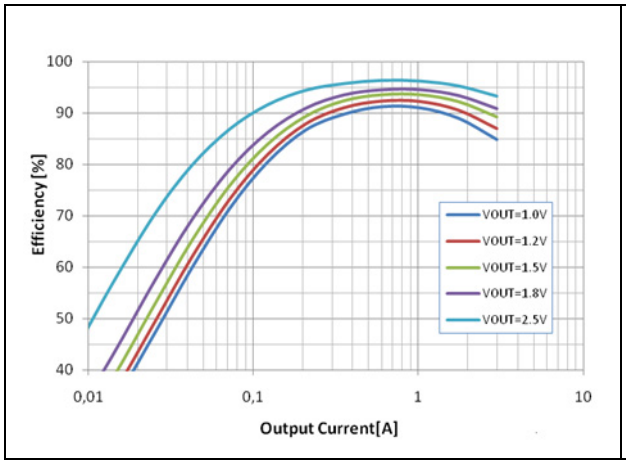


Figure 5. Efficiency vs. output current - V_{IN} = 5 V, R_{PM} = 240 kΩ

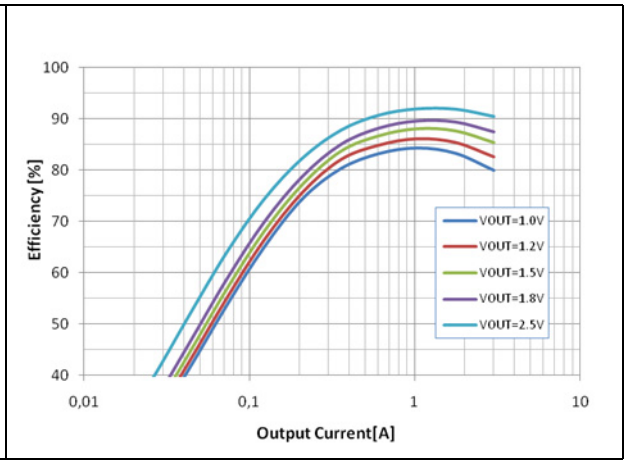


Figure 6. Load regulation - V_{IN} = 3.3 V

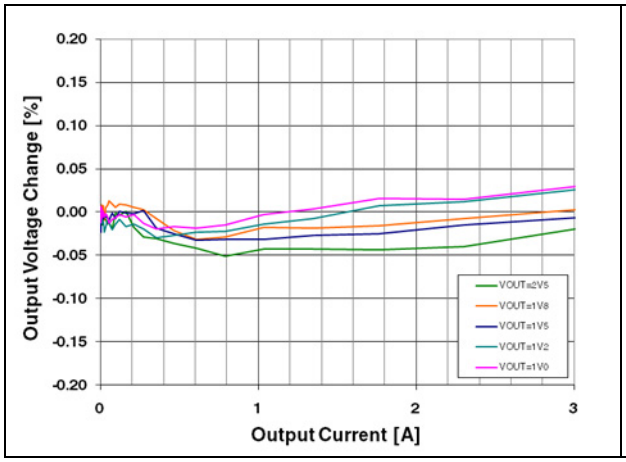


Figure 7. Load regulation - V_{IN} = 5 V

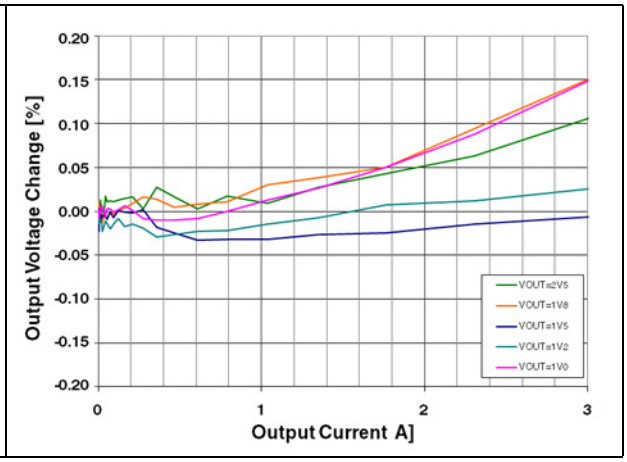
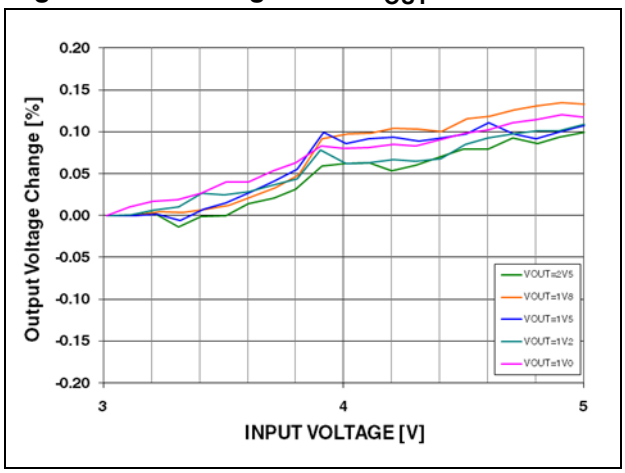


Figure 8. Line regulation - I_{OUT} = 3 A



5 Device description

The PM8903A is a high efficiency synchronous step-down monolithic switching regulator capable of delivering up to 3 A continuous output current.

The power input voltage (V_{IN}) can range from 2.8 V to 6 V, the signal input voltage (V_{CC}) can range from 2.9 V to 5.5 V.

Thanks to the 0.6 V internal reference and 0-100% duty cycle capability, the PM8903A can precisely regulate output voltages ranging from 0.6 V to almost V_{IN} (limited only by minimum T_{OFF} time). The output voltage accuracy is better than ±1% over line, load and temperature.

The PM8903A embeds low $R_{DS(on)}$ (35 mΩ) N-channel MOSFETs for both HS (high-side) and LS (low-side) and implements the proprietary pulse-skipping technology, therefore, the PM8903A guarantees high efficiency over all the load range.

The voltage mode control loop with high bandwidth error amplifier and external compensation enables a wide range of output filter configurations (including all MLCC solutions) and fast response to load transient. The high-switching frequency (typically 1.1 MHz) and the small VFQFPN16 3x3 mm package allow very compact VR solutions.

The PM8903A features a full set of protections and output voltage monitoring:

- Precise and accurate dual level overcurrent protection (internally compensated against temperature variations)
- Over and undervoltage protection
- Overtemperature protection
- Undervoltage lockout on both signal and power supply
- Power Good open drain output easily provides real-time information about the output voltage.

By simply connecting two PM8903As through the SYNCH pin, they can synchronize each other with 180° phase shift switching interleaving, reducing RMS current absorption from the input filter and preventing ‘beating frequency’ noise, therefore allowing the size and cost of the input filter to be reduced.

A simple resistor connected from the PSKIP/MS pin to ground enables/disables pulse-skipping technology and assigns master or slave status to the IC.

The dedicated ENABLE pin (EN) offers easy control on the power sequencing or to reset the latched protection. Forcing the EN low, the device enters shutdown state and absorbs a total quiescent current from V_{CC} and V_{IN} less than 15 µA.

5.1 Power section

The PM8903A integrates two low $R_{DS(on)}$ (35 mΩ) N-channel MOSFETs as low-side and high-side switches, optimized for fast switching transition and high efficiency over all the load range. The power stage is designed to deliver a continuous output current up to 3 A.

The HS MOSFET drain is connected to the VIN pins (power input), the LS MOSFET source is connected to the PGND pins (power ground), and HS MOSFET source and LS MOSFET drain are connected together and to the PHASE pins (see *Figure 2*). The driving section is supplied from the V_{IN} pins through an internal voltage regulator (V_{DRIVE}) that assures the proper driving voltage over all the VIN range.

To properly supply the power section the following is advised:

- Bypass V_{IN} pins to PGND pins as close as possible to the IC package with high quality MLCC capacitors (at least 10 µF).
- Connect the bootstrap capacitor (typically a 100 nF ceramic capacitor rated to stand V_{IN} voltage) from the BOOT pin to the PHASE pin to supply the HS driver.

Caution: Do not connect an external bootstrap diode. The IC already integrates an active bootstrap diode to charge the bootstrap capacitor, saving the cost of this external component.

The PM8903A embodies an anti-shoot-through and adaptive deadtime control to minimize low-side body diode conduction time and consequently reduce power losses:

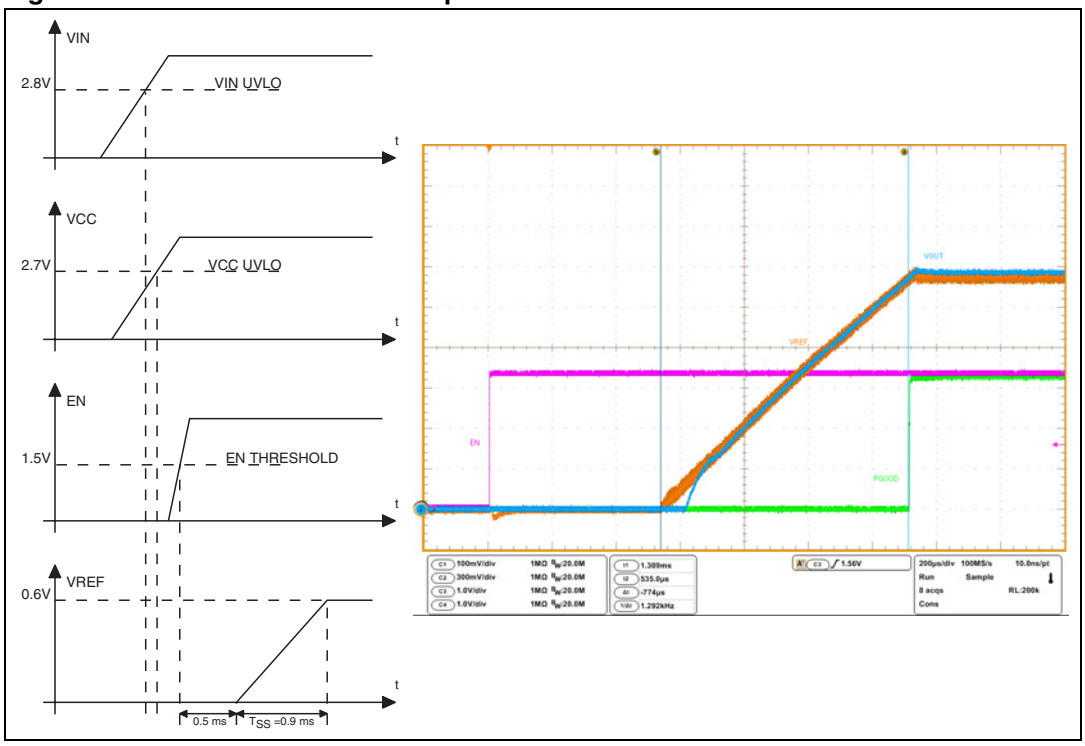
- When the voltage at the PHASE pin drops (to check high-side MOSFET turn-off), the LS MOSFET is suddenly switched on
- When the gate driving voltage of LS drops (to check low-side MOSFET turn-off), the HS MOSFET is suddenly switched on.

If the current flowing in the inductor is negative, voltage on the PHASE pin never drops. A watchdog controller is implemented to allow the LS MOSFET to turn on even in this case, allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative (if pulse-skipping is disabled).

5.2 Startup and shutdown management

The PM8903A monitors the supply voltage on both VCC and VIN pins. Once both VCC and VIN voltages are above the respective UVLO (undervoltage lockout) thresholds and the EN pin is high, the device waits for 0.5 ms (typ.) and then begins the soft-start.

Figure 9. PM8903A soft-start sequence



The PM8903A implements the soft-start by gradually increasing the internal reference from 0 V to 0.6 V in a 1024 switching clock (0.79 ms typ.), linearly charging the output capacitors to the final regulation voltage in closed loop regulation. The soft-start prevents high inrush current from power supply rail.

5.2.1 Low-side-less startup

In order to avoid any kind of negative undershoot and dangerous return from the load during startup, the PM8903A performs a special sequence in enabling the LS driver to switch: during the soft-start phase, the LS driver results disabled (LS = OFF) until the first PWM pulse occurs. This avoids the dangerous negative spike on the output voltage that may happen if starting over a pre-biased output.

As long as the output voltage is biased to a voltage higher than the programmed one, the control loop does not provide the HS pulse that enables LS. In this case LS is enabled at the end of the soft-start time and, if the device is allowed to sink (PSKIP disabled), it discharges the output to the final regulation value.

This particular feature of the device masks the LS turn-on only from the control loop point of view: protection has higher priority and can turn on the LS MOSFET if an overvoltage event is detected.

5.2.2 Soft-off

The PM8903A implements the soft-off sequence turning off both HS and LS MOSFETs and connecting the integrated bleeding resistor (100 Ω) between the PHASE and PGND pin.

When small load currents are applied to the converter, the soft-off sequence allows the discharging of the output voltage within a maximum time (T_{SO}) that depends only on the output capacitance value.

$$T_{SO} = 5 \cdot 100 \cdot C_{OUT}$$

The PM8903A begins the soft-off sequence, and remains in a latched state, if one of the following conditions occurs:

- VCC voltage falls below UVLO threshold
- OVP (overvoltage protection)
- UVP (undervoltage protection)
- OCP (overcurrent protection)
- EN pin is pulled low.

Cycle EN or VCC to recover from latched state with a new soft-start sequence.

5.3 Output voltage monitoring and protection

The PM8903A monitors the output voltage status through the FB pin and compares the voltage on this pin with the internal reference in order to provide over and undervoltage protection as well as PGOOD signal.

5.3.1 Overvoltage protection

Overvoltage protection is active as soon as the device is enabled and both V_{CC} and V_{IN} voltages are above the respective undervoltage lockout levels.

The protection is triggered when the voltage sensed on the FB pin rises over the OVP threshold (0.72 V typ.) and the device acts as follows:

- HS MOSFET is suddenly forced OFF
- LS MOSFET is turned on (to discharge the output and protect the load) until V_{FB} drops to 0.3 V, it is then turned off (to avoid negative spikes on the output voltage). If V_{FB} recrosses OVP rising threshold, LS is turned on again.

This protection state is latched, cycle EN or VCC to recover.

5.3.2 Undervoltage protection

Undervoltage protection is active from the end of soft-start.

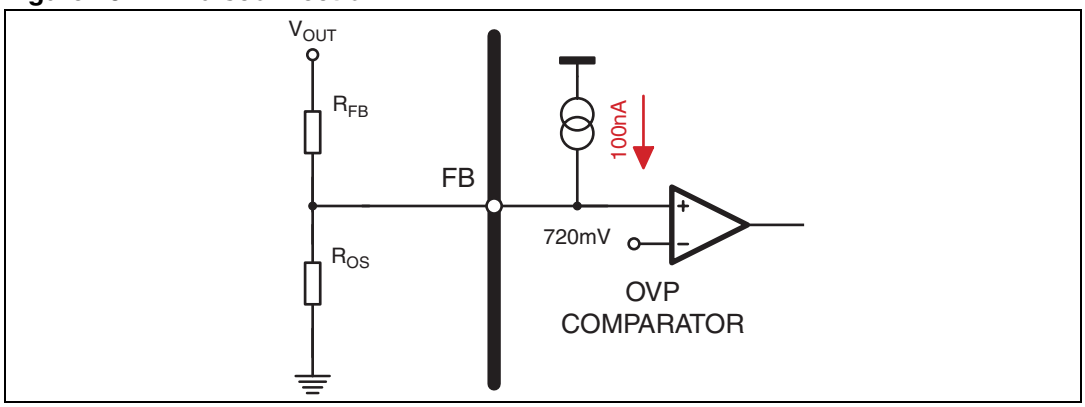
If V_{FB} falls below the UVP threshold (0.48 V typ.), undervoltage protection is triggered and the device starts a soft-off sequence (see *Section 5.2.2*).

This protection state is latched, cycle EN, VCC or VIN to recover.

5.3.3 Feedback disconnection protection

In order to protect the load even if the FB pin is not connected to the PCB, a 100 nA current is constantly sourced from the FB pin: if the FB pin is left floating, it is internally pulled high triggering OVP protection and preventing V_{OUT} from rising out of control.

Figure 10. FB disconnection



5.3.4 Power Good (PGOOD)

PGOOD is an open drain output, left floating when V_{OUT} is in regulation at the programmed voltage, at the end of soft-start.

PGOOD is forced low, to communicate that the output voltage is no longer in regulation, if one of the following conditions is verified:

- The voltage of the FB pin exits from the PGOOD window (±20% of V_{REF})
- The device is disabled, EN is forced low
- VCC voltage is below the UVLO threshold
- Any protection is triggered (OVP, UVP, OCP, OTP).

5.4 Overcurrent protection

Overcurrent protection is active as soon as the device is enabled and both VCC and VIN voltages are above the respective UVLO levels.

The overcurrent function protects the converter from a shorted output or overload by sensing the output current information across the integrated MOSFETs as follows:

- During normal operation the output current information is monitored reading the current flowing in the HS MOSFET
- When the converter is working with an on-time lower than 130 ns (typ.) the current is monitored reading the current flowing in the LS MOSFET.

If the monitored current information is bigger than the overcurrent thresholds, an overcurrent event is detected.

For maximum safety and load protection, the PM8903A implements a dual level overcurrent protection system.

- **First level threshold**

  During a switching cycle, if the monitored current information exceeds a 4.6 A (typ.) threshold, first level overcurrent is detected: the HS MOSFET is turned off and the LS MOSFET is turned on until the next cycle. If four first level OC events are detected in four consecutive switching cycles, overcurrent protection is triggered.

- **Second level threshold**

  If the monitored current information exceeds the 5.2 A (typ.) threshold, overcurrent protection is triggered immediately.

When overcurrent protection is triggered, the device suddenly turns off the HS and keeps the LS turned on until the output current drops to 600 mA, then the device turns off both LS and HS MOSFETs in a latched condition; cycle EN or VCC to recover.

5.5 Overtemperature protection

It is recommended that the device never exceeds the maximum allowable junction temperature. This temperature increase is mainly caused by the total power dissipated from the integrated power MOSFETs.

To avoid any damage to the device when reaching high temperature, the PM8903A implements a thermal shutdown feature: when the junction temperature reaches 140 °C the device turns off both MOSFETs.

When the junction temperature drops to 100 °C, the device restarts with a new soft-start sequence.

5.6 Synchronization

Synchronization of two PM8903As is enabled simply connecting the SYNCH pins of the two devices together. No synchronization is implemented if the SYNCH pin is left floating.

When synchronization is enabled, the first device must be configured as a master and the second device must be configured as a slave. Connect a resistor between the PSKIP/MS pin and ground, and select the resistor value according to *Table 7*, to program the IC to be master or slave.

Caution: Do not connect together the synchronization pin of two master devices in order to avoid any damage to the ICs.

When two PM8903As are synchronized together they act as follows:

- **Master mode**

  The SYNCH pin is configured as clock output. The device provides, on the SYNCH pin, its internal switching clock information with a 180 ° time shifting.

- **Slave mode**

  The SYNCH pin is configured as clock input. The device uses the clock information received on the SYNCH pin to synchronize its internal switching clock.

5.7 Pulse-skipping

The PM8903A implements an ST proprietary adaptive pulse-skipping algorithm which requires no configuration by the user and is independent from application setup and parasites.

The algorithm allows to strongly increase the overall system efficiency skipping some switching cycles (so reducing the equivalent switching frequency of the converter) when the load current is low.

In many applications, MLCCs (multi layer ceramic capacitors) are used as the input or output filter, or both. MLCCs can produce audible noise if the switching frequency is in the human hearing range. To avoid audible noise, the PM8903A pulse-skipping algorithm limits the minimum equivalent switching frequency above the audio band.

Pulse-skipping mode is enabled connecting a resistor between the PSKIP/MS pin and ground, and selects the resistor value according to *Table 7*.

5.8 Multifunction pin PSKIP/MS

With this pin it is possible to:

- Enable/disable the pulse-skipping management
- Assign to the IC master or slave status
- Select the switching frequency.

Connect a resistor (R_{PM}) between the PSKIP/MS pin and GND in order to set the IC functionality according to *Table 7*.

Table 7. PSKIP/MS pin configuration

R_{PM}	Pulse-skipping	Synch mode	Switching frequency
0 Ω	Disabled	Slave	1.1 MHz
24 kΩ	Enabled	Slave	1.1 MHz
56 kΩ	Disabled	Slave	0.8 MHz
110 kΩ	Disabled	Master	1.0 MHz
180 kΩ	Enabled	Master	1.1 MHz
240 kΩ (or pin floating)	Disabled	Master	1.1 MHz

6 Application information

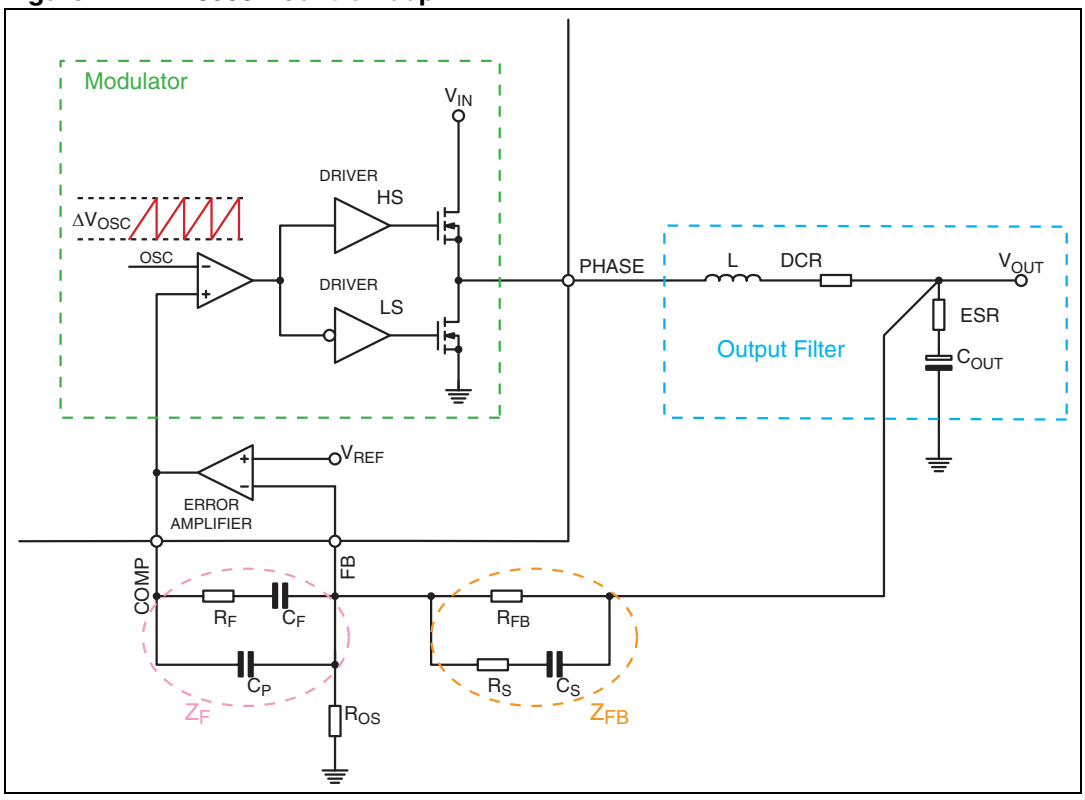
6.1 Compensation network

The PM8903A implements a voltage mode control loop (see *Figure 11*). The output voltage is regulated to the internal reference (offset resistor between FB node and GND can be neglected in control loop calculation).

Error amplifier output is compared with the oscillator sawtooth waveform to provide the PWM signal to the driver section. The PWM signal is then transferred to the switching node with V_{IN} amplitude. This waveform is filtered by the output filter.

The converter transfer function is the small signal transfer function between the output of the EA and V_{OUT}. This function has a double pole at frequency F_{LC} depending on the L-C output filter and a zero at F_{ESR} depending on the output capacitor ESR. The DC gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Figure 11. PM8903A control loop



The compensation network closes the loop joining V_{OUT} and EA output with a transfer function ideally equal to $-Z_F/Z_{FB}$.

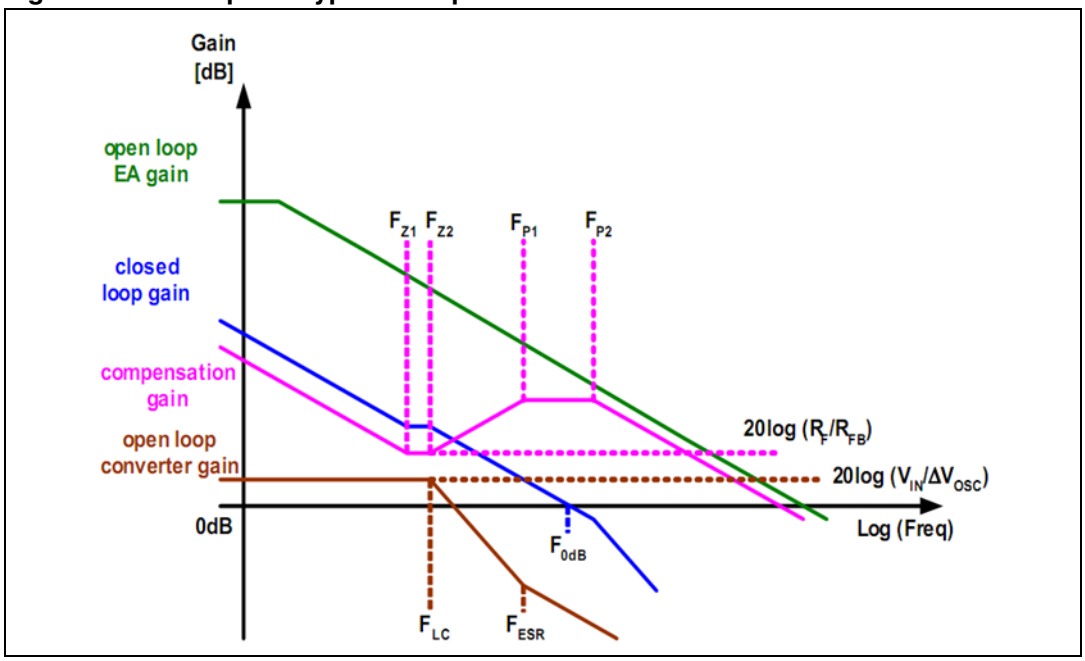
The compensation goal is to close the control loop assuring high DC regulation accuracy, good dynamic performance, and stability. To achieve this, the overall loop needs high DC gain, high bandwidth and good phase margin.

High DC gain is achieved giving an integrator shape to the compensation network transfer function. Loop bandwidth (F_{0dB}) can be fixed choosing the right R_F/R_{FB} ratio, however, for

stability, it should not exceed $F_{SW}/2\pi$. To achieve a good phase margin, the control loop gain must cross the 0 dB axis with -20 dB/decade slope.

For example, *Figure 12* shows an asymptotic bode plot of a type III compensation.

Figure 12. Example of type III compensation



The open loop converter singularities are:

$$F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR}$$

The compensation network singularity frequencies are:

$$F_{Z1} = \frac{1}{2\pi \cdot R_F \cdot C_F}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R_{FB} + R_S) \cdot C_S}$$

$$F_{P1} = \frac{1}{2\pi \cdot R_F \cdot \left(\frac{C_F \cdot C_P}{C_F + C_P}\right)}$$

$$F_{P2} = \frac{1}{2\pi \cdot R_S \cdot C_S}$$

The following suggestions may be followed in order to place the poles and zeroes of the compensation network.

- Select a value for R_{FB} in the range of some kΩ
- Select R_F in order to obtain the desired closed loop regulator bandwidth according to the approximate formula:

$$R_F = \frac{F_{0dB}}{F_{LC}} \cdot \frac{\Delta V_{OSC}}{V_{IN_MAX}} \cdot R_{FB}$$

- Select C_F in order to place F_{Z1} below F_{LC} (typically $0.1*F_{LC}$):

$$C_F = \frac{1}{2\pi \cdot R_F \cdot 0.1 \cdot F_{LC}}$$

- Select C_P in order to place F_{P1} at $0.5*F_{SW}$:

$$C_P = \frac{1}{\pi \cdot R_F \cdot F_{SW}}$$

- Select C_S and R_S in order to place F_{Z2} at F_{LC} and F_{P2} at half of the switching frequency:

$$C_S = \frac{1}{2\pi \cdot R_{FB} \cdot F_{LC}}$$

$$R_S = \frac{1}{\pi \cdot C_S \cdot F_{SW}}$$

- Check that compensation network gain is lower than open loop EA gain before F_{0dB}
- Check phase margin obtained (it should be greater than 45 °)
- Repeat the whole procedure if necessary.

6.2 Output voltage setting

The PM8903A integrates a 0.6 V internal reference (V_{REF}), with a total accuracy of ±1% over line, load, and temperature variations (excluding external resistor divider tolerance, when present).

The output voltage can be easily programmed connecting ROS and RFB resistors as follows (see also *Figure 1 on page 4*).

- Connect pin FB to V_{OUT} through R_{FB} resistor
- Connect pin FB to GND through R_{OS} resistor.

Usually, the R_{FB} resistor is selected in order to obtain the desired closed loop regulator bandwidth (see *Section 6.1* for details) and it is not changed when setting the output voltage.

Therefore, the output voltage setting is easily achieved using the following formula to select the value of the R_{OS} resistor:

$$R_{OS} = R_{FB} \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}}$$

6.3 Inductor design

The inductance value is defined by a compromise between the dynamic response time, the efficiency, the cost, and the size. The inductor must be calculated to maintain the ripple current (ΔI_L) between 20% and 30% of the maximum output current (typ.). The inductance value can be calculated with the following relationship:

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

where F_{SW} is the switching frequency, V_{IN} is the input voltage, and V_{OUT} is the output voltage.

Increasing the value of the inductance reduces the current ripple but, at the same time, increases the converter response time to a dynamic load change. The response time is the time required by the inductor to change its current from the initial to the final value. Until the inductor finishes its charging time, the output current is supplied by the output capacitors. Minimizing the response time can minimize the output capacitance required. If the compensation network is well designed, during a load variation the device is able to set a duty cycle value very different (0% or 100%) from the steady-state one. When this condition is reached, the response time is limited by the time required to change the inductor current.

6.4 Output capacitors

The output capacitors are basic components to define the ripple voltage across the output and for the fast transient response of the power supply. They depend on the output voltage ripple requirements, as well as any output voltage deviation requirement during a load transient.

During steady-state conditions, the output voltage ripple is influenced by both the ESR and the capacitive value of the output capacitors as follows:

$$\Delta V_{OUT_ESR} = \Delta I_L \cdot ESR$$

$$\Delta V_{OUT_C} = \Delta I_L \cdot \frac{1}{8 \cdot C_{OUT} \cdot F_{SW}}$$

where ΔI_L is the inductor current ripple. In particular, the expression that defines ΔV_{OUT_C} takes into consideration the output capacitor charge and discharge as a consequence of the inductor current ripple.

During a load variation, the output capacitor supplies the current to the load or absorbs the current stored in the inductor until the converter reacts. In fact, even if the controller immediately recognizes the load transient and sets the duty cycle at 100% or 0%, the current slope is limited by the inductor value. The output voltage has a drop that, also in this case, depends on the ESR and capacitive charge/discharge as follows:

$$\Delta V_{OUT_ESR} = \Delta I_{OUT} \cdot ESR$$

$$\Delta V_{OUT_C} = \Delta I_{OUT} \cdot \frac{L \cdot \Delta I_{OUT}}{2 \cdot C_{OUT} \cdot \Delta V_L}$$

where ΔV_L is the voltage applied to the inductor during the transient response ($D_{MAX} \cdot V_{IN} - V_{OUT}$ for the load appliance or V_{OUT} for the load removal).

MLCC capacitors have typically low ESR to minimize the ripple but also have low capacitance that does not minimize the voltage deviation during dynamic load variations.

Electrolytic capacitors have a large capacitance to minimize voltage deviation during load transients while they do not show the same ESR values as the MLCC, resulting then in higher ripple voltages.

A mix between an electrolytic and MLCC capacitor can be used to minimize ripple as well as reducing voltage deviation in dynamic mode.

The high bandwidth error amplifier of the PM8903A and external compensation enables a wide range of output filter configurations (including all MLCC solutions) and fast transient response.

6.5 Input capacitors

The input capacitor bank is designed considering, mainly, the input RMS current that depends on the output deliverable current (I_{OUT}) and the duty-cycle (D) for the regulation as follows:

$$I_{rms} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

The equation reaches its maximum value, $I_{OUT}/2$, with D = 0.5. The losses depend on the input capacitor ESR and, in the worst case, are:

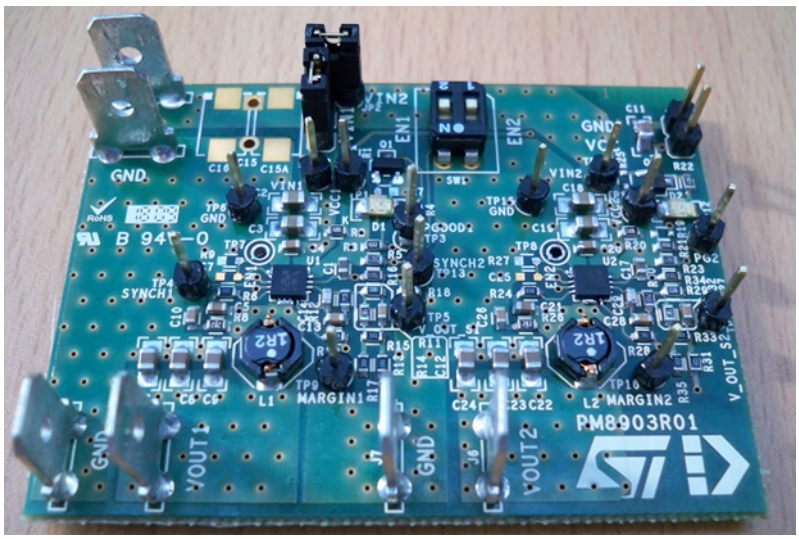
$$P = ESR \cdot (I_{OUT}/2)^2$$

7 PM8903A demonstration board

The PM8903A demonstration board realizes, in a four-layer PCB, a high efficiency synchronous step-down monolithic switching converter capable of delivering up to 3 A continuous output current.

The demonstration board shows the operation of the device in a general purpose application. Two devices are present on the demonstration board and connected through the SYNCH pin, also allowing the testing of the synchronization capability of the PM8903A. The two devices are synchronized to each other with 180° phase shift switching interleaving, reducing RMS current absorption from the input filter and preventing beating frequency noise, therefore allowing a reduction in the size and cost of the input filter.

Figure 13. PM8903A demonstration board



The input voltage (VIN) can range from 2.8 V to 6 V and the supply voltage (VCC) can range from 2.9 V to 5.5 V.

The output voltage is programmed to be 1.5 V but can be easily programmed, changing a single resistor, from 0.6 V to almost V_{IN} with a total accuracy better than ±1% over line, load and temperature.

A simple resistor connected from the PSKIP / MS pin to ground enables / disables pulse-skipping technology and assigns, to the IC, master or slave status.

The dedicated dip switch SW1 allows the enabling / disabling of each device and offers easy control on the power sequencing or to reset latched protection. Forcing EN low, the device enters a shutdown state and absorbs a total quiescent current from VCC and VIN less than 15 µA.

7.1 Detailed demonstration board description

This section describes:

- Demonstration board schematics, see *Figure 14*
- Demonstration board layout, see *Figure 15*
- Demonstration board BOM (bill of materials), see *Table 8*.

Furthermore, the following sub-sections detail how to configure and use the standard demonstration board.

Figure 14. PM8903A demonstration board schematic

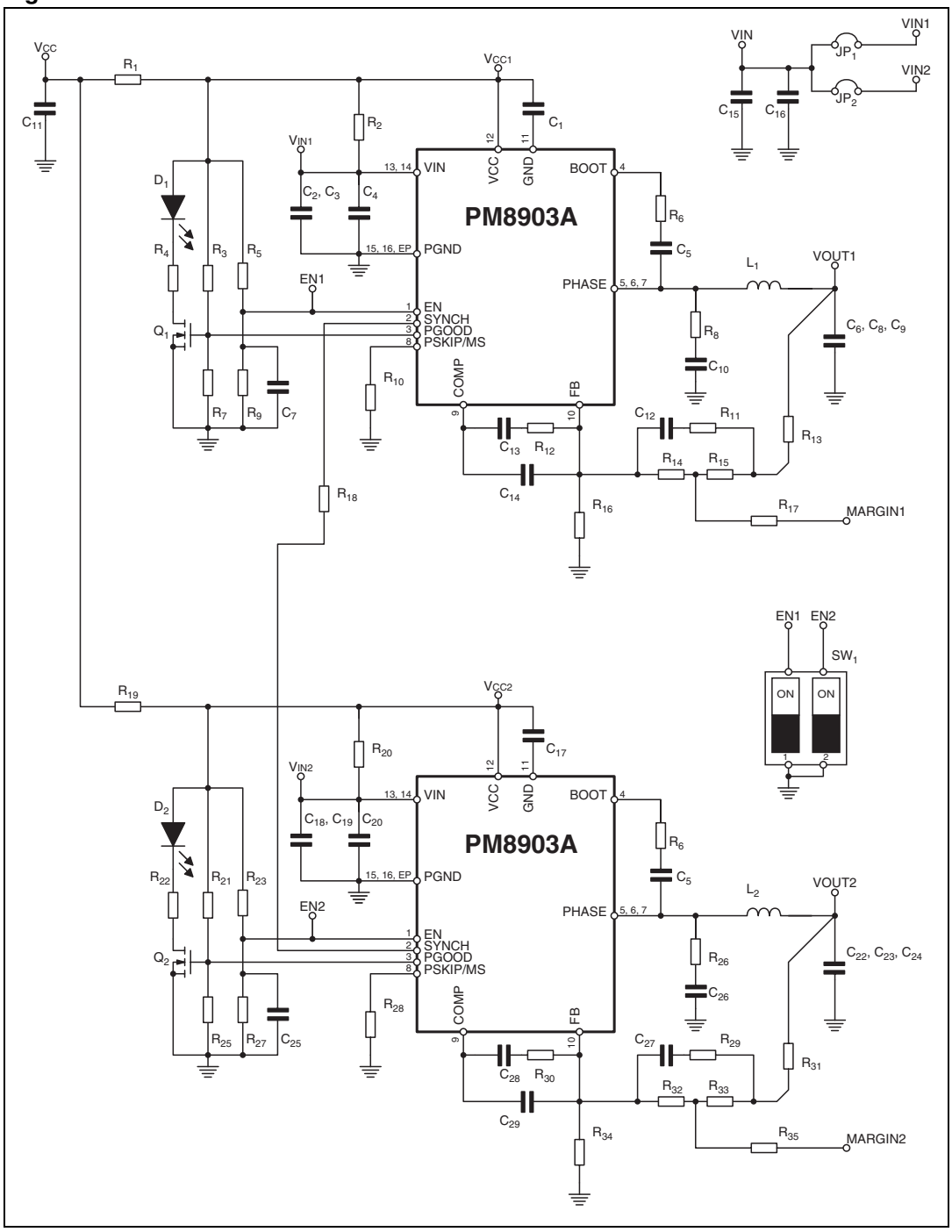


Figure 15. PM8903A demonstration board layout

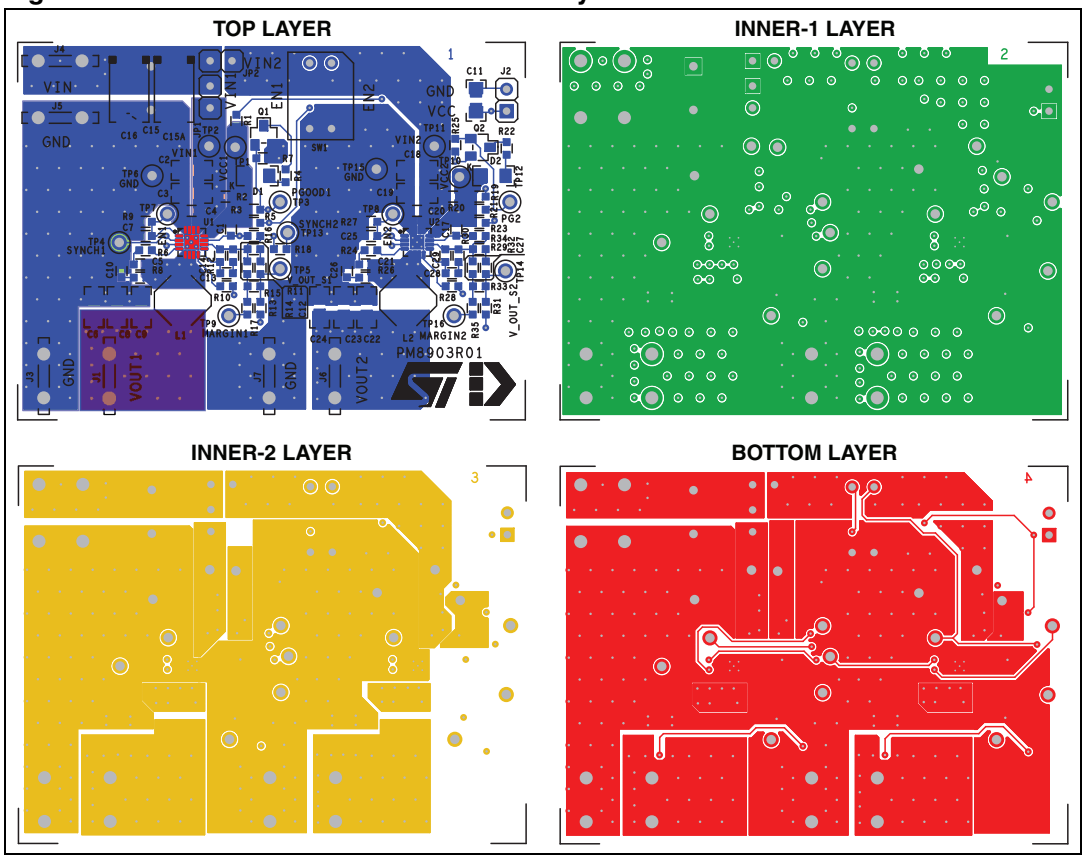


Table 8. PM8903A demonstration board - bill of material

Reference	Alias	Value	Manufacturer P.N.	Package	Supplier
Resistors					
R1, R7, R9, R19, R25, R27		NM		0603	
R2, R20		10 Ω		0603	
R3, R21	$R_{PGOOD(1,2)}$	10 kΩ		0603	
R4, R22		1 kΩ		0603	
R5, R23		560 kΩ		0603	
R6, R24	$R_{BOOT(1,2)}$	0 Ω		0603	
R8, R26	$R_{SNUBBER(1,2)}$	NM		0603	
R10	$R_{PM(1)}$	270 kΩ		0603	
R11, R29	$R_{S(1,2)}$	100 Ω		0603	
R12, R30	$R_{F(1,2)}$	680 Ω		0603	
R13, R17, R18, R31, R35		0 Ω		0603	
R14, R32	$R_{FB1(1,2)}$	0 Ω		0603	

Table 8. PM8903A demonstration board - bill of material (continued)

Reference	Alias	Value	Manufacturer P.N.	Package	Supplier
R15, R33	$R_{FB2(1,2)}$	3.3 kΩ		0603	
R16, R34	$R_{OS(1,2)}$	2.2 kΩ		0603	
R28	$R_{PM(2)}$	0 Ω		0603	
Capacitors					
C1, C17	$C_{VCC(1,2)}$	1 µF, X7R		0603	
C2, C3, C18, C19	$C_{VIN(1,2)}$	22 µF, X5R, 6.3 V, 10% - MLCC	GRM21BR60J226ME	0805	MURATA
C4, C20	$C_{VIN(1,2)}$	100 nF, X7R		0603	
C5, C21	$C_{BOOT(1,2)}$	100 nF, X7R		0603	
C6, C8, C9, C22, C23, C24	$C_{OUT(1,2)}$	10 µF X7R 6.3 V 10% - MLCC	GRM21BR70J106KE	0805	MURATA
C7, C25		NM		0603	
C10, C26	$C_{SNUBBER(1,2)}$	NM		0603	
C11	C_{VCC}	10 µF X7R 6.3 V 10% - MLCC	GRM21BR70J106KE	0805	MURATA
C12, C27	$C_{S(1,2)}$	4.7 nF, X7R		0603	
C13, C28	$C_{F(1,2)}$	22 nF, X7R		0603	
C14, C29	$C_{P(1,2)}$	220 pF, X7R		0603	
C15a, C16	C_{IN}	NM		Case D	
C15	$C_{IN)}$	NM		T.H.M	
Inductors					
L1, L2		1.0 µH, 10.4 mΩ	SPM5030T-1R0M		TDK
Alternative inductors					
L1, L2		1.2 µH, 35 mΩ	H.DI0520-1R2		NEC
		1.2 µH, 25 mΩ	LTF5022T-1R2N4R2-LC		TDK
Active components					
D1, D2		LED			
Q1, Q2		2N7002			STM
U1, U2		PM8903A			STM

7.1.1 Power input (V_{IN})

Connect a power supply to connectors J4(VIN) and J5(GND) on the demonstration board to provide voltage on the power input pins of both devices. Input voltage can range from 2.8 V to 6 V bus.

If the voltage is between 2.9 V and 5.5 V, it can also supply the signal input pins of both devices (through the V_{CC} pin). In this case, make sure that resistors R2/R20 are NM (not mounted) and mount 0 Ω resistors on R1/R19 locations.

7.1.2 Signal input (V_{CC})

The controller is usually supplied separately from the power stage through the V_{CC} input pins.

Connect a power supply to connector J2 (pin one is VC and pin two is GND) on the demonstration board to provide voltage on the signal input pins of both devices. Supply voltage can range from 2.9 V to 5.5 V.

7.1.3 Output (V_{OUT})

On the standard demonstration board, the output voltage is programmed to be 1.5 V, but it can be easily changed mounting one of the values suggested in *Table 9*.

Select the R_{OS} (R16/R34) resistor value with the following formula in order to program a custom value for the output voltage of each device.

$$R_{OS} = R_{FB} \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}}$$

where:

- V_{OUT} is the desiderated output voltage
- V_{REF} is the internal voltage reference (0.6 V)
- R_{FB} resistor, on the demonstration board, is the sum of two resistors (R14/R15 for device U1 and R32/R33 for device U2) and has a total value of 3.3 kΩ.

Table 9. Typical R_{OS} resistors (R16/R34)

Programmed output voltage	Resistor value
0.6 V	NM
0.8 V	10 kΩ
1.0 V	4.9 kΩ
1.2 V	3.3 kΩ
1.5 V	2.2 kΩ
1.8 V	1.65 kΩ
2.5 V	1 kΩ

7.1.4 Test points and jumper connection

Use the following test points in order to measure the most important signals of the PM8903A.

- VCC1 / VCC2: monitor the supply voltages
- VIN1 / VIN2: monitor the input voltages
- V_OUT_S1 / V_OUT_S2: monitor the output voltages (use these test points to perform efficiency load-line regulation measurements)
- PGOOD1 / PGOOD2: (active high) monitor the regular functioning of the controllers
- SYNCH1 / SYNCH2: these are usually shorted when two devices are synchronized together.

Unplug jumpers JP1 /JP2 in order to remove the power input voltage from device U1, device U2, or both. Provide power supply voltage to one device at a time when performing efficiency tests.

Turn on Dip-Switch SW1 in order to disable device U1, device U2, or both.

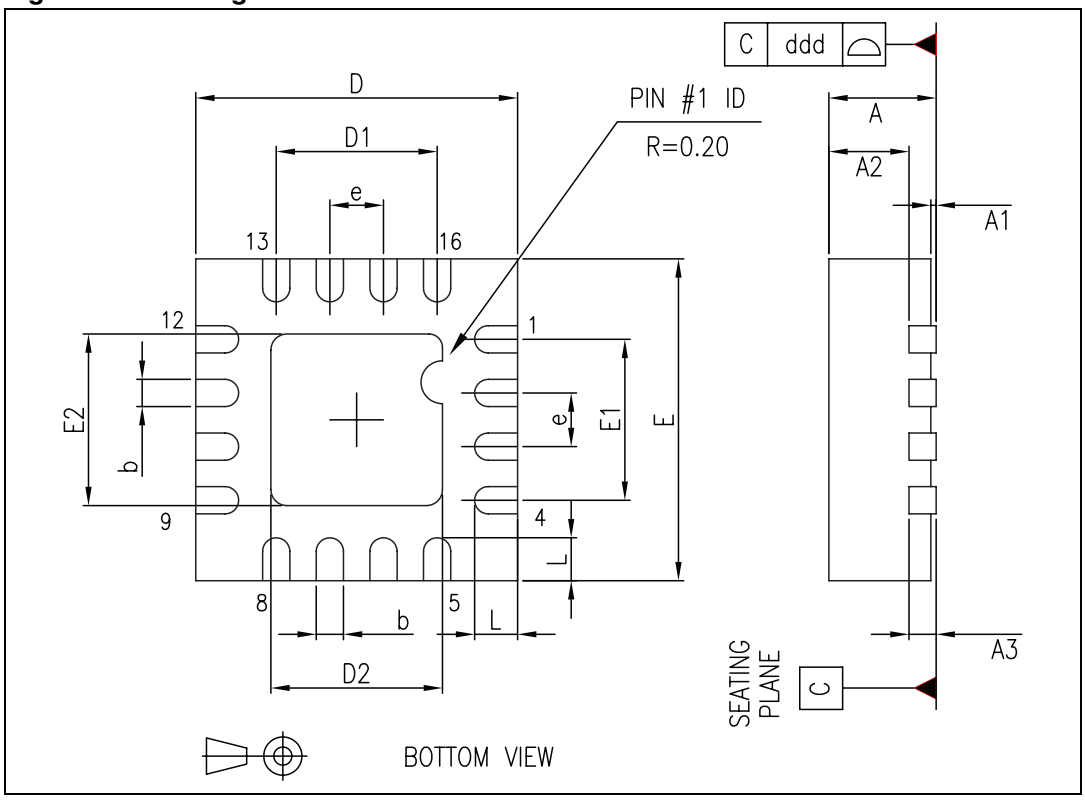
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 10. VFQFPN16 3 x 3 x 1.0 mm mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.20	
b	0.18	0.25	0.30
D	2.85	3.00	3.15
D1		1.50	
D2			1.60
E	2.85	3.00	3.15
E1		1.50	
E2			1.60
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd			0.08

Figure 16. Package dimensions



9 Revision history

Table 11. Document revision history

Date	Revision	Changes
11-Jan-2013	1	First release

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