PM8324 TEMAP 84FDL

High Density T1/E1 Framer with Integrated VT/TU Mappers and M13 Muxes

Released Product Brief

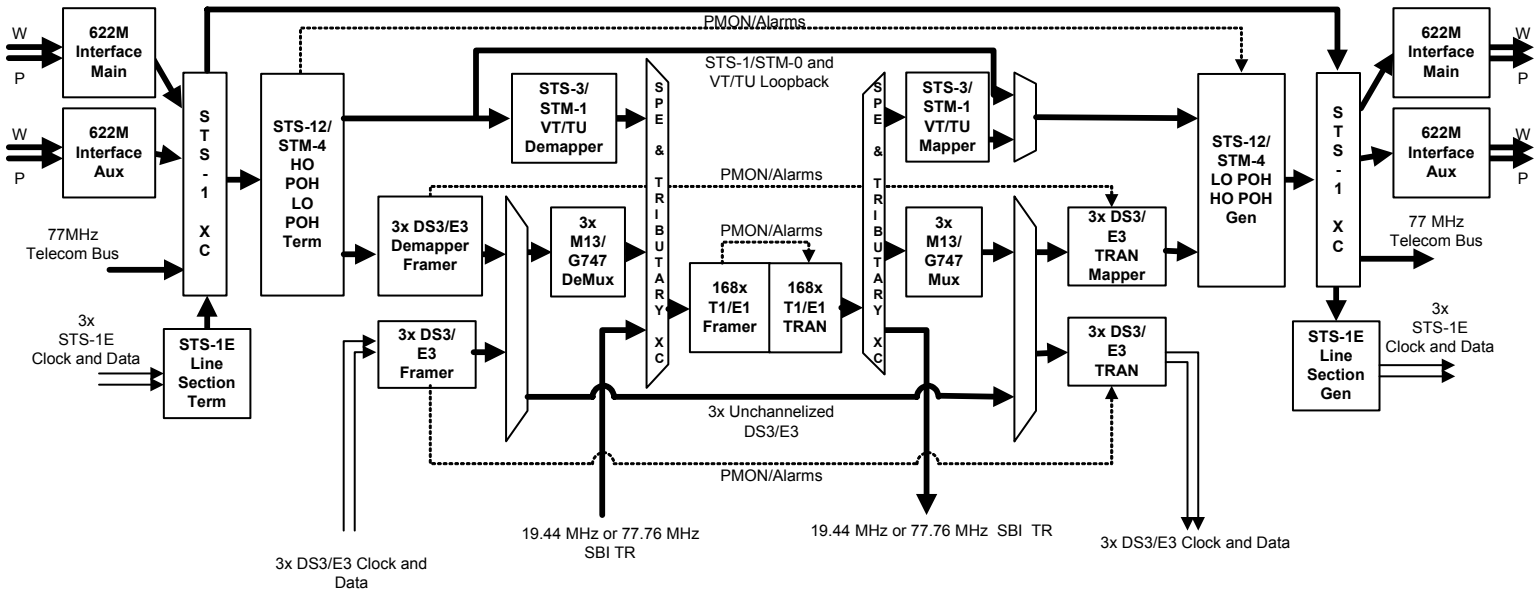
Product Overview

The PM8324 TEMAP 84FDL is a high density T1/E1 framer with integrated VT/TU mappers and M13 multiplexers. This feature-rich device is ideally suited for applications performing high-density transport or termination of channelized DS3 or unchannelized DS3, E3, T1, or E1 over existing SONET/SDH facilities.

Product Highlights

- Processes 84 T1s/63 E1s or an STS-3/STM-1
- Integrates SONET/SDH and DS3/E3 functionality as well as 84 T1/63 E1 bidirectional PMON-capable transceivers:
  - SONET/SDH functions include high order path processing, low order path processing, T1/E1 to VT/TU mapping, and DS3/E3 to AU-3/TU-3 mapping
  - DS3/E3 functions include three DS3/E3 bidirectional PMON-capable transceivers and three M13 multiplexers
- Line side interfaces include:
  - A 77.76 MHz byte wide parallel TelecomBus supporting an STS-12/STM-4
  - Two Working and two Protect 622 MHz serial TelecomBus interfaces supporting a full STS-12/STM-4 of traffic
  - Three serial DS3/E3/EC-1 links
- System side interface is a 19.44 MHz or 77.76 MHz byte serial SBI TR bus used to connect T1/E1 line interface units
- Provides an input and output STS-1 level cross-connect to groom incoming and outgoing data streams
- Provides a serial interface for extracting and inserting the low order path and the high order path
- Supports bit asynchronous mapping of T1/E1 tributaries into SONET/SDH
- Generates and terminates Low Order Path overhead (V5, J2, Z6, Z7 bytes)
- Provides Full Duplex performance monitoring for T1, E1, DS3, and E3 tributaries provided for add and drop directions
- Supports inband error reporting by updating the REI, RDI, and auxiliary RDI bits in the V5 byte (G1 byte for TU-3) with the status of the received tributary
- Supports M13 and C-bit parity DS3 formats
- Provides High Order Path overhead (J1, B3, C2, G1 bytes) processing and the corresponding errors and indications
- Each T1 transceiver can be independently configured to support the common DS1 signal formats (with full SF/ESF support or partial SLC®96 support) or bypassed (unframed mode)
- Provides in-line DS3/E3 and T1/E1 framers and transmitters for each data path allowing true bi-directional performance monitoring of each path
- Each T1 transceiver:
  - Detects the presence of Yellow and AIS patterns
  - Integrates Yellow, Red, and AIS alarms
  - Supports ingress performance monitoring, ESF bit-oriented codes, HDLC messages on the ESF data link, inband loopback codes, and PRBS generation/detection

Block Diagram



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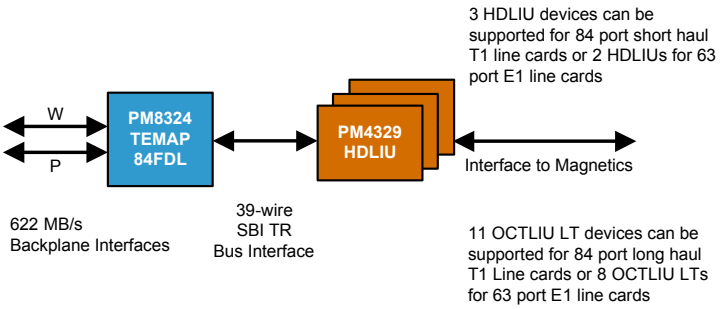
- Each E1 transceiver:
  - Detects the presence of remote alarm and AIS patterns
  - Integrates Red and AIS alarms
  - Supports ingress performance monitoring, support for HDLC messages in the National Use bits, Sa-bit codewords, and V5.2 link ID detection
- Contains desynchronizers and jitter attenuators (JATs) that provide Jitter and Wander compliant E1, T1, DS3, and E3 physical interfaces without the need for external jitter attenuators
- Provides an input and output T1/E1 tributary cross-connect to allow switching of tributaries between the VT/TU mapper, M13 multiplexer and SBI TR bus

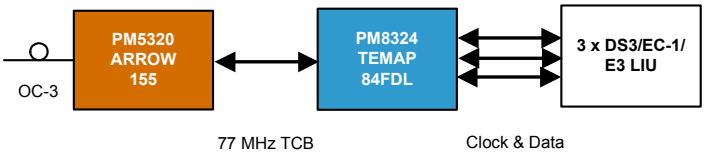
Applications

- Long Haul T1/E1 Line Cards
- Short Haul T1/E1 Line Cards

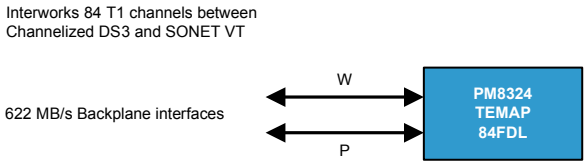
T1/E1 Line Card



3-Port DS3/E3/EC-1/Transmux Line Card



Portless Transmux



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