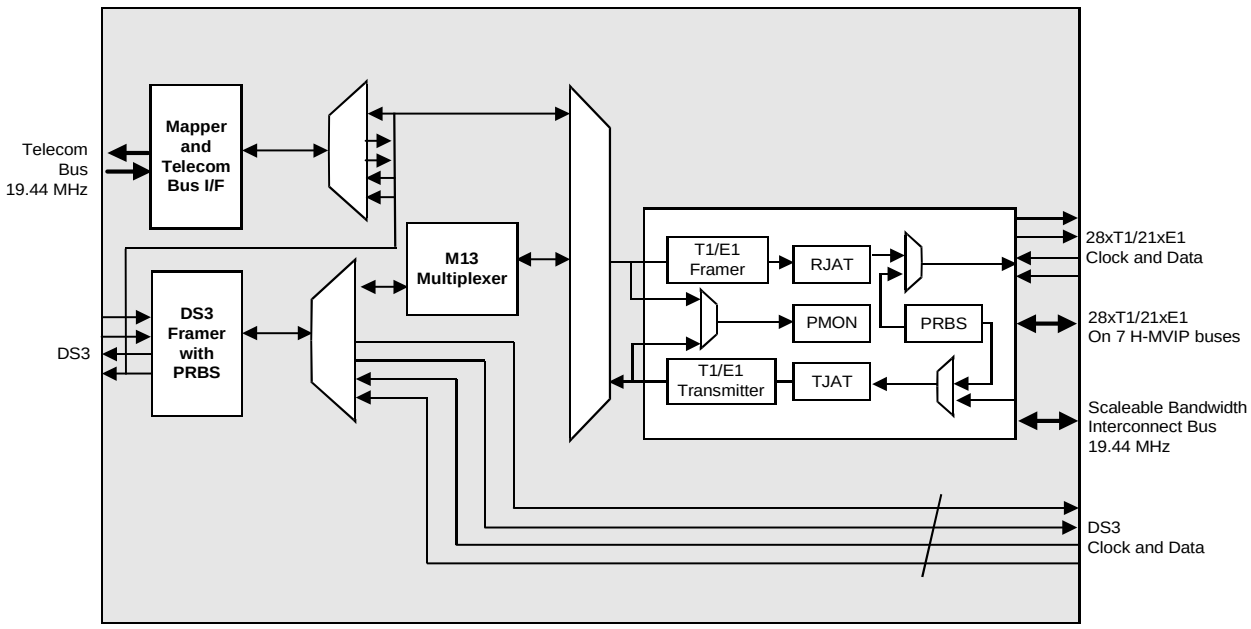
High Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Mux

FEATURES

- Monolithic device which integrates 28 T1 framers, 21 E1 framers, a SONET/SDH VT1.5/V2/TU-11/TU-12 bit asynchronous mapper, a full featured M13 multiplexer with DS-3 framer, and a SONET/SDH DS-3 mapper for terminating DS-3 multiplexed T1 streams, SONET/SDH mapped T1 streams or SONET/SDH mapped E1 streams.
- Seven T1 modes of operation:
  1. Up to 28 T1 streams mapped as bit asynchronous VT1.5 virtual tributaries into a STS-1 SPE or TU-11 tributary units into a STM-1/VC3 or TUG3 from a STM-1/VC4.
  2. Single STS-1, AU3 or TUG3 Bit Asynchronous VT1.5 or TU-11 Mapper with ingress or egress link monitoring per T1 tributary.
  3. Up to 28 T1 streams M13 multiplexed into a serial DS-3.
  4. Up to 28 T1 streams M13 multiplexed into a DS-3; the DS-3 is asynchronously mapped into a STS-1/STM-2/STM-0 SPE.
  5. DS-3 M13 Multiplexer with ingress or egress link monitoring per T1 tributary.
  6. Up to 28 DS-3 multiplexed T1 streams are mapped as bit asynchronous VT1.5 virtual tributaries or TU-11 tributary units, providing a transmultiplexing function between DS-3 and SONET/SDH.
  7. Up to 21 T1 streams mapped as bit asynchronous VT2 virtual tributaries into a STS-1 SPE or TU-12 tributary units into a STM-1/VC3 or TUG3 from a STM-1/VC4.
- Two E1 modes of operation:
  1. Up to 21 E1 streams mapped as bit asynchrounous VT2 virtual tributaries into a STS-1 SPE or TU-12 tributary units into a STM-1/VC3 or TUG3 from a STM-1/VC4.
  2. Single STS-1, AU3 or TUG3 Bit Asynchronous VT2 or TU-12 Mapper with ingress or egress per tributary link monitoring.
- Supports a byte serial Scalable Bandwidth Interconnect (SBI™) bus interface for high density system side device interconnection of up to 84 T1 streams, 63 E1 streams, three DS-3 streams or three E3 streams.
- Up to 28 VT1.5/TU-11 or 21 VT2/TU-12 tributaries can be passed as transparent virtual tributaries (with pointer processing) between the SONET/SDH TelecomBus on the line side and the SBI bus on the system side.
- Supports transfer of PCM data to/from 1.544 MHz and 2.048 MHz system-side devices. Also supports a fractional T1 or E1 system interface with independent ingress/egress Nx64 Kb/s rates. Supports a 2.048 MHz system-side interface for T1 mode without external clock gapping.
- Supports 8 Mb/s MVIP on the system interface for all T1 or E1 links, a separate 8 Mb/s MVIP system interface for all T1 or E1 CAS channels and a separate 8 Mb/s MVIP system interface for all T1 or E1 CCS and V5.1/V5.2 channels.
- Supports the M23 and C-bit parity DS-3 formats.
- Supports stand-alone unchannelized DS-3 framer mode for access to the entire DS-3 payload. When configured to operate as a DS-3 Framer, gapped transmit and receive clocks can be optionally generated for interface to link layer devices which only need access to payload data bits.
- Provides an on-board programmable binary pseudo-random sequence generator and detector for error testing at DS-3 rates and an on-board pseudo-random binary sequence generator and detector on each tributary for error testing at DS1, E1 or N*DS0 rates.

BLOCK DIAGRAM



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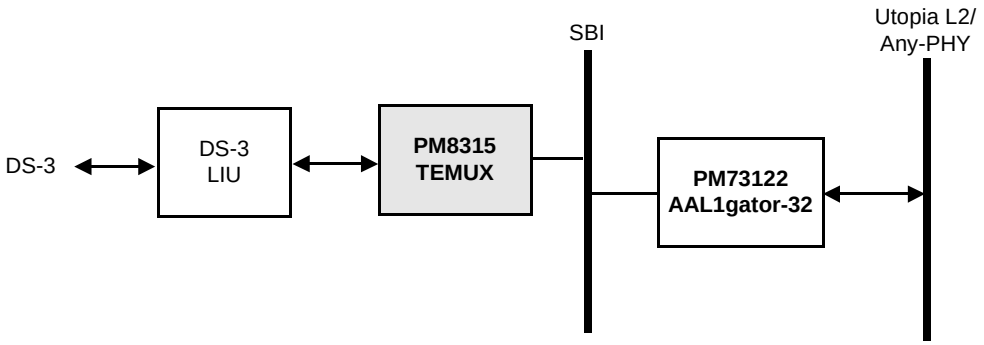
- Supports IEEE P1149.1 JTAG test port.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power +2.5/3.3 V CMOS technology.
- Available in a high density 324-pin PBGA (23 mm by 23 mm) package.
- -40 ^{O}C to +85 ^{O}C Industrial temperature operation.

APPLICATIONS

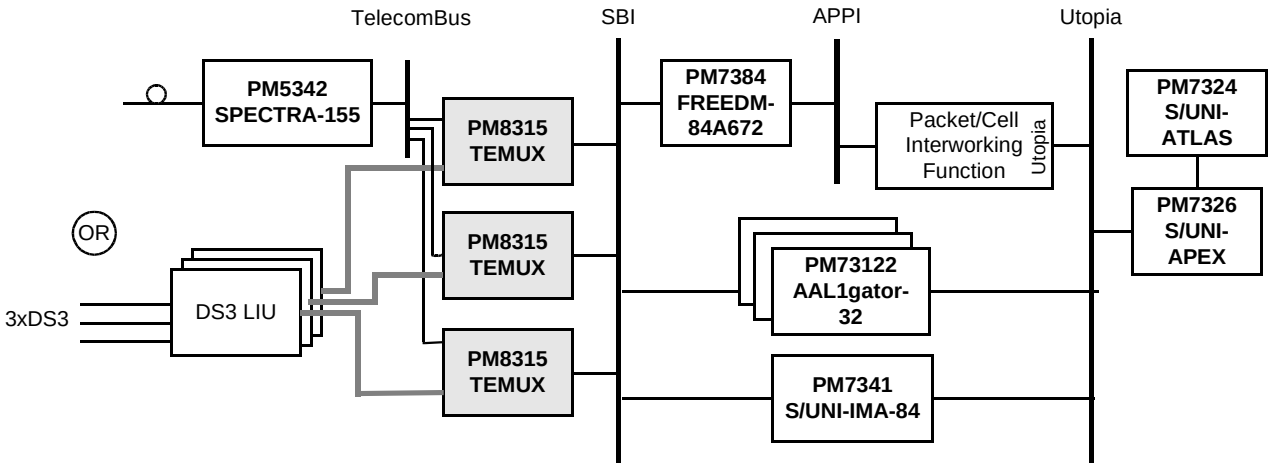
- Channelized and Unchannelized DS-3 Internet interfaces for Remote Access Concentrators, Routers and Switches.
- Channelized and Unchannelized DS-3 Frame Relay Interfaces.
- M13 Mux/Demux Equipment.
- SONET-SDH Add/Drop and Terminal Multiplexers.
- Integrated Services Platform.

TYPICAL APPLICATIONS

STRUCTURED CIRCUIT EMULATION APPLICATION



MULTISERVICE APPLICATION



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