PM8312 TEMUX 32

High-Density 32-Channel T1/E1/J1 Framer with Integrated VT/TU Mapper & M13 Multiplexer

Released
Product Brief

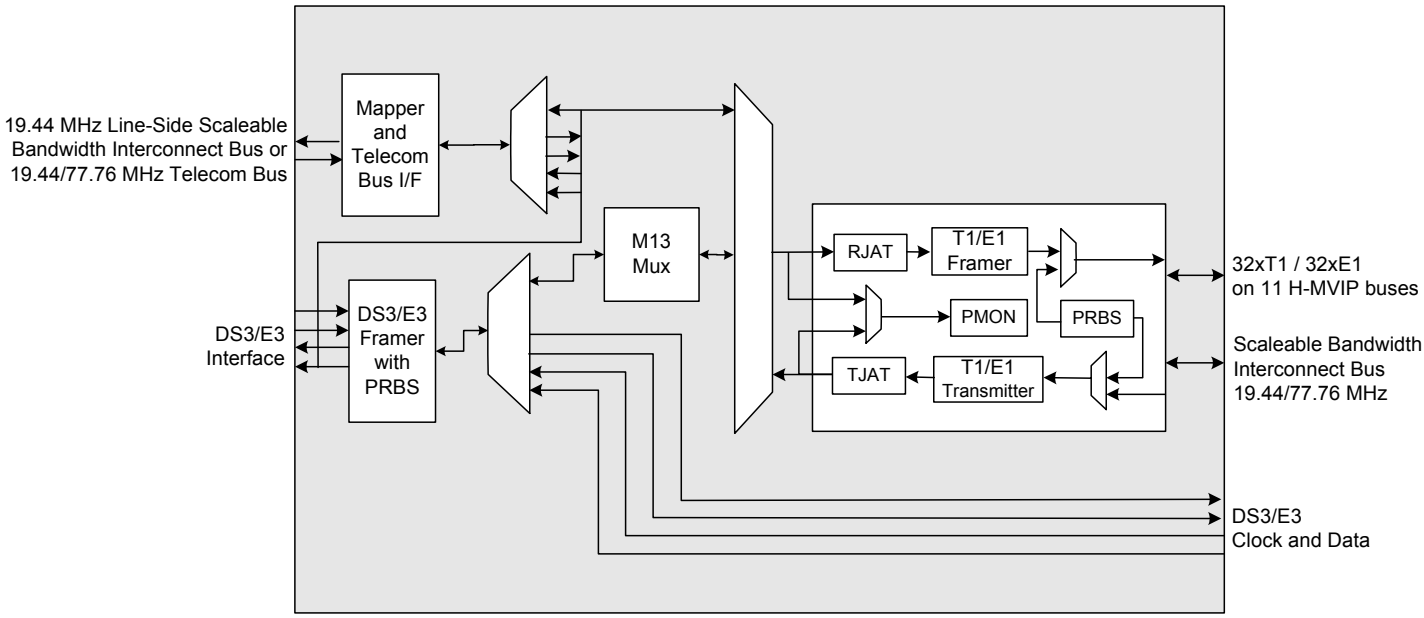
PRODUCT OVERVIEW

The PM8312 TEMUX 32 device is a 64-Mbit/s multi-channel T1/E1 framer with an integrated VT/TU Mapper and M13 Multiplexer.

PRODUCT HIGHLIGHTS

- This monolithic device integrates:
  - 32 T1 framers.
  - 32 E1 framers.
  - One SONET/SDH VT1.5/VT2/TU11/TU12 bit asynchronous or byte synchronous mapper.
  - One full-featured M13 multiplexer with DS3 framer.
  - One SONET/SDH DS3 mapper for terminating unchannelized DS-3 or DS3-multiplexed T1/E1 streams.
- Supports a wide range of T1, E1 and J1 framing formats.
- Supports DS3 framing modes such as M23, C-bit parity, and ITU-T Recommendation G.747.
- Stand-alone unchannelized E3 framer mode (ITU-T Rec. G.751 or G.832) for access to the entire E3 payload.
- Flexible line-side and system-side interface support:
  - Supports a 19.44-MHz Scaleable Bandwidth Interconnect (SBI™) Interface for high-density line-side device interconnection to PMC-Sierra's T1/E1 line interface products, including the 8-port PM4323 OCTLIU LT and the 32-port PM4329 HDLIU.
  - Provides a 19.44 or 77.76 MHz SONET/SDH Add/Drop Telecom bus interface for seamless connection with PMC-Sierra's SONET/SDH devices.
  - Supports a byte-serial Scaleable Bandwidth Interconnect (SBI) interface at 19.44 MHz or 77.76 MHz for high-density system-side device interconnection to PMC-Sierra's link layer products.
  - Supports 8 Mbit/s H-MVIP system interface for all T1 or E1 links, a separate 8 Mbit/s H-MVIP system interface for all T1/E1 CAS channels, and a separate 8 Mbit/s H-MVIP system interface for all T1 or E1 CCS and V5.1/V5.2 channels.
  - Supports 28 T1 or 21 E1 links in DS3 mode and up to 32 T1 or E1 links when using the line-side SBI interface or SONET/SDH mode.
  - Supports transparent virtual tributaries when the SBI interface is used with a SONET/SDH mapper.
  - Supports insertion and extraction of arbitrary rate (e.g. fractional DS3) data streams to and from the SBI bus interface.

BLOCK DIAGRAM



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- Provides jitter attenuation in the T1/E1 tributary receive and transmit directions.
- Provides three independent de-jittered T1 or E1 recovered clocks for system timing and redundancy.
- Provides per-link diagnostic and line loopbacks.
- Provides PRBS generators and detectors at DS3 and E3 rates, and on each tributary for error testing at T1, E1 and NxDS0 rates as recommended in ITU-T 0.151, 0.152.
- Provides a generic eight-bit microprocessor bus interface for configuration, control and status monitoring.
- Provides a standard five-signal P1149.1 JTAG test port for boundary scan board test purposes.
- Feature-rich functional software drivers available with device.

VOLTAGE

- Low power 1.8 V/3.3 V CMOS technology. All pins are 5 V tolerant.

PACKAGE

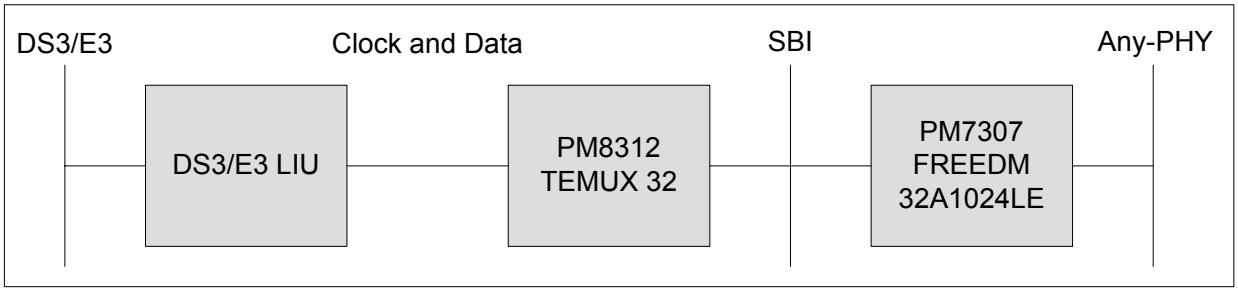
- 324-pin fine pitch PBGA package (23 mm x 23 mm).
- Supports industrial temperature range (-40 °C to 85 °C) operation.

APPLICATIONS

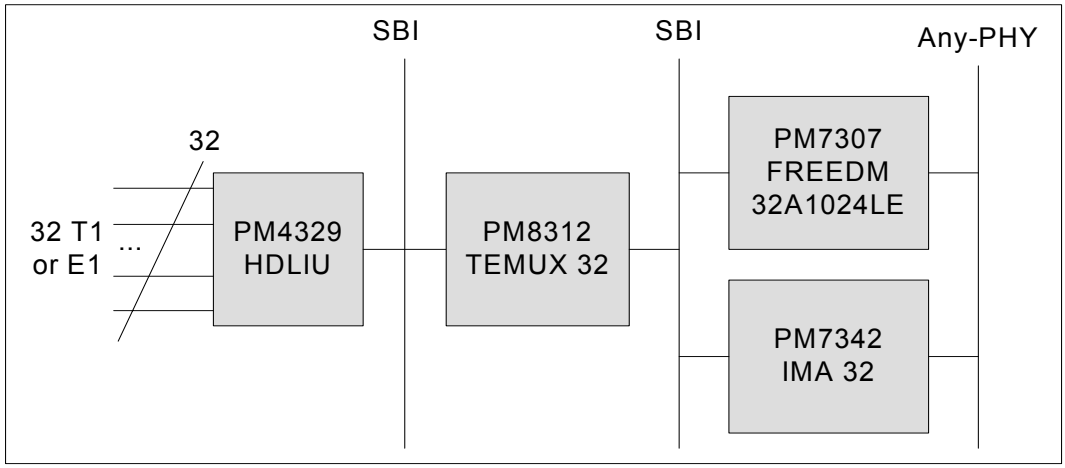
- Wireless Base Station Controllers or Radio Network Controllers
- Wireless Base Stations or 3G Node Bs
- Voice and Media Gateways
- Access and Edge Routers
- Multi-Service Switches
- Mult-Service Edge Aggregation Equipment
- Multi-Service Provisioning Platforms
- xDSL and FTTx Uplink Cards

TYPICAL APPLICATIONS

Channelized T3 Line Card



Wireless Radio Network Controller or Multiservice Edge Aggregation Line Card



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