PM7345

S/UNI-PDH™

S/UNI-PDH

SATURN USER-NETWORK INTERFACE FOR ATM PLESIOCHRONOUS DIGITAL HIERARCHY DATACOM

DATA SHEET

ISSUE 6: JUNE 1998

PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
6	June 1998	Data Sheet Reformatted — No Change in Technical Content. Generated R6 data sheet from PMC-930818, R9

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1 FEATURES

- Implements the ATM Direct Cell Mapping into DS1, DS3, E1, E3 transmission systems according to ITU-T Draft Recommendation G.804.
- Implements the Physical Layer Convergence Protocol (PLCP) for DS1 and DS3 transmission systems according to the ATM Forum User Network Interface Specification and ANSI TA-TSY-000773, TA-TSY-000772, and E1 and E3 transmission systems according to the ETSI Draft Standards T/NA(91)17, and T/NA(91)18.
- Implements the ATM physical layer for Broadband ISDN according to ITU-T Recommendation I.432.
- Provides on-chip DS3 and E3 (G.751 and G.832) framers.
- Directly interfaces to available E3/DS3 line interface units.
- Uses the PMC-Sierra PM4341 T1XC, PM6341 E1XC, and PM4351 COMET framer/line interface chips for DS1 and E1 applications.
- Provides support for an arbitrary rate external transmission system interface up to a maximum rate of 52 Mbit/s.
- Support is provided for SMDS and ATM mappings into various rate transmission systems as defined below, as well as supporting the evolving mappings defined in G.804:

Rate	Format	SMDS PLCP mapping	ATM Direct mapping
45 MHz	C-bit	√	√
	M23	√	√
34 MHz	G.751	√	√
	G.832		√
2 MHz	CRC-4	√	√
	PCM30	√	√
1.5 MHz	ESF	√	√
	SF	√	√



Evolving through G.804

SMDS PLCP mapping	ATM Direct mapping
√	√
	√
	√
	√

- Provides an 8-bit microprocessor interface for configuration, control and status monitoring.
- Low power CMOS technology.

- Available in a high density 100-pin PQFP package, or in an 84-pin PLCC package which is pin-compatible with the PMC-Sierra PM7321 PLPP standard product.

The receiver section:

- Provides frame synchronization for the M23 or C-bit parity DS3 applications, alarm detection, and accumulates line code violations, framing errors, parity errors, path parity errors and FEBE events. In addition, far end alarm channel codes are detected, and an integral HDLC receiver is provided to terminate the path maintenance data link.

- Provides frame synchronization for the G.751 or G.832 E3 applications, alarm detection, and accumulates line code violations, framing errors, parity errors, and FEBE events. In addition, in G.832, the Trail Trace is detected, and an integral HDLC receiver is provided to terminate either the Network Requirement or the General Purpose data link.

- Provides frame synchronization, path overhead extraction, and cell extraction for DS1 PLCP, DS3 PLCP, E1 PLCP, G.751 E3 PLCP formats, or G.832 formatted streams.

- Provides detection of yellow alarm and loss of frame (LOF), and accumulates BIP-8 errors, framing errors and FEBE events.

- Provides ATM framing using cell delineation.

- Provides cell descrambling, header check sequence (HCS) error detection, idle/unassigned cell filtering, and accumulates the number of received idle/unassigned cells, the number of received cells written to the FIFO, and the number of HCS errors.

- Provides a four cell FIFO for rate decoupling between the line, and a higher layer processing entity. This FIFO may be bypassed to minimize the delay through the device when processing PLCP frames.

- Provides an asynchronous 8-bit wide FIFO interface for accessing received cell data bytes (available in either 84-pin PLCC or 100-pin PQFP packages).

- Provides a synchronous 8-bit wide FIFO with receive byte parity generation and compatible timing with current “UTOPIA” specifications for single PHY and multi-PHY interfaces (available only in the 100-pin PQFP package).

The transmitter section:

- Provides frame insertion for the M23 or C-bit parity DS3 applications, alarm insertion, and diagnostic features. In addition, far end alarm channel codes may be inserted, and an integral HDLC transmitter is provided to insert the path maintenance data link.

- Provides frame insertion for the G.751 or G.832 E3 applications, alarm insertion, and diagnostic features. In addition, for G.832, the Trail Trace is inserted, and an integral HDLC transmitter is provided to insert either the Network Requirement or the General Purpose data link.

- Provides frame insertion and path overhead insertion for DS1, DS3, E1 or E3 based PLCP formats. In addition, alarm insertion, and diagnostic features are provided.

- Provides an optional 8 kHz reference input for locking the transmit PLCP frame rate to an externally applied frame reference.

- Provides optional ATM cell scrambling, HCS generation/insertion, programmable idle/unassigned cell insertion, diagnostics features and accumulates transmitted cells read from the FIFO.

- Provides a four cell FIFO for rate decoupling between the line, and a higher layer processing entity. This FIFO may be bypassed to minimize the delay through the device when processing PCLP frames.

- Provides an asynchronous 8-bit wide FIFO interface for accessing transmit cell data bytes (available in either 84-pin PLCC or 100-pin PQFP packages).

- Provides a synchronous 8-bit wide FIFO with transmit byte parity checking and compatible timing with current “UTOPIA” specifications for single PHY and multi-PHY interfaces (available only in the 100-pin PQFP package).

Bypass and Loopback features:

- Allows bypassing of the DS3 or E3 framer to enable transmission system sublayer processing by an external device (for example, the PM4341 DS1 Framer/LIU may be used for DS1-based services, and the PM6341 E1 Framer/LIU may be used for E1-based services).

- Provides for DS3 or E3 diagnostic loopback, DS3 or E3 line loopback, DS3 or E3 payload loopback, and ATM cell loopback.

2 APPLICATIONS

- ATM or SMDS Routers, Bridges, Switches, and Adapter Cards
- DQDB Access Units
- ATM and SMDS test equipment

3 REFERENCES

- American National Standard for Telecommunications, ANSI T1.107-1995 - “Digital Hierarchy - Formats Specifications”.
- Bell Communications Research, TA-TSY-000773 - “Local Access System Generic Requirements, Objectives, and Interface in Support of Switched Multi-megabit Data Service” Issue 2, March 1990 and Supplement 1, December 1990.
- ITU-T, Recommendation I.432 - “B-ISDN User-Network Interface - Physical Layer Specification”, 1993.
- ITU-T Recommendation G.704 – “General Aspects of Digital Transmission Systems; Terminal Equipments – Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels”, July, 1995.
- ITU-T Blue Book, Recommendation G.751, - “Digital Multiplex Equipments Operating at the Third Order Bit Rate of 34368 kbit/s and the Fourth Order Bit Rate of 139264 kbit/s and using Positive Justification”, Vol. III, Fascicle III.4, 1988.
- ITU-T Recommendation G.804 - “ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH)”, 1993.
- ITU-T Recommendation G.832 - “Transport of SDH Elements on PDH Networks: Frame and Multiplexing Structures”, 1993.
- ETSI 300 269 “Metropolitan Area Network Physical Layer Convergence Procedure for 2.048 Mbit/s”, April 1994.
- ETSI 300 270 “Metropolitan Area Network Physical Layer Convergence Procedure for 34.368 Mbit/s”, April 1994.
- IEEE, Std 802.6-1990 - “Distributed Queue Dual Bus Subnetwork of a Metropolitan Area Network”.

- ATM Forum, V3.1, October, 1995 - “ATM User-Network Interface Specification”.
- ATM Forum, 94-0406R5, E3 (34,368 kpbs) Physical Layer Interface”, Dec. 21, 1994.
- ATM Forum, 95-1207R1, “DS3 Physical Layer Interface Specification”, December, 1995.
- ATM Forum, Level 1, V2.00 - February 1994 - “An ATM PHY Data path Interface”.

4 APPLICATION EXAMPLES

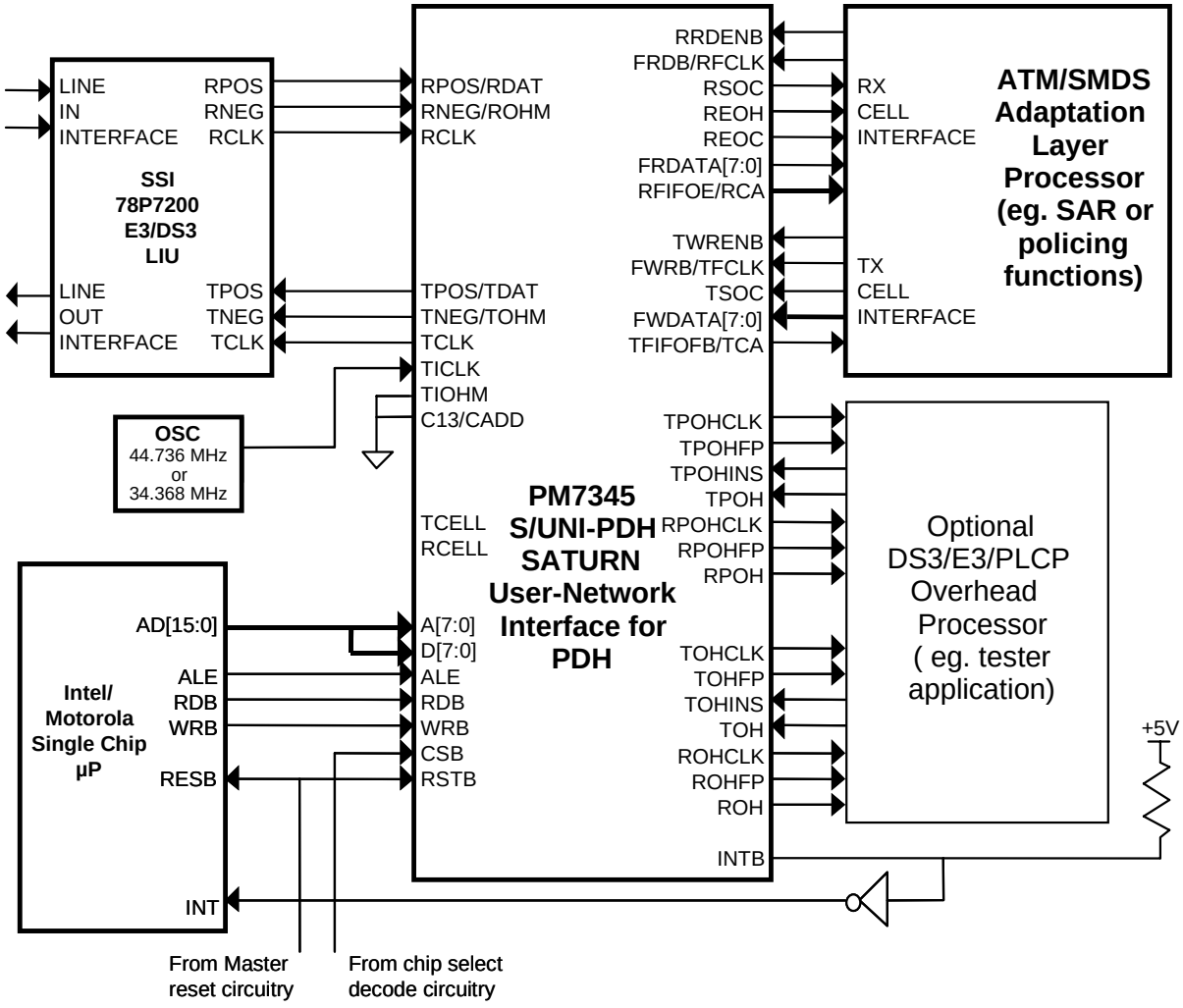
The PM7345 S/UNI-PDH is used to implement ATM user network interfaces (UNI) and network node interfaces (NNI). An example of a DS3/E3 User Network Interface (figure 1) and a DS1/E1 User Network Interface (figure 2) illustrate the interconnect between the S/UNI-PDH and system elements required to implement a complete ATM physical layer interface.

In figure 1, the DS3/E3 line interface function is provided by a commercially available DS3/E3 Line Interface Unit (LIU) product available from Silicon Systems. The DS3/E3 framing function, along with all PLCP processing, and ATM transmission convergence sublayer processing are performed by the S/UNI-PDH.

In figure 2, the DS1 LIU and framing functions are provided by the PM4341 T1 Transceiver (T1XC) product available from PMC-Sierra. The E1 LIU and framing functions are provided by the PM6341 E1 Transceiver (E1XC) product, also available from PMC-Sierra. The combination of these transceiver devices with the S/UNI-PDH allows both PLCP-formatted DS1/E1 signals, and ITU-T G.804 compliant DS1/E1 signals to be processed. The G.804 specification defines ATM direct cell mappings for a variety of transmission formats, including the 1.544 Mbit/s DS1, and the 2.048 Mbit/s E1 formats.

The optional PLCP and DS3/E3 Overhead Processors illustrated are expected to be implemented using programmable logic devices. For further S/UNI-PDH application information, please refer to document number PMC-930410, "The ATM Physical Layer".

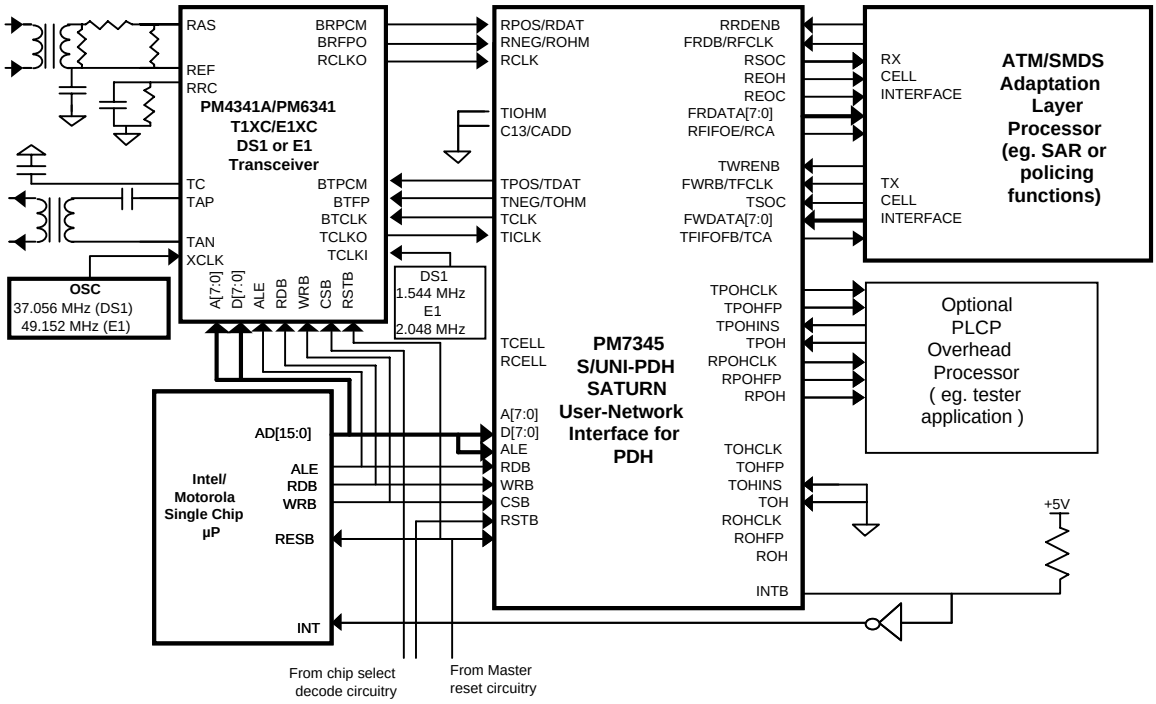
Figure 1 - DS3 and E3 User Network Interface



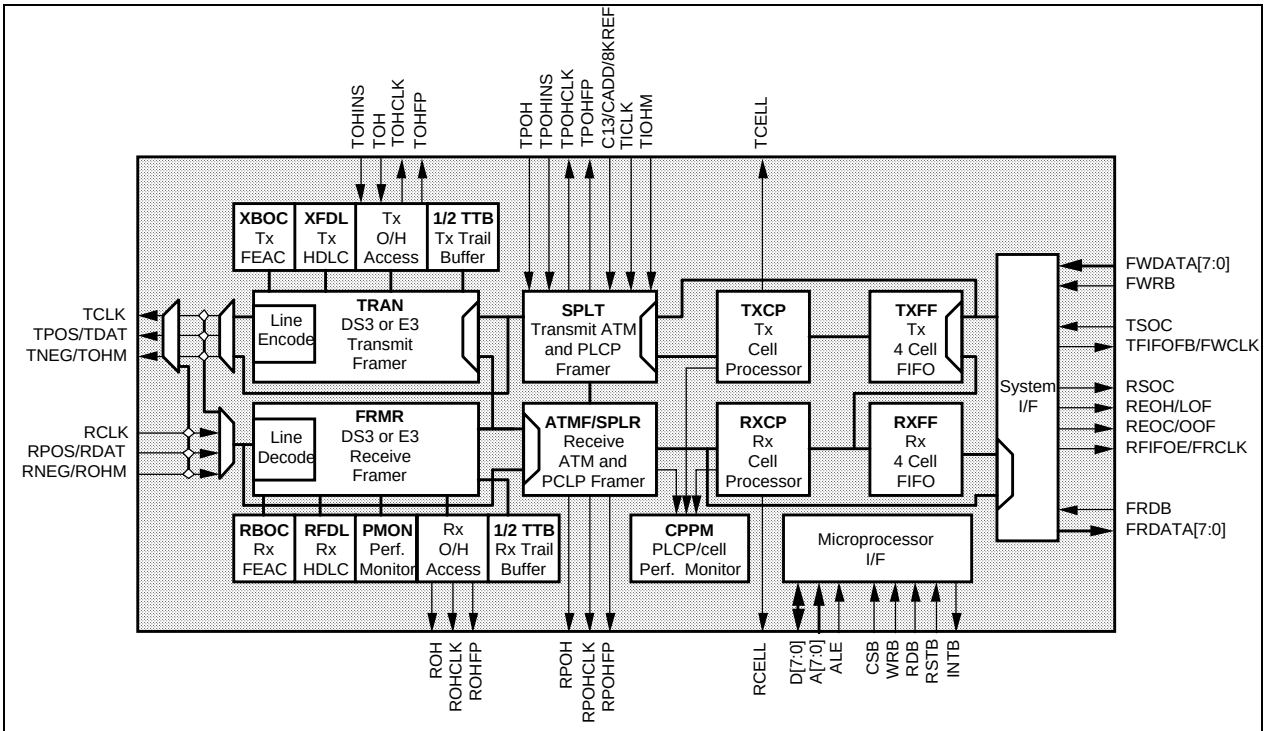
Layout information for the SSI 78P7200 E3/DS3 LIU is found in the OPERATION section of this document. Please refer to it as an example of the E3 and DS3 configuration used by PMC-Sierra.[1]

[1] Please contact Silicon Systems at (714) 573-6200 for detailed application information concerning the 78P7200 E3/DS3 LIU.

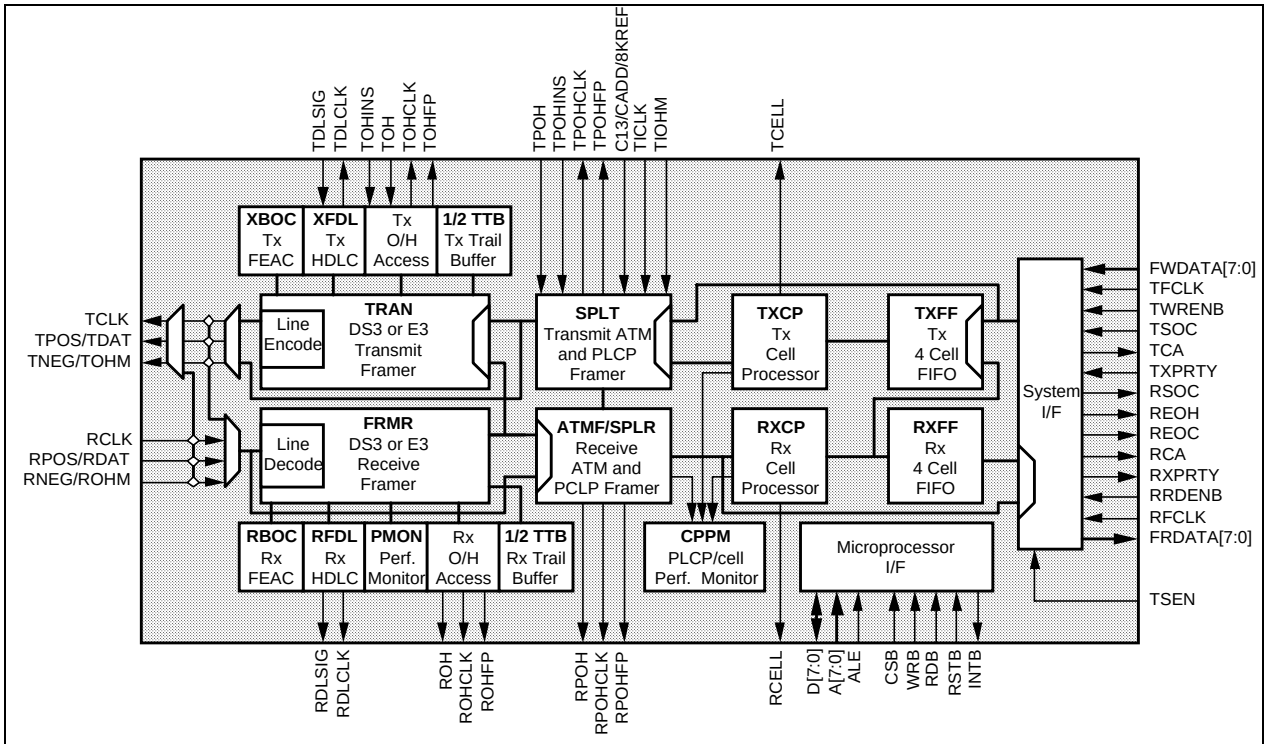
Figure 2 - DS1 and E1 User Network Interface



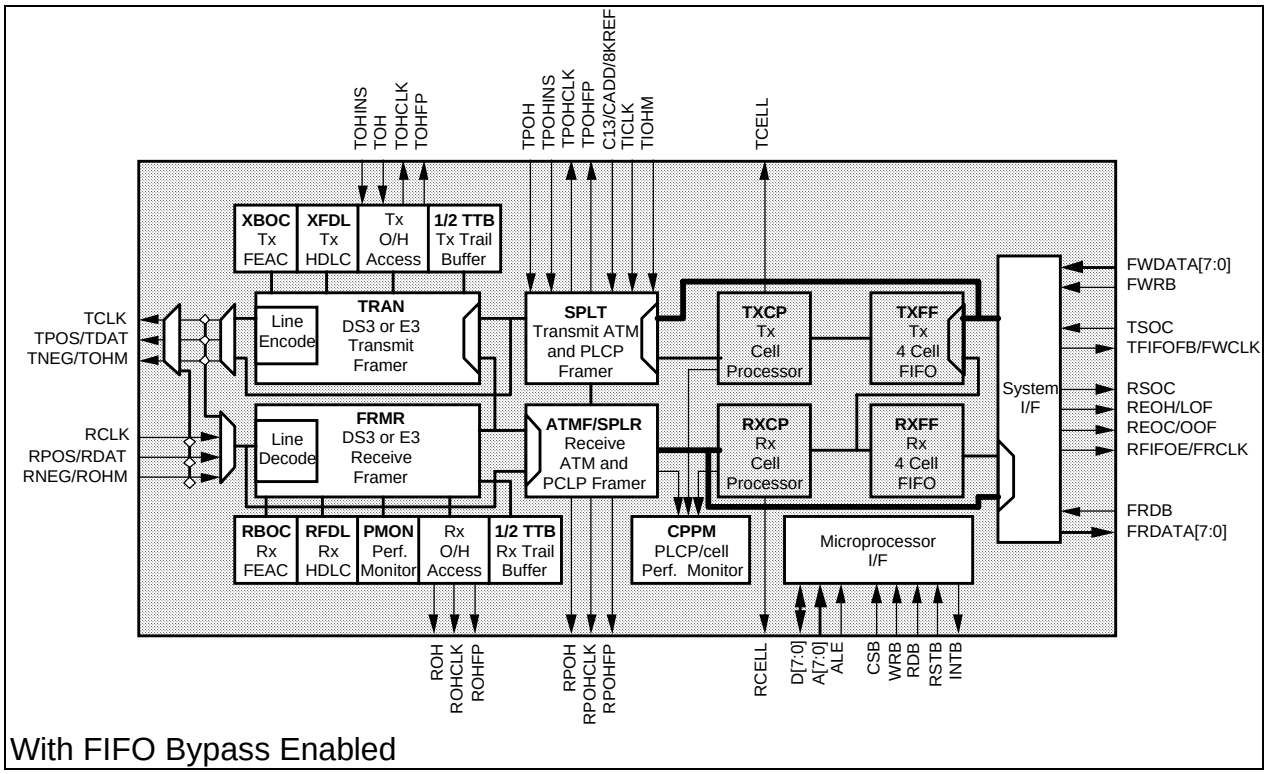
5 BLOCK DIAGRAM



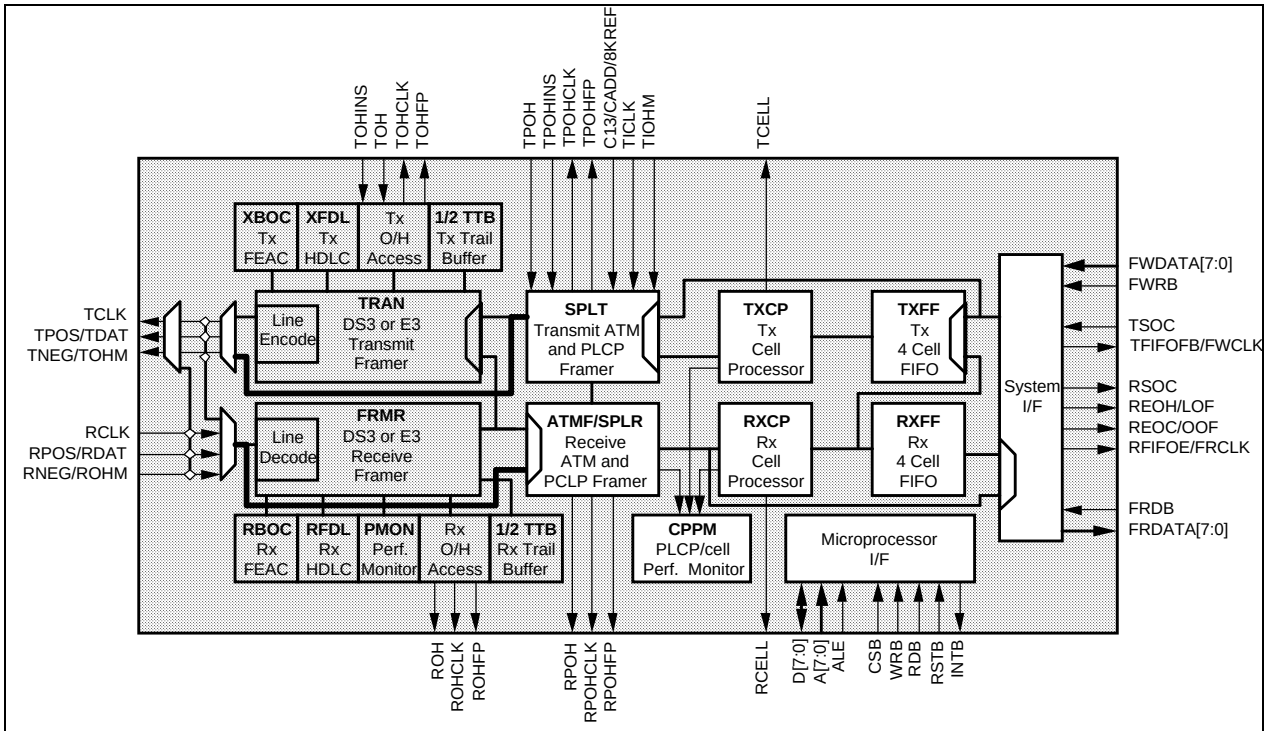
Normal Operating Mode (84-pin PLCC Async FIFO interface shown)



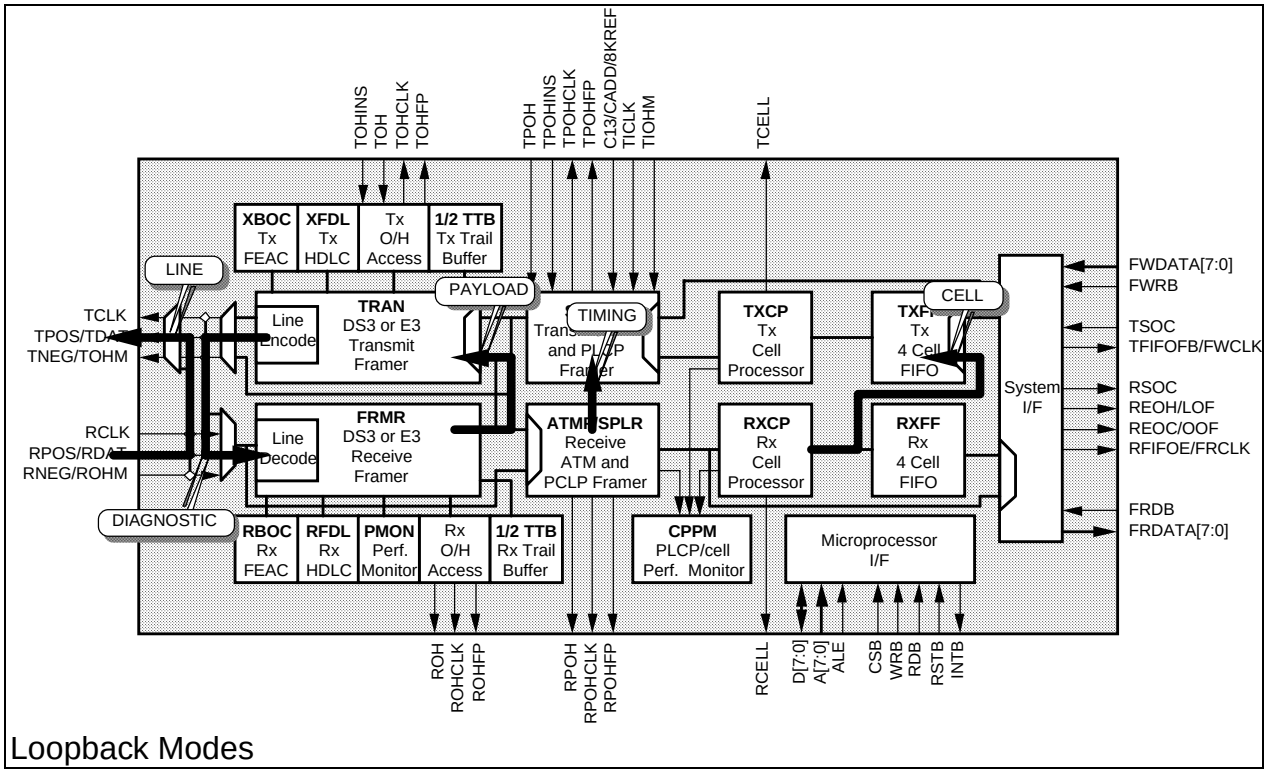
Normal Operating Mode (100-pin PQFP Sync FIFO interface shown)



With FIFO Bypass Enabled



With DS3/E3 Framer Bypassed



Loopback Modes

6 DESCRIPTION

The PM7345 S/UNI-PDH is an ATM physical layer processor with integrated DS3 and E3 framing. PLCP sublayer DS1, DS3, E1, and E3 processing is supported as is ATM cell delineation.

The S/UNI-PDH contains an integral DS3 framer, which provides DS3 framing and error accumulation in accordance with ANSI specifications, and an integral E3 framer, which provides E3 framing in accordance with ITU-T Recommendations G.832 and G.751. When configured for DS3 transmission system sublayer processing, the S/UNI-PDH accepts and outputs either a B3ZS-encoded bipolar or a unipolar signal compatible with M23 and C-bit parity applications. When configured for E3 transmission system sublayer processing, the S/UNI-PDH accepts and outputs either a HDB3-encoded bipolar or a unipolar signal compatible with G.751 and G.832 applications. When configured for DS1, or E1 transmission system sublayer processing, the S/UNI-PDH accepts and outputs a unipolar signal with appropriate clock and frame pulse signals for physical sublayer processing. When configured for other transmission systems, the S/UNI-PDH provides a generic interface for physical sublayer processing.

In the DS3 receive direction, the S/UNI-PDH frames to a DS3 signal with a maximum average reframe time of 1.5 ms and detects line code violations, loss of signal, framing bit errors, parity errors, path parity errors, AIS, far end receive failure and idle code. The DS3 overhead bits are extracted and presented on a serial output. When in C-bit parity mode, the Path Maintenance Data Link and the Far End Alarm and Control (FEAC) channel are extracted. An HDLC receiver is provided for Path Maintenance Data Link support. In addition, valid bit-oriented codes in the FEAC channel are detected and are available through the microprocessor port.

In the E3 receive direction, the S/UNI-PDH frames to either a G.751 or G.832 E3 signal with a maximum average reframe time of 0.5 ms and detects line code violations, loss of signal, framing bit errors, AIS, and remote alarm indication. Further, when processing G.832 formatted data, parity errors, far end receive failure, and far end block errors are also detected; and the Trail Trace message is extracted and made available through the microprocessor port. An HDLC receiver is provided for either the G.832 Network Requirement or the G.832 General Purpose Data Link support.

Error event accumulation is also provided by the S/UNI-PDH. Framing bit errors, line code violations, parity errors, path parity errors and far end block errors are accumulated in saturating counters.

In the DS3 transmit direction, the S/UNI-PDH inserts DS3 framing, X and P bits. When enabled for C-bit parity operation, a bit-oriented code transmitter and an HDLC transmitter are provided for insertion of the FEAC channel and the Path Maintenance Data Link into the appropriate overhead bits. The Alarm Indication Signal can be inserted when enabled by an external input or using an internal register bit; other status signals such as the idle signal can be inserted when enabled by an internal register bit. When M23 operation is selected, the C-bit Parity ID bit (the first C-bit of the first M sub-frame) is forced to toggle so that downstream equipment will not confuse an M23-formatted stream with stuck-at 1 C-bits for C-bit Parity application.

In the E3 transmit direction, the S/UNI-PDH inserts E3 framing in either G.832 or G.751 format. When enabled for G.832 operation, an HDLC transmitter is provided for insertion of either the Network Requirement or General Purpose Data Link into the appropriate overhead bits. The Alarm Indication Signal and other status signals can be inserted by internal register bits.

The S/UNI-PDH also supports diagnostic modes in which it inserts parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, or all-zeros.

The S/UNI-PDH provides cell delineation for ATM cells using the PLCP framing format, or by using the header check sequence octet in the ATM cell header as specified by ITU-T Recommendation I.432. DS1, DS3, E1 and E3 based PLCP frame formats can be processed. An interface consistent with the generic physical interface defined by ITU-T Recommendation I.432 is provided for arbitrary rates up to 52 Mbit/s. This interface is used to provide physical layer support for transmission systems that do not have an associated PLCP sublayer, or to provide an efficient means of directly mapping ATM cells to existing transmission system formats (such as DS3 and DS1).

In the PLCP receive direction, framing, path overhead extraction and cell extraction is provided. BIP-8 error events, frame octet error events and far end block error events are accumulated.

In the PLCP transmit direction, the S/UNI-PDH provides overhead insertion using inputs or internal registers, DS3 nibble and E3 byte stuffing, automatic BIP-8 octet generation and insertion and automatic far end block error insertion. Diagnostic features for BIP-8 error, framing error and far end block error insertion are also supported.

In the cell receive path, idle/unassigned cells may be dropped according to a programmable filter. By default, incoming cells with single bit HCS errors are corrected and written to the FIFO buffer. Optionally, cells can be dropped upon

detection of a HCS error. The ATM cell payloads are optionally descrambled. Assigned cells containing no detectable HCS errors are written to a FIFO buffer. Cells are read from the FIFO using an asynchronous 8-bit wide datapath interface or a synchronous 9-bit wide datapath, depending upon the packaging option selected. Counts of error-free assigned cells, and cells containing HCS errors are accumulated independently for performance monitoring purposes.

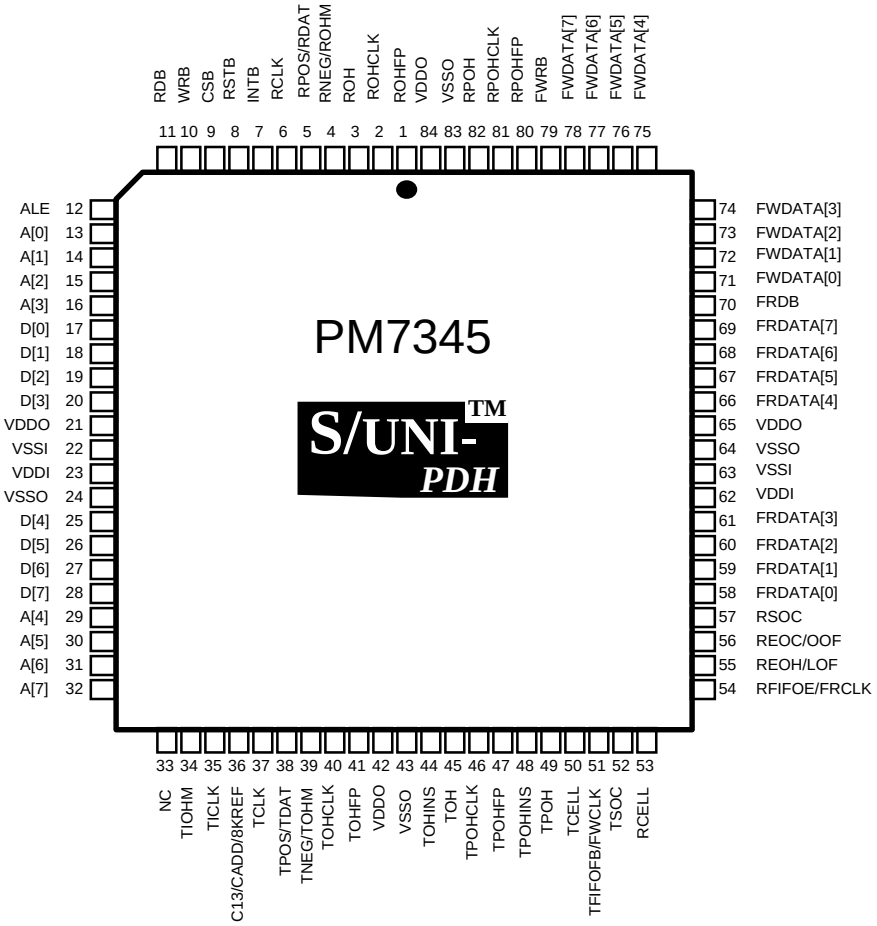
In the cell transmit path, cells are written to a FIFO buffer using an asynchronous 8-bit wide datapath interface or a synchronous 9-bit wide datapath interface, depending upon the packaging option selected. Idle/unassigned cells are automatically inserted when the FIFO contains less than one full cell. HCS generation, and cell payload scrambling are optionally provided.

Both receive and transmit cell FIFOs provide buffering for four cells. The FIFOs provide the rate matching interface between the higher layer ATM entity and the S/UNI-PDH.

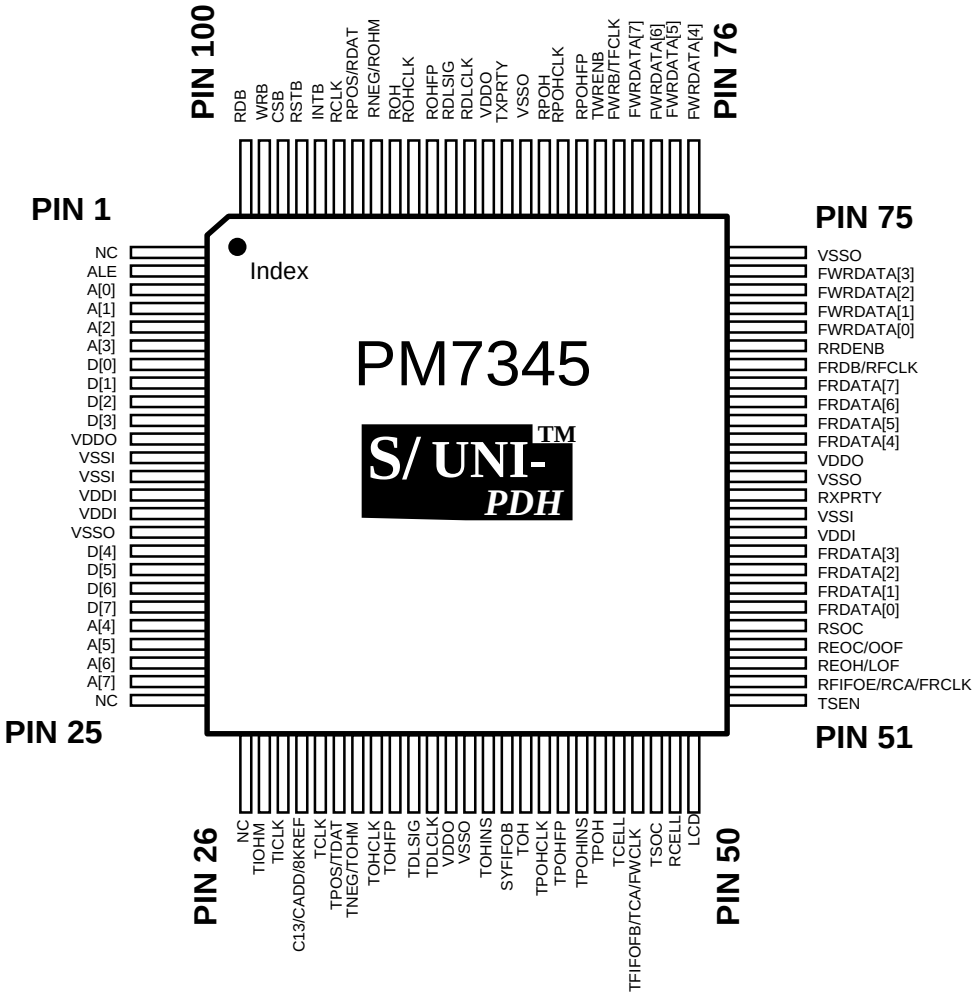
The S/UNI-PDH is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be identified, acknowledged, or masked via this interface.

7 PIN DIAGRAM

The S/UNI-PDH is available in an 84-pin PLCC.



The S/UNI-PDH is also available in a 100-pin PQFP having a body size of 14x14mm and a pin pitch of 0.5mm.



8 PIN DESCRIPTION

Pin Name	Type	Pin No. QFP	Pin No. PLCC	Function
RCLK	Input	95	6	**Receive Clock (RCLK).** RCLK provides the receive direction timing. RCLK is the externally recovered transmission system baud rate clock that samples the RPOS/RDAT and RNEG/ROHM inputs on its rising or falling edge. The RCLK maximum frequency is 52 MHz.
RPOS/	Input	94	5	**Receive Positive Pulse (RPOS).** RPOS contains the positive pulses received on the B3ZS-encoded DS3, or the HDB3-encoded E3, transmission system when the dual-rail NRZ input format is selected. RPOS contains the entire stream when the single-rail (unipolar) NRZ input format is enabled. The dual-rail/single-rail selection is controlled by the UNI bit in the DS3 FRMR or the E3 FRMR Configuration Registers.
RDAT				**Receive Data (RDAT).** RDAT contains the received transmission system stream when a non-DS3/E3 based transmission system is being processed (for example RDAT may contain a DS1 or E1 stream). The RPOS/RDAT pin function selection is controlled by the FRMRBP bit in the S/UNI-PDH Configuration Register. Both RPOS and RDAT are sampled on the rising edge of RCLK by default, and may be enabled to be sampled on the falling edge of RCLK. This sampling is controlled by the RCLKINV bit in the S/UNI-PDH Control Register. In addition, signal polarity control is provided by the RPNINV bit in the S/UNI-PDH Control Register.

RNEG/ ROHM	Input	93	4	**Receive Negative Pulse (RNEG).** RNEG contains the negative pulses received on the B3ZS encoded DS3, or the HDB3-encoded E3, transmission system when the dual-rail NRZ input format is selected. RNEG contains line code violation indications when the single-rail (unipolar) NRZ input format is enabled. Each line code violation is represented by an RCLK period-wide pulse. The dual-rail/single-rail selection is controlled by the UNI bit in the DS3 FRMR or E3 FRMR Configuration Registers. **Receive Overhead Mask (ROHM).** ROHM indicates the position of overhead bits in the non-DS3/E3 based transmission system stream, RDAT. When a PLCP formatted signal is received, ROHM is pulsed once per transmission frame, and indicates the DS1 or E1 frame alignment. When a non-PLCP based signal is received, ROHM indicates the position of each overhead bit in the transmission frame. The RNEG/ROHM pin function selection is controlled by the FRMRBP bit in the S/UNI-PDH Configuration Register. Both RNEG and ROHM are sampled on the rising edge of RCLK by default, and may be enabled to be sampled on the falling edge of RCLK. This sampling is controlled by the RCLKINV bit in the S/UNI-PDH Control Register. In addition, signal polarity control is provided by the RPNINV bit in the S/UNI-PDH Control Register.
ROHCLK	Output	91	2	**Receive DS3/E3 Overhead Clock (ROHCLK).** ROHCLK is active when a DS3 or E3 stream is being processed. ROHCLK is nominally a 526 kHz clock when processing DS3, is nominally a 1.072 MHz clock when processing G.832 E3, and is nominally a 1.074 MHz clock when processing G.751 E3. ROH, and ROHFP are updated on the falling edge of ROHCLK.

ROH	Output	92	3	**Receive DS3/E3 Overhead Data (ROH).** ROH contains the overhead bits (C, F, X, P, and M) extracted from the received DS3 stream; ROH contains the overhead bytes (FA1, FA2, EM, TR, MA, NR, and GC) extracted from the received G.832 E3 stream; ROH contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) extracted from the received G.751 E3 stream. ROH is updated on the falling edge of ROHCLK.
ROHFP	Output	90	1	**Receive DS3/E3 Overhead Frame Position (ROHFP).** ROHFP locates the individual overhead bits in the received overhead data stream, ROH. ROHFP is high during the X1 overhead bit position in the ROH stream when processing a DS3 stream. ROHFP is high during the first bit of the FA1 byte when processing a G.832 E3 stream. ROHFP is high during the RAI overhead bit position when processing a G.751 E3 stream. ROHFP is updated on the falling edge of ROHCLK.
RPOHCLK	Output	83	81	**Receive PLCP Overhead Clock (RPOHCLK).** RPOHCLK is active when PLCP processing is enabled. The frequency of this signal depends on the selected PLCP format. RPOHCLK is nominally a 26.7 kHz clock for a DS1 PLCP frame, a 768 kHz clock for a DS3 PLCP frame, a 33.7 kHz clock for an E1 based PLCP frame, or a 576 kHz clock for a G.751 E3 based PLCP frame. RPOHFP and RPOH are updated on the falling edge of RPOHCLK.
RPOH	Output	84	82	**Receive PLCP Overhead Data (RPOH).** RPOH contains the PLCP path overhead octets (Zn, F1, B1, G1, M1, M2, and C1) extracted from the received PLCP frame when the PLCP layer is in-frame. When the PLCP layer is in the loss of frame state, RPOH is forced to all ones. The octet data on RPOH is shifted out in order from the most significant bit (bit 1) to the least significant bit (bit 8). RPOH is updated on the falling edge of RPOHCLK.

RPOHFP	Output	82	80	**Receive PLCP Overhead Frame Position (RPOHFP).** RPOHFP locates the individual PLCP path overhead bits in the receive overhead data stream, RPOH. RPOHFP is logic 1 while bit 1 (the most significant bit) of the path user channel octet (F1)is present in the RPOH stream. RPOHFP is updated on the falling edge of RPOHCLK.
RDLSIG	Output	89	n/a	**Receive Data Link Signal (RDLSIG).** In DS3 mode, RDLSIG contains the Path Maintenance Data Link signal from the received C-bit Parity DS3 stream. RDLSIG is not affected by the RNETOP bit in the S/UNI-PDH Data Link and FERF Control register while in DS3 mode. In E3 G.832 mode, RDLSIG contains the NR or GC data link signal, as selected by the RNETOP bit, from the received E3 G.832 stream. In E3 G.751 mode, RDLSIG contains the National Use bit from the received G.751 E3 stream if the RNETOP bit is logic one. RDLSIG is updated on the falling edge of RDLCLK.
RDLCLK	Output	88	n/a	**Receive Data Link Clock (RDLCLK).** RDLCLK is active when a DS3 or E3 G.832 stream is being processed. With an E3 G.751 stream, the RNETOP bit in the S/UNI-PDH Data Link and FERF Control register must be set to logic one for RDLCLK to be active.
RCELL	Output	49	53	**Receive Cell Indication (RCELL).** RCELL pulses once for every cell received. RCELL is updated using timing derived from the receive input clock (RCLK) and is active for a minimum of 8 RCLK periods. RCELL is forced to logic 0 when in the FIFO bypass mode.

LCD	Output	50	n/a	**Loss of Cell Delineation (LCD).** The LCD signal indicates when cell delineation cannot be found. LCD transitions to logic 1 when an out of cell delineation (OCD) defect has persisted past a selected threshold. Once asserted, OCD remains logic 1 until no OCD defect has been detected past the selected threshold. The OCD defect state is entered when the cell delineation state machine is not in the SYNC state (please refer to the Functional Description section for an explanation of the cell delineation state machine). The LCD indication is available for register access and can be enabled to generate a microprocessor interrupt.
FRDB/	Input	69	70	**FIFO Read (FRDB).** FRDB reads cell octets from the receive FIFO. The data is enabled on the FRDATA[7:0] outputs on the falling edge of FRDB. RSOC, REOH, and REOC are updated on the rising edge of FRDB. Note that when the receive FIFO is bypassed, FRDB should be logic 1 to minimize the S/UNI-PDH power consumption.
RFCLK				**Read FIFO Clock (RFCLK).** RFCLK is used to read bytes from the synchronous FIFO interface. This interface is only available in the 100-pin PQFP package when the synchronous FIFO interface is enabled (SYFIFOB tied to logic 0). RFCLK must cycle at a 25 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflow. RRDENB is sampled using the rising edge of RFCLK. RSOC, RCA, RXPRTY, and FRDATA[7:0] are all updated on the rising edge of RFCLK.

RRDENB	Input	70	n/a	**Receive FIFO Read Enable (RRDENB).** This active low enable signal is used to initiate reads from the synchronous receive FIFO interface (when SYFIFOB is tied to logic 0). RRDENB sampled (on the rising edge of RFCLK) at logic 0 indicates that RSOC and FRDATA[7:0] will be sampled by the ATM layer at the end of the current RFCLK cycle (on the next rising edge of RFCLK). When RRDENB is sampled at logic 1, no read is performed. RRDENB must be used in conjunction with RFCLK to access the FIFO at a high enough instantaneous rate as to avoid FIFO overflow. The RRDENB signal is only available in the 100-pin PQFP package. RRDENB contains an integral pull-down resistor.

RFIFOE/	Output	52	54	**Receive FIFO Empty (RFIFOE).** RFIFOE indicates the receive FIFO status. RFIFOE is logic 1 when the cell-based FIFO is empty and logic 0 when the FIFO contains at least 1 cell. RFIFOE timing is applicable when using the asynchronous FIFO interface in the S/UNI-PDH (either in the 84-pin PLCC or when SYFIFOB is tied to logic 1 in the 100-pin package). Note that with the asynchronous FIFO interface RFIFOE transitions from empty to full (logic 1 to logic 0) on write cell boundaries with timing derived from the RCLK input. RFIFOE transitions from full to empty (logic 0 to logic 1) on read cell boundaries on the rising edge of FRDB. RFIFOE should be treated by the ATM layer as a purely asynchronous signal.
RCA/				**Receive Cell Available (RCA).** RCA is available in the 100-pin PQFP package when SYFIFOB is tied to logic 0. When the synchronous FIFO interface is used, RCA is an active high signal and is logic 1 when the cell-based FIFO contains at least 1 cell and is logic 0 when the cell-based FIFO is empty. RCA can be enabled to transition low when the FIFO is empty (default) or when the FIFO is 4 bytes away from being empty (almost empty), as controlled by the REMPTY4 register bit. RCA transitions on rising edges of the RFCLK.
FRCLK				**Receive Cell Clock (FRCLK).** FRCLK is derived from RCLK when the receive FIFO is bypassed (the FIFOBP bit in the S/UNI-PDH Configuration Register is logic 1). FRDATA[7:0], LOF, OOF, and RSOC are updated on the falling edge of FRCLK.

RSOC	Tristate	55	57	**Receive Start of Cell (RSOC).** RSOC indicates the start of a 53 octet cell. It is asserted when the first octet is read from the receive FIFO. RSOC is tristateable in the 100-pin PQFP package when TSEN is logic 1. It is forced tristate while FRDB is high and the receive FIFO is not bypassed (when SYFIFOB is logic 1), or while RRDENB is sampled high by the rising edge of RFCLK (when SYFIFOB is logic 0). The RSOC logic value is driven on the pin while FRDB is low (asynchronous FIFO interface) or while RRDENB is sampled logic 0 (synchronous interface). RSOC is updated on the rising edge of FRDB or RFCLK. When the receive FIFO is bypassed, RSOC is updated on the falling edge of FRCLK.
REOH/ LOF	Tristate	53	55	**Receive End of Header (REOH).** REOH is asserted when the fifth octet of the 53 octet cell is read from the receive FIFO. REOH is tristatable in the 100-pin PQFP package when TSEN is logic 1. It is forced tristate while FRDB is high and the receive FIFO is not bypassed (when SYFIFOB is logic 1), or while RRDENB is sampled high by the rising edge of RFCLK (when SYFIFOB is logic 0). The REOH logic value is driven on the pin while FRDB is low (asynchronous FIFO interface) or while RRDENB is sampled logic 0 (synchronous interface). REOH is updated on the rising edge of FRDB or RFCLK. **PLCP Loss of Frame (LOF).** LOF is asserted while the PLCP receiver is in a loss of frame state. LOF may be used to indicate the valid/invalid status of the FRDATA[7:0] octets to a higher layer processing entity while the receive FIFO is bypassed. LOF is updated on the falling edge of FRCLK. The REOH/LOF pin function selection is controlled by the FIFOBP bit in the S/UNI-PDH Configuration Register.

REOC/ OOF	Tristate	54	56	**Receive End of Cell (REOC).** REOC is asserted when the 53rd octet of the 53 octet cell is being read from the receive FIFO. RSOC is tristatable in the 100-pin PQFP package when TSEN is logic 1. It is forced tristate while FRDB is high and the receive FIFO is not bypassed (when SYFIFOB is logic 1), or while RRDENB is sampled high by the rising edge of RFCLK (when SYFIFOB is logic 0). The RSOC logic value is driven on the pin while FRDB is low (asynchronous FIFO interface) or while RRDENB is sampled logic 0 (synchronous interface). REOC is updated on the rising edge of FRDB or RFCLK. **PLCP Out of Frame (OOF).** OOF is asserted while the PLCP receiver is in an out of frame state. OOF may be used to indicate the valid/invalid status of the FRDATA[7:0] octets to a higher layer processing entity while the receive FIFO is bypassed. OOF is updated on the falling edge of FRCLK. The REOC/OOF pin function selection is controlled by the FIFOBP bit in the S/UNI-PDH Configuration Register.
FRDATA[7] FRDATA[6] FRDATA[5] FRDATA[4] FRDATA[3] FRDATA[2] FRDATA[1] FRDATA[0]	Tristate Tristate Tristate Tristate Tristate Tristate Tristate Tristate	68 67 66 65 59 58 57 56	69 68 67 66 61 60 59 58	**Receive FIFO Data (FRDATA[7:0]).** FRDATA[7:0] contains the cell octet that is read from the receive FIFO. The FRDATA[7:0] bus is tristatable in the 100-pin PQFP package when TSEN is logic 1. FRDATA[7:0] is forced tristate while FRDB is high and the receive FIFO is not bypassed (when SYFIFOB is logic 1), or while RRDENB is sampled high by the rising edge of RFCLK (when SYFIFOB is logic 0). The octet read from the receive FIFO is driven on the FRDATA[7:0] bus while FRDB is low (asynchronous FIFO interface) or while RRDENB is sampled logic 0 (synchronous interface). FRDATA[7:0] is updated on the falling edge of FRCLK when the receive FIFO is bypassed.

RXPRTY	Tristate	62	n/a	**Receive FIFO Read Data Parity (RXPRTY).** RXPRTY is only available in the 100-pin PQFP package. RXPRTY indicates the parity of the byte on FRDATA[7:0]. Even or Odd parity is computed over the FRDATA[7:0] bus, depending upon the REVEN register bit setting. If REVEN is logic 1, even parity is calculated; if REVEN is logic 0, odd parity is calculated. By default, RXPRTY indicates odd parity. RXPRTY is tristatable when TSEN is logic 1. RXPRTY is forced tristate while FRDB is high (when SYFIFOB is logic 1), or while RRDENB is sampled high by the rising edge of RFCLK (when SYFIFOB is logic 0). The parity value is driven on RXPRTY while FRDB is low (asynchronous FIFO interface) or while RRDENB is sampled logic 0 (synchronous interface).
TSEN	Input	51	n/a	**Tristate Bus Enable (TSEN).** TSEN controls the tristatability of the FRDATA[7:0], RXPRTY, REOH, REOC and RSOC pins in the 100-pin PQFP package. When TSEN is logic 1, the FRDATA[7:0] bus, RXPRTY, REOH, REOC and RSOC can be tristated by either the FRDB signal or the sampled RRDENB signal (depending upon the interface selected by SYFIFOB). When TSEN is logic 0, the FRDATA[7:0] bus, RXPRTY, REOH, REOC and RSOC are always active and forced to digital logic values. TSEN contains an integral pull-up resistor.

FWRB/ TFCLK	Input	80	79	**FIFO Write (FWRB).** FWRB writes cell octets to the transmit FIFO. The data present on the FWDATA[7:0] bus is written into the transmit FIFO on the rising edge of FWRB. TSOC is sampled on the falling edge of FWRB. **Transmit FIFO Write Clock (TFCLK).** TFCLK is used to write bytes into the synchronous transmit FIFO interface. This interface is only available in the 100-pin PQFP package when the synchronous FIFO interface is enabled (SYFIFOB tied to logic 0). TFCLK must cycle at a 25 MHz or lower instantaneous rate. TWRENB, TSOC, TXPRTY, and FWDATA[7:0] are all sampled on the rising edge of TFCLK. TCA is updated on the rising edge of TFCLK.
TWRENB	Input	81	n/a	**Transmit FIFO Write Enable (TWRENB).** This active low enable signal is used to initiate writes into the transmit FIFO. TWRENB is sampled on the rising edge of TFCLK. When TWRENB is sampled as a logic 0, the byte sampled on the FWDATA[7:0] bus is written to the transmit FIFO. When TWRENB is sampled as a logic 1, no write is performed. A complete 53 byte cell must be written to the FIFO before it is inserted into the transmission layer. Idle/Unassigned cells are inserted when a complete cell is not available. The TWRENB signal is only available in the 100-pin PQFP package when SYFIFOB is tied to logic 0. TWRENB contains an integral pull-down resistor.
TCELL	Output	46	50	**Transmit Cell Indication (TCELL).** TCELL pulses once for every cell transmitted. TCELL is updated using timing derived from the transmit input clock (TICLK) and is active for a minimum of 8 TICLK periods. TCELL is forced to logic 0 when in the FIFO bypass mode.

TFIFOFB/	Output	47	51	**Transmit FIFO Not Full (TFIFOFB).** TFIFOFB indicates the transmit FIFO status. The depth of the transmit FIFO is controlled using the TXCP Control register. When TFIFOFB is logic 1, the transmit FIFO is not full and cells can be written into the transmit FIFO. TFIFOFB timing is applicable when using the asynchronous FIFO interface in the S/UNI-PDH (either in the 84-pin PLCC or when SYFIFOB is tied to logic 1 in the 100-pin package). Note that with the asynchronous FIFO interface TFIFOFB transitions from empty to full/almost full (logic 1 to logic 0) on the rising edge of FWRB. TFIFOFB transitions from full to empty (logic 0 to logic 1) on read cell boundaries with timing derived from the TICLK input. TFIFOFB should be treated by the ATM layer as a purely asynchronous signal. TFIFOFB can also programmed to indicate full or almost-full through the TFULL4 register bit. When TFULL4 is logic 1, TFIFOFB transitions from empty to almost full, indicating that the transmit FIFO can accept no more than four writes before overflowing. When TFULL4 is logic 0 (default), TIFIFOB transitions from empty to full, indicating that the transmit FIFO can accept no more writes before overflowing. (cont.)

TCA/	Output	47	51	**Transmit Cell Available (TCA).** TCA is available in the 100-pin PQFP package when SYFIFOB is tied to logic 0. When the synchronous FIFO interface is used, TCA is an active high signal and is logic 1 when the cell-based transmit FIFO is not full and a complete cell may be written in. TCA can be enabled to transition low when the FIFO is 4 writes away from being full (almost full) or when the FIFO is full (default), as controlled by the TFULL4 register bit. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells by the FIFODP[1:0] bits of TXCP Control register. If the programmed depth is less than four, more than one cell may be written after TCA is asserted. TCA transitions on rising edges of the TFCLK.
FWCLK				**Transmit Cell Clock (FWCLK).** FWCLK is derived from the transmit source clock (TICLK, or RCLK as determined by the timing mode selected) when the transmit FIFO is bypassed (the FIFOBP bit in the S/UNI-PDH Configuration Register is logic 1). FWDATA[7:0], and TSOC are sampled on the rising edge of FWCLK.
TSOC	Input	48	52	**Transmit Start of Cell (TSOC).** TSOC identifies the start of a cell on FWDATA[7:0]. When TSOC is logic 1, the octet on FWDATA[7:0] is expected to be the first octet of a 53 octet cell. It is not necessary for TSOC to be present each cell; an internal cell counter flywheels based on the last occurrence of TSOC. TSOC is sampled on the falling edge of FWRB (in the asynchronous FIFO interface), or TSOC is sampled on the rising edge of TFCLK (in the synchronous FIFO interface). TSOC is sampled on the rising edge of FWCLK when the transmit FIFO is bypassed.

FWDATA[7] FWDATA[6] FWDATA[5] FWDATA[4] FWDATA[3] FWDATA[2] FWDATA[1] FWDATA[0]	Input Input Input Input Input Input Input Input	79 78 77 76 74 73 72 71	78 77 76 75 74 73 72 71	**Transmit FIFO Data (FWDATA[7:0]).** FWDATA[7:0] contains the cell octet that is written to the transmit FIFO. In the asynchronous FIFO interface (in the 84-pin PLCC package or in the 100-pin PQFP package when SYFIFOB is tied to logic 1), FWDATA[7:0] is sampled on the rising edge of FWRB. In the synchronous FIFO interface (i.e. 100-pin package with SYFIFOB tied to logic 0), FWDATA[7:0] is sampled on the rising edge of TFCLK when TWRENB is logic 0. FWDATA[7:0] is sampled on the rising edge of FWCLK when the transmit FIFO is bypassed.
TXPRTY	Input	86	n/a	**Transmit FIFO Write Data Parity (TXPRTY).** TXPRTY is only available in the 100-pin PQFP package. TXPRTY indicates the parity of the byte input on the FWDATA[7:0] bus. Even or Odd parity is computed over the FWDATA[7:0] bus, depending upon the TEVEN register bit setting, and compared to the value input on TXPRTY. If TEVEN is logic 1, even parity is calculated and compared; if TEVEN is logic 0, odd parity is calculated. By default, TXPRTY is expected to indicate odd parity. When using the synchronous FIFO (when SYFIFOB is tied to logic 0), TXPRTY is sampled on the rising edge of TFCLK when TWRENB is asserted. When using the asynchronous FIFO (when SYFIFOB is tied to logic 1), TXPRTY is sampled on the rising edge of FWRB. If the computed parity does not match the value on TXPRTY, a parity error is flagged and an interrupt generated, if enable. TXPRTY contains an integral pull-up resistor.
TICLK	Input	28	35	**Transmit Input Clock (TICLK).** TICLK provides the transmit direction timing. TICLK is the externally generated transmission system baud rate clock; it is internally buffered to produce the transmit clock output, TCLK, and can be enabled to update the TPOS/TDAT and TNEG/TOHM outputs on the TICLK rising edge. The TICLK maximum frequency is 52 MHz.

TIOHM	Input	27	34	**Transmit Input Overhead Mask (TIOHM).** TIOHM indicates the position of overhead bits in the transmission system stream, TDAT. TIOHM is delayed internally to produce the TOHM output. When configured for operation over a DS1, a DS3, an E1, or an E3 transmission system sublayer, TIOHM is not required, and should be set to logic 0. When configured for other transmission systems, TIOHM is set to logic 1 for each overhead bit position. TIOHM is set to logic 0 if the transmission system contains no overhead bits. TIOHM is sampled on the rising edge of TICLK.
TCLK	Output	30	37	**Transmit Output Clock (TCLK).** TCLK provides the transmit direction timing. TCLK is a buffered version of TICLK and can be enabled to update the TPOS/TDAT and TNEG/TOHM outputs on its rising or falling edge.

TPOS/	Output	31	38	**Transmit Positive Pulse (TPOS).** TPOS contains the positive pulses transmitted on the B3ZS-encoded DS3, or HDB3-encoded E3, transmission system when the dual-rail NRZ output format is selected. TPOS contains the entire stream when the single-rail (unipolar) NRZ input format is enabled. The dual-rail/single-rail selection is controlled by the TUNI bit in the S/UNI-PDH Control Register.
TDAT				**Transmit Data (TDAT).** TDAT contains the transmit transmission system stream when a non-DS3/E3 based transmission system is processed (for example TDAT may contain a DS1 or E1 stream). The TPOS/TDAT pin function selection is controlled by the FRMRBP bit in the S/UNI-PDH Configuration Register. Both TPOS and TDAT are updated on the falling edge of TCLK by default, and may be enabled to be updated on the rising edge of TCLK. This sampling is controlled by the TCLKINV bit in the S/UNI-PDH Control Register. In addition, output signal polarity control is provided by the TPNINV bit in the S/UNI-PDH Control Register. Finally, both TPOS and TDAT can be updated on the rising edge of TICLK, enabled by the TICLK bit in the S/UNI-PDH Control Register.

TNEG/	Output	32	39	**Transmit Negative Pulse (TNEG).** TNEG contains the negative pulses transmitted on the B3ZS-encoded DS3, or HDB3-encoded E3, transmission system when the dual-rail NRZ output format is selected. TNEG indicates the location of the M-frame boundary for DS3, and indicates the position of the frame boundary for E3, when the single-rail (unipolar) NRZ input format is enabled. The dual-rail/single-rail selection is controlled by the TUNI bit in the S/UNI-PDH Control Register.
TOHM				**Transmit Overhead Mask (TOHM).** TOHM indicates the position of overhead bits (non-payload bits) in the transmit transmission system stream, TDAT. When an internally masked signal is transmitted (the EXT bit in the SPLT is cleared), TOHM indicates the frame alignment bit positions based on the internal time slot counter synchronized by a TIOHM pulse. When an externally masked signal is transmitted (the EXT bit in the SPLT is set), TOHM is a delayed version of the TIOHM input, and indicates the position of each overhead bit in the transmission frame. The TNEG/TOHM pin function selection is controlled by the FRMRBP bit in the S/UNI-PDH Configuration Register. Both TNEG and TOHM are updated on the falling edge of TCLK by default and may be enabled to be updated on the rising edge of TCLK. This is controlled by the TCLKINV bit in the S/UNI-PDH Control Register. In addition, output signal polarity control is provided by the TPNINV bit in the S/UNI-PDH Control Register. Finally, both TNEG and TOHM can be updated on the rising edge of TICLK, enabled by the TICLK bit in the S/UNI-PDH Control Register.

TOHCLK	Output	33	40	**Transmit Overhead Clock (TOHCLK).** TOHCLK is active when a DS3 or E3 stream is being processed. TOHCLK is nominally a 526 kHz clock for DS3, is nominally a 1.072 MHz clock for G.832 E3, and is nominally a 1.074 MHz clock for G.751 E3. TOHFP is updated on the falling edge of TOHCLK. TOH, and TOHINS are sampled on the rising edge of TOHCLK.
TOH	Input	41	45	**Transmit DS3/E3 Overhead Data (TOH).** TOH contains the overhead bits (C, F, X, P, and M) that may be inserted in the transmit DS3 stream; TOH contains the overhead bytes (FA1, FA2, EM mask, TR, MA, NR, and GC) that may be inserted in the transmit G.832 E3 stream; TOH contains the overhead bits (RAI, National Use, Stuff Indication, and Stuff Opportunity) that may be inserted in the transmit G.751 E3 stream. TOH is sampled on the rising edge of TOHCLK.
TOHFP	Output	34	41	**Transmit DS3/E3 Overhead Frame Position (TOHFP).** TOHFP is used to align the individual overhead bits in the transmit overhead data stream, TOH, to the DS3 M-frame or the E3 frame. For DS3, TOHFP is high during the X1 overhead bit position in the TOH stream. For G.832 E3, TOHFP is high during the first bit of the FA1 byte. For G.751 E3, TOHFP is high during the RAI overhead bit position in the TOH stream. TOHFP is updated on the falling edge of TOHCLK.
TOHINS	Input	39	44	**Transmit DS3/E3 Overhead Insertion (TOHINS).** TOHINS controls the insertion of the DS3 or E3 overhead bits from the TOH input. When TOHINS is high, the associated overhead bit in the TOH stream is inserted in the transmitted DS3 or E3 frame. When TOHINS is low, the DS3 or E3 overhead bit is generated and inserted internally. TOHINS is sampled on the rising edge of TOHCLK.

TDLSIG	Input	35	n/a	**Transmit Data Link Signal (TDLSIG).** In DS3 mode, TDLSIG contains the Path Maintenance Data Link signal that may be inserted in the C-bit Parity DS3 stream if the TNETOP bit in the S/UNI-PDH Data Link Control register is set to logic one. In E3 G.832 mode, TDLSIG contains the NR or GC data link signal, as selected by the TNETOP bit, that may be inserted in the transmit G.832 E3 stream. In E3 G.751 mode, TDLSIG contains the National Use bit that may be inserted in the G.751 E3 stream if the TNETOP bit is set to logic one. TDLSIG is sampled on the rising edge of TDLCLK. TDLSIG contains an integral pull-up resistor.
TDLCLK	Output	36	n/a	**Transmit Data Link Clock (TDLCLK).** TDLCLK is active when a DS3 or E3 G.751 stream is being processed, if the TNETOP bit in the S/UNI-PDH Data Link Control register is set to logic one. TDLCLK is active when an E3 G.832 stream is being processed, independent of the TNETOP bit.
TPOHCLK	Output	42	46	**Transmit PLCP Overhead Clock (TPOHCLK).** TPOHCLK is active when PLCP processing is enabled. TPOHCLK is nominally a 26.7 kHz clock for a DS1 PLCP frame, a 768 kHz clock for a DS3 PLCP frame, a 33.7 kHz clock for an E1 based PLCP frame, and a 576 kHz clock for an G.751 E3 based PLCP frame. TPOHFP is updated on the falling edge of TPOHCLK. TPOH, and TPOHINS are sampled on the rising edge of TPOHCLK.
TPOH	Input	45	49	**Transmit PLCP Overhead Data (TPOH).** TPOH contains the PLCP path overhead octets (Zn, F1, B1, G1, M1, M2, and C1) which may be inserted in the transmit PLCP frame. The octet data on TPOH is shifted in order from the most significant bit (bit 1) to the least significant bit (bit 8).TPOH is sampled on the rising edge of TPOHCLK.

TPOHFP	Output	43	47	**Transmit Path Overhead Frame Position (TPOHFP).** The TPOHFP output locates the individual PLCP path overhead bits in the transmit overhead data stream, TPOH. TPOHFP is logic 1 while bit 1 (the most significant bit) of the path user channel octet (F1) is present in the TPOH stream. TPOHFP is updated on the falling edge of TPOHCLK.
TPOHINS	Input	44	48	**Transmit Path Overhead Insertion (TPOHINS).** TPOHINS controls the insertion of PLCP overhead octets on the TPOH input. When TPOHINS is logic 1, the associated overhead bit in the TPOH stream is inserted in the transmit PLCP frame. When TPOHINS is logic 0, the PLCP path overhead bit is generated and inserted internally. TPOHINS is sampled on the rising edge of TPOHCLK. Note, when operating in G.751 E3 PLCP mode, bits 8, 7 and 6 of the C1 octet should not be manipulated.

C13/CADD	Input	29	36	**Transmit Stuff Control (C13/CADD).** C13/CADD controls stuffing when configured for DS3 or G.751 E3 PLCP frame formats and when the 8KREF bit in the S/UNI-PDH Control Register is set to logic 0. When DS3 PLCP format is enabled, C13/CADD determines whether to use a 13 or 14 nibble trailer at the next stuff opportunity. When logic 0, a 14 nibble trailer is used. When logic 1, a 13 nibble trailer is used. When G.751 E3 PLCP format is enabled, C13/CADD determines whether to add or subtract one octet from the internally generated octet stuff pattern at the next stuff opportunity. When logic 0, one octet is subtracted from the next 18, 19, or 20 octet trailer. When logic 1, one octet is added to the next 18, 19, or 20 octet trailer. C13/CADD is internally synchronized and thus can be asynchronous.
8KREF				**8 kHz Reference Input (8KREF).** The PLCP frame rate can be locked to an external 8 kHz reference applied on this input when the 8KREF bit in the S/UNI-PDH Control Register is set to logic 1. An internal phase-frequency detector compares the transmit PLCP frame rate with the externally applied 8 kHz reference and adjusts the PLCP frame rate by taking control over the internal C13/CADD signal. The 8KREF input must transition high once every 125 µs for correct operation. The 8KREF input is treated as an asynchronous signal and must be "glitch-free". The minimum high or low period of the 8KREF pin is 20 ns. Only the rising edge is used.
SYFIFOB	Input	40	n/a	**Synchronous FIFO Enable (SYFIFOB).** This active low signal selects between the synchronous and asynchronous FIFO interfaces on the system side. This signal is available only in the 100-pin PQFP package and must be tied to VSS to enable the synchronous FIFO interface. SYFIFOB is not available in the 84-pin PLCC package and is pulled to logic 1 internally by an integral pull-up resistor, thus selecting the asynchronous FIFO interface.

INTB	Output	96	7	**Interrupt (INTB).** The active low interrupt is activated when an unmasked interrupt is detected on any of the internal interrupt sources. The INTB signal is removed when the interrupt is acknowledged by reading the associated interrupt status register. The INTB output is open drain.
CSB	Input	98	9	**Chip Select (CSB).** The active low chip select is low to enable S/UNI-PDH register accesses. If CSB is not required (i.e., register accesses are controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O I/O I/O I/O I/O I/O I/O I/O	20 19 18 17 10 9 8 7	28 27 26 25 20 19 18 17	**Bidirectional Data Bus (D[7:0]).** D[7:0] is used during S/UNI-PDH read and write accesses.
RDB	Input	100	11	**Read Enable (RDB).** The active low read enable is pulsed low to enable a S/UNI-PDH register read access. The S/UNI-PDH drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
WRB	Input	99	10	**Write Strobe (WRB).** The active low write strobe is pulsed low to enable a S/UNI-PDH register write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB while CSB is low.
ALE	Input	2	12	**Address Latch Enable (ALE).** The address latch enable latches the address bus, A[7:0], when logic 0. When ALE is logic 1, the address latches are transparent. ALE contains an integral pullup resistor.
RSTB	Input	97	8	**Reset (RSTB).** The active low schmitt triggered reset asynchronously resets the S/UNI-PDH. RSTB contains an integral pullup resistor. A minimum assertion interval of 100 nsec is recommended.

A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input Input Input Input Input Input Input Input	24 23 22 21 6 5 4 3	32 31 30 29 16 15 14 13	**Address Bus (A[7:0]).** The address bus (A[7:0) selects specific registers during accesses.
VDDO[0] VDDO[1] VDDO[2] VDDO[3]	Power Power Power Power	11 37 64 87	21 42 65 84	**Pad Ring Power (VDDO[3:0]).** These pins must be connected to a common, well decoupled +5 VDC supply together with the VDDI[2:0] pins. Care must be taken to avoid coupling noise induced on the VDDO pins into the VDDI pins.
VDDI[0] VDDI[1] VDDI[2]	Power Power Power	14 15 60	23 n/a 62	**Core Power (VDDI[2:0]).** These pins must be connected to a common, well decoupled +5 VDC supply together with the VDDO[3:0] pins.
VSSO[0] VSSO[1] VSSO[2] VSSO[3] VSSO[4]	Ground Ground Ground Ground Ground	16 38 63 85 75	24 43 64 83 n/a	**Pad Ring Ground (VSSO[4:0]).** These pins must be connected to a common ground together with the VSSI[2:0] pins. Care must be taken to avoid coupling noise induced on the VSSO pins into the VSSI pins.
VSSI[0] VSSI[1] VSSI[2]	Ground Ground Ground	12 13 61	22 n/a 63	**Core Ground (VSSI[2:0]).** These pins must be connected to a common ground together with the VSSO[4:0] pins.

Notes on Pin Description:

1. Most S/UNI-PDH inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels. The high speed inputs, RCLK, RPOS/RDAT, RNEG/ROHM, TICLK, C13/CADD, and TIOHM inputs operate at CMOS logic levels. The ALE, RSTB, TSEN, TDLSIG, TXPRTY, and SYFIFOB inputs have pullups. The RRDENB and TWRENB inputs have integral pull-down resistors. RSTB uses a schmitt trigger input.

2. The TCLK, TPOS/TDAT, TNEG/TOHM, RSOC, REOH, REOC, RFIFOE, TFIFOFB outputs, and the FRDATA[7:0] and RXPRTY tristate outputs have non slew-rate limited 2 mA drive capability. The D[7:0] bidirectionals and INTB have 4 mA slew-rate limited drive capability. All other S/UNI-PDH digital outputs have 2 mA slew-rate limited drive capability.

3. The VSSO and VSSI ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-PDH.

4. The VDDO and VDDI power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the S/UNI-PDH.

9 FUNCTIONAL DESCRIPTION

9.1 DS3 Framer

The DS3 Framer (T3-FRMR) Block integrates circuitry required for decoding a B3ZS-encoded signal and framing to the resulting DS3 bit stream. The T3-FRMR is directly compatible with the M23 and C-bit parity DS3 applications.

The T3-FRMR decodes a B3ZS-encoded signal and provides indications of line code violations. The B3ZS decoding algorithm and the LCV definition can be independently chosen through software. A loss of signal (LOS) defect is also detected for B3ZS encoded streams. LOS is declared when inputs RPOS and RNEG contain zeros for 175 consecutive RCLK cycles. LOS is removed when the ones density on RPOS and/or RNEG is greater than 33% for 175 ±1 RCLK cycles.

The framing algorithm examines five F-bit candidates simultaneously. When at least one discrepancy has occurred in each candidate, the algorithm examines the next set of five candidates. When a single F-bit candidate remains in a set, the first bit in the supposed M-subframe is examined for the M-frame alignment signal (i.e., the M-bits, M1, M2, and M3 are following the 010 pattern). Framing is declared, and out-of-frame is removed, if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. During the examination of the M-bits, the X-bits and P-bits are ignored. The algorithm gives a maximum average reframe time of 1.5 ms.

While the T3-FRMR is synchronized to the DS3 M-frame, the F-bit and M-bit positions in the DS3 stream are examined. An out-of-frame defect is detected when 3 F-bit errors out of 8 or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration Register), or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. The M-bit error criteria for OOF can be disabled by the MBDIS bit in the DS3 Framer Configuration register. The 3 out of 8 consecutive F-bits out-of-frame ratio provides more robust operation, in the presence of a high bit error rate, than the 3 out of 16 consecutive F-bits ratio. Either out-of-frame criteria allows an out-of-frame defect to be detected quickly when the M-subframe alignment patterns or, optionally, when the M-frame alignment pattern is lost.

Also while in-frame, line code violations, M-bit or F-bit framing bit errors, and P-bit parity errors are indicated. When C-bit parity mode is enabled, both C-bit parity errors and far end block errors are indicated. These error indications, as well as the line code violation and excessive zeros indication, are accumulated over 1 second intervals with the Performance Monitor (PMON). Note that the framer is an off-line

framer, indicating both OOF and COFA events. Even if an OOF is indicated, the framer will continue indicating performance monitoring information based on the previous frame alignment.

Three DS3 maintenance signals (a RED alarm condition, the alarm indication signal, and the idle signal) are detected by the T3-FRMR. The maintenance detection algorithm employs a simple integrator with a 1:1 slope that is based on the occurrence of "valid" M-frame intervals. For the RED alarm, an M-frame is said to be a "valid" interval if it contains a RED defect, defined as an occurrence of an OOF or LOS event during that M-frame. For AIS and IDLE, an M-frame interval is "valid" if it contains AIS or IDLE, defined as the occurrence of less than 15 discrepancies in the expected signal pattern (1010... for AIS, 1100... for IDLE) while valid frame alignment is maintained. This discrepancy threshold ensures the detection algorithms operate in the presence of a 10^{-3} bit error rate. For AIS, the expected pattern may be selected to be: the framed "1010" signal; the framed arbitrary DS3 signal and the C-bits all zero; the framed "1010" signal and the C-bits all zero; the framed all-ones signal (with overhead bits ignored); or the unframed all-ones signal (with overhead bits equal to ones). Each "valid" M-frame causes an associated integration counter to increment; "invalid" M-frames cause a decrement. With the "slow" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 127, which results in a detection time of 13.5 ms. With the "fast" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 21, which results in a detection time of 2.23 ms (i.e., 1.5 times the maximum average reframe time). RED, AIS, or IDLE are removed when the respective counter decrements to 0.

Valid X-bits are extracted by the T3-FRMR to provide indication of far end receive failure (FERF). A FERF defect is detected if the extracted X-bits are equal and are logic 0 (X1=X2=0); the defect is removed if the extracted X-bits are equal and are logic 1 (X1=X2=1). If the X-bits are not equal, the FERF status remains in its previous state. The extracted FERF status is buffered for 2 M-frames before being reported within the DS3 FRMR Status register. This buffer ensures a better than 99.99% chance of freezing the FERF status on a correct value during the occurrence of an out of frame.

When the C-bit parity application is enabled, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted. Codes in the FEAC channel are detected by the Bit Oriented Code Detector (RBOC). HDLC messages in the Path Maintenance Data Link are received by the Data Link Receiver (RFDL) and brought out to the RDLSIG output with an associated clock on RDLCLK. RDLSIG and RDLCLK are available only in the 100-pin PQFP package.

The T3-FRMR can be enabled to automatically assert the RAI indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or RED,

or AIS. When C-Bit parity is selected, the T3-FRMR automatically inserts C-Bit parity FEBE upon detection of receive C-Bit parity error.

The T3-FRMR extracts the entire DS3 overhead (56 bits per M-frame) using the ROH output, along with the ROHCLK, and ROHFP outputs.

The T3-FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the T3-FRMR. Access to these registers is via a generic microprocessor bus.

9.2 E3 Framer

The E3 Framer (E3-FRMR) Block integrates circuitry required for decoding an HDB3-encoded signal and framing to the resulting E3 bit stream. The E3-FRMR is directly compatible with the G.751 and G.832 E3 applications.

The E3-FRMR searches for frame alignment in the incoming serial stream based on either the G.751 or G.832 formats. Regardless of format selected, the E3-FRMR expects to see the selected framing pattern error-free for three consecutive frames before declaring INFRAME. Once the frame alignment is established, the incoming data is continuously monitored for framing bit errors and byte interleaved parity errors (in G.832 format).

While in-frame, the E3-FRMR also extracts various overhead bytes and processes them according to the framing format selected:

- in G.832 E3 format, the E3-FRMR extracts:
  - the Trail Trace bytes and outputs them as a serial stream for further processing by the Trail Trace Buffer (TTB) block;
  - the FERF bit and indicates an alarm when the FERF bit is a logic 1 for 3 or 5 consecutive frames. The FERF indication is removed when the FERF bit is a logic 0 for 3 or 5 consecutive frames;
  - the FEBE bit and outputs it for accumulation in PMON;
  - the Payload Type bits and buffers them so that they can be read by the microprocessor;
  - the Timing Marker bit and asserts the Timing Marker indication when the value of the extracted bit has been in the same state for 3 or 5 consecutive frames;

- the Network Operator byte and presents it as a serial stream for further processing by the RFDL block when the RNETOP bit in the S/UNI-PDH Data Link and FERF Control register is logic 1; otherwise, the byte is brought out on the RDLSIG output with an associated clock on RDLCLK. RDLSIG and RDLCLK are available only in the 100-pin PQFP package. When not configured for Tandem Connection Maintenance, all 8 bits of the Network Operator byte are extracted and presented on the overhead output and, optionally, presented to the RFDL. When configured for Tandem Connection, the first four bits of the byte identify the incoming error count (IEC) and are accumulated in the PMON. The last four bits of the byte are output on the overhead stream and, optionally, presented to the RFDL. However, it is not envisioned that the Tandem Connection Maintenance mode will be used in S/UNI-PDH applications;
- the General Purpose Communication Channel byte and presents it to the RFDL when the RNETOP bit in the S/UNI-PDH Data Link and FERF Control register is logic 0; otherwise, the byte is brought out on the RDLSIG output with an associated clock on RDLCLK. RDLSIG and RDLCLK are available only in the 100-pin PQFP package.

• in G.751 E3 mode, the E3-FRMR extracts:
  - the Remote Alarm Indication bit (bit 11 of the frame) and indicates a Remote Alarm when the RAI bit is a logic 1 for 3 or 5 consecutive frames. Similarly, the Remote Alarm is removed when the RAI bit is logic 0 for 3 or 5 consecutive frames;
  - the National Use reserved bit (bit 12 of the frame) and presents it as a serial stream for further processing in the RFDL when the RNETOP bit in the S/UNI-PDH Data Link and FERF Control register is logic 0; otherwise, the bit is brought out on the RDLSIG output with an associated clock on RDLCLK. RDLSIG and RDLCLK are available only in the 100-pin PQFP package. Optionally, an interrupt can be generated when the National Use bit changes state.

Further, while in-frame, the E3-FRMR indicates the position of all the overhead bits in the incoming digital stream to the ATMF/SPLR block. For G.751 mode, the tributary justification bits can optionally be identified as either overhead or payload for payload mappings that take advantage of the full bandwidth.

The E3-FRMR declares a loss of frame alignment if the framing pattern is in error for four consecutive frames. The E3-FRMR is an "off-line" framer, where all frame alignment indications, all overhead bit indications, and all overhead bit processing continue based on the previous alignment. Once the framer has determined the new frame alignment, the out-of-frame indication is removed and a COFA indication is declared if the new alignment differs from the previous alignment.

The E3-FRMR detects the presence of AIS in the incoming data stream when less than 8 zeros in a frame are detected while the framer is OOF in G.832 mode, or when less than 5 zeros in a frame are detected while OOF in G.751 mode. This algorithm provides a probability of detecting AIS in the presence of a 10^{-3} BER as 92.9% in G.832 and 98.0% in G.751.

Loss of signal is LOS is declared when no marks have been received for 32 consecutive bit periods. Loss of signal is deasserted after 32 bit periods during which there is no sequence of four consecutive zeros.

The E3-FRMR can also be enabled to automatically assert the RAI/FERF indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or AIS. The E3-FRMR can also be enabled to automatically insert G.832 FEBE upon detection of receive BIP-8 errors.

9.3 PMON Performance Monitor Accumulator

The Performance Monitor (PMON) Block interfaces directly with either the DS3 Framer (T3-FRMR) to accumulate line code violation (LCV) events, parity error (PERR) events, path parity error (CPERR) events, far end block error (FEBE) events, and framing bit error (FERR) events using saturating counters; or the E3-FRMR to accumulate LCV, PERR (in G.832 mode), FEBE, FERR, and incoming error counts (IEC) in G.832 Tandem Connection mode. Due to the off-line nature of the DS3 or E3 Framers, PMON continues to accumulate performance meters even while the T3-FRMR or the E3-FRMR has declared OOF.

When an accumulation interval is signalled by a write to the PMON register address space or a write to the CPPM register address space, the PMON transfers the current counter values into microprocessor accessible holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

When counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled. If the holding registers have not been read since the last interrupt, an overrun status bit is set. In addition, a register is provided to indicate changes in the PMON counters since the last accumulation interval.

9.4 RBOC Bit-Oriented Code Detector

Bit-Oriented Code Detector is only use in T3 C-bit Parity mode.

The Bit-Oriented Code Detector (RBOC) Block detects the presence of 63 of the 64 possible bit-oriented codes (BOCs) contained in the C-bit parity far-end alarm and control (FEAC) channel. The 64th code ("111111") is similar to the HDLC flag sequence and is ignored.

Bit-oriented codes (BOCs) are received on the FEAC channel as 16-bit sequences each consisting of 8 ones, a zero, 6 code bits, and a trailing zero ("111111110xxxxxx0"). BOCs are validated when repeated at least 10 times. The RBOC can be enabled to declare a code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable Register. The RBOC declares that the code is removed if two code sequences containing code values different from the detected code are received in a moving window of ten code periods.

Valid BOCs are indicated through the RBOC Interrupt Status Register. The BOC bits are set to all ones ("111111") when no valid code is detected. The RBOC can be programmed to generate an interrupt when a detected code has been validated and when the code is removed.

9.5 RFDL Facility Data Link Receiver

The Facility Data Link Receiver (RFDL) Block is a microprocessor peripheral used to receive LAPD/HDLC frames on the DS3 C-bit parity Path Maintenance Data Link, on the E3 G.832 Network Requirement byte or the General Purpose data link (selectable using the RNETOP bit in the S/UNI-PDH Data Link and FERF Control register), or on the G.751 Network Use bit.

The RFDL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives frame data, and calculates the CRC-CCITT frame check sequence (FCS).

Received data is placed into a 4-byte FIFO buffer. The RFDL Status Register contains bits which indicate overrun, end of message, flag detected, and buffered data available.

On end of message, the RFDL Status Register also indicates the FCS status and the number of valid bits in the final data byte. Interrupts are generated when one, two or three (programmable count) bytes are stored in the FIFO buffer. Interrupts are also generated when the terminating flag sequence, abort sequence, or FIFO buffer overrun are detected.

9.6 SPLR PLCP Layer Receiver

The PLCP Layer Receiver (SPLR) Block integrates circuitry to support DS1, DS3, E1, and G.751 E3 PLCP frame processing. The SPLR provides framing for PLCP based transmission formats.

The SPLR frames to a DS1, DS3, E1, and G.751 E3 based PLCP frames with maximum average reframe times of 635 µs, 22 µs, 483 µs, and 32 µs respectively. Framing is declared (out of frame is removed) upon finding 2 valid, consecutive sets of framing (A1 and A2) octets and 2 valid and sequential path overhead identifier (POHID) octets. While framed, the A1, A2, and POHID octets are examined. OOF is declared when an error is detected in both the A1 and A2 octets or when 2 consecutive POHID octets are found in error. LOF is declared when an OOF state persists for more than 25 ms, 1 ms, 20 ms, or 1 ms for DS1, DS3, E1, or G.751 E3 PLCP formats respectively. When OOF is cleared, the LOF counter is decremented at a rate 1/12 (DS3 PLCP), 1/10 (E1, DS1 PLCP) or 1/9(G.751 E3 PLCP) of the incrementing rate. LOF is thus removed when an in-frame state persists for more than 250 ms for a DS1 signal, 12 ms for a DS3 signal, 200 ms for an E1 signal, or 9 ms for a G.751 E3 signal. When LOF is declared, PLCP reframe is initiated.

When in frame, the SPLR extracts the path overhead octets and outputs them bit serially on output RPOH, along with the RPOHCLK and RPOHFP outputs. Framing octet errors and path overhead identifier octet errors are indicated as frame errors. Bit interleaved parity errors and far end block errors are indicated. The yellow signal bit is extracted and accumulated to indicate yellow alarms. Yellow alarm is declared when 10 consecutive yellow signal bits are set to logical 1; it is removed when 10 consecutive received yellow signal bits are set to logical 0. The C1 octet is examined to maintain nibble alignment with the incoming transmission system sublayer bit stream.

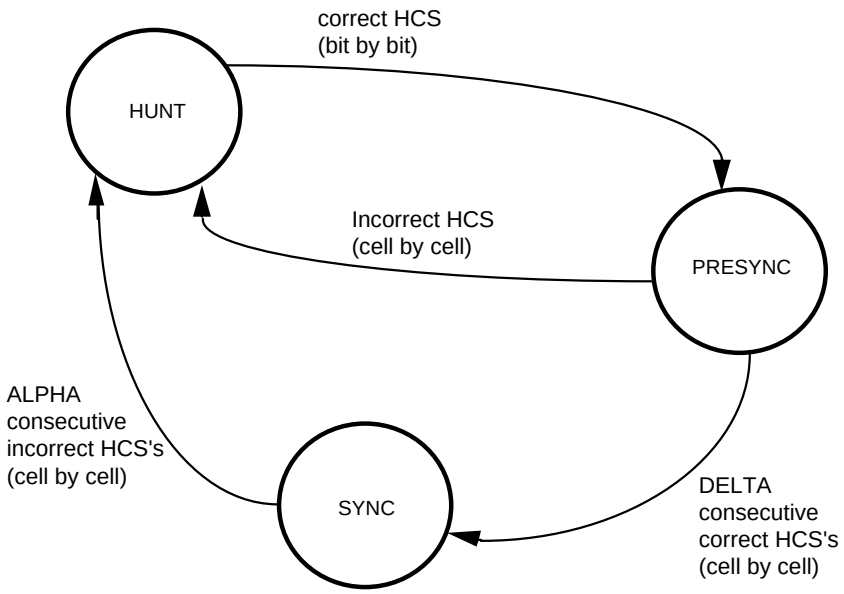
9.7 ATMF ATM Cell Delineator

The ATM Cell Delineator (ATMF) Block integrates circuitry to support HCS-based cell delineation for non-PLCP based transmission formats. The ATMF block accepts a bit serial cell stream from an upstream transmission system sublayer entity (such as the T3-FRMR or E3-FRMR Block) and converts the stream into a byte serial format. Cell delineation is used to locate to the cell boundaries.

Cell delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the ATM cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries.

The ATMF performs a sequential bit by bit hunt for a correct HCS sequence. This state is referred to as the HUNT state. When a correct HCS is found, the ATMF locks on the particular cell boundary and assumes the PRESYNC state. This state verifies that the previously detected HCS pattern was not a false indication. If the HCS pattern was a false indication then an incorrect HCS should be received within the next DELTA cells. At that point a transition back to the HUNT state is executed. If an incorrect HCS is not found in this PRESYNC period then a transition to the SYNC state is made. In this state synchronization is not relinquished until ALPHA consecutive incorrect HCS patterns are found. In such an event a transition is made back to the HUNT state. The state diagram of the cell delineation process is shown in figure 3.

Figure 3 - Cell delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6 as recommended in ITU-T Recommendation I.432. These values result in a maximum average time to frame of 500 µs for a DS3 stream carrying ATM cells directly mapped into the DS3 information payload.

Loss of cell delineation (LCD) is detected by counting the number of incorrect cells while in the HUNT state. The counter value is stored in the RXCP LCD Count Threshold register. The threshold has a default value of 360 which results in an E3 G.832 application detection time of 4.5 ms, and E3 G.751 application detection time

of 5.0 ms, an E1 application detection time of 77 ms, a DS3 application detection time of 3.5 ms, and a DS1 application detection time of 100 ms. If the counter value is set to zero, the LCD output signal is asserted for every incorrect cell.

9.8 RXCP Receive Cell Processor

The Receive Cell Processor (RXCP) Block integrates circuitry to support cell payload descrambling, header check sequence (HCS) verification and idle/unassigned cell filtering.

The RXCP operates upon a delineated cell stream. For PLCP based transmissions systems, cell delineation is performed by the SPLR. For non-PLCP based transmission systems, cell delineation is performed by the ATMF. Framing status indications from these blocks ensure that cells are not written to the RXFF while the SPLR is in the loss of frame state, or cells are not written to the RXFF while the ATMF is in the HUNT or PRESYNC states.

The RXCP descrambles the cell payload field using the self synchronizing descrambler with a polynomial of $x^{43} + 1$. The header portion of the cells is not descrambled. Note that cell payload scrambling is optional in the S/UNI-PDH, yet is required by ITU-T Recommendation I.432. The ATM Forum DS3 UNI specification requires that cell payloads are unscrambled for the DS3 physical layer interface (however, discussions are ongoing to make scrambling a requirement in the future).

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RXCP verifies the received HCS using the accumulation polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432.

The RXCP can be programmed to drop all cells containing an HCS error or to filter cells based on the HCS and/or the 4 octet cell header. Filtering according to a particular HCS and/or 4 octet header pattern is programmable through the RXCP configuration/control registers. More precisely, filtering is performed when filtering is enabled or when HCS errors are found when HCS checking is enabled. Otherwise, all cells are passed on regardless of any error conditions. Cells are blocked if the HCS pattern is invalid or if the filtering 'Match Pattern' and 'Match Mask' registers are programmed with a certain blocking pattern. Idle cells are not automatically filtered. If they are required to be filtered, then that filtering criterion (i.e. the Null cell pattern) must be programmed through the IDLE/Unassigned Cell Pattern and Mask registers. For direct mapped or PLCP mapped ATM cells, Null cells (Idle cells) are identified by the standardized header pattern of 'H00, 'H00, 'H00 and 'H01 in the first 4 octets followed by the valid HCS octet. When operating in a DQDB system the

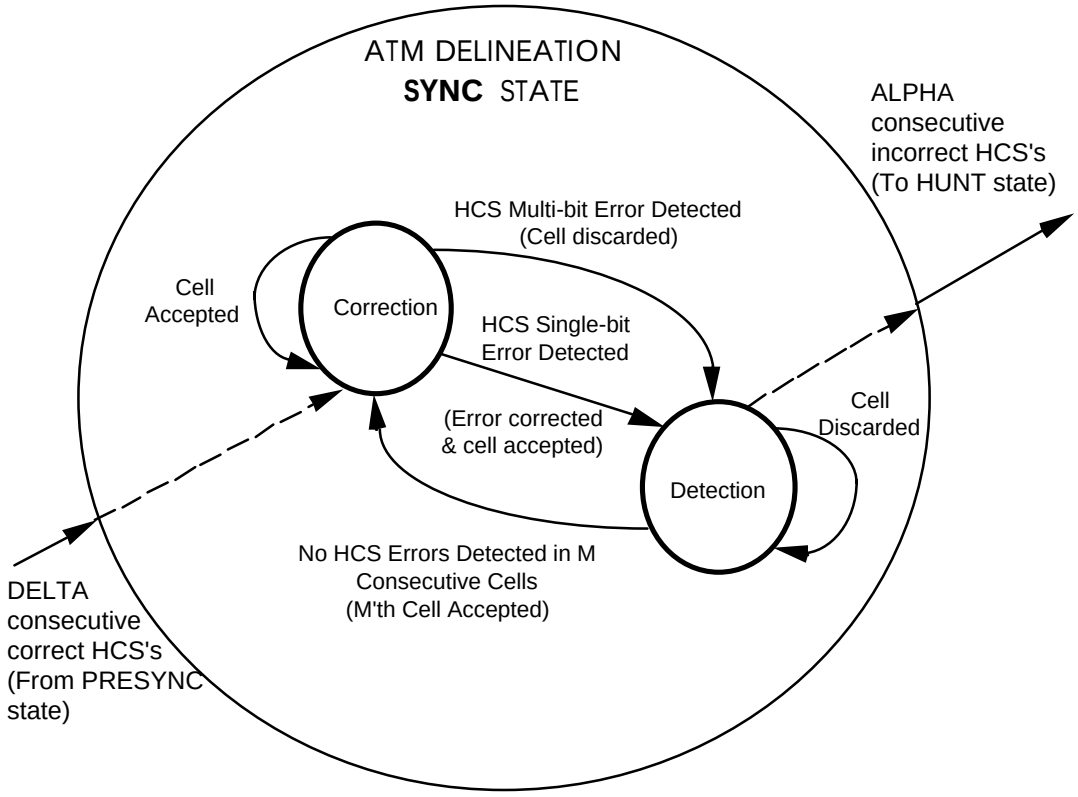
PLCP 'Null cell' (Idle cell) slots are identified by the standardized header pattern of 'B0xxxxxx, 'H00, 'H00, 'H00 in the first 4 octets followed by the valid HCS octet. The 7 “don’t care” x bits of the first byte of the header are handled by leaving these bits cleared in the appropriate header Idle/Unassigned Cell Mask register.

While the cell delineation state machine is in the SYNC state, the HCS verification circuit implements the state machine shown in "Figure 4 HCS Verification State Diagram."

In normal operation, the HCS verification state machine remains in the 'Correction' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single-bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single-bit error or a multi-bit error, the state machine transitions to the 'Detection' state.

A programmable hysteresis is provided when dropping cells based on HCS errors. When a cell with an HCS error is detected, the RXCP can be programmed to continue to discard cells until m (where m = 1, 2, 4, 8) cells are received with correct HCS. The value of m is selected by writing the DETHYST[1:0] bits located in the RXCP Framing control register (0x41H). The mth cell is not discarded (see figure 4). Note that the dropping of cells due to HCS errors only occurs while the ATMF is in the SYNC state (for non-PLCP based transmission systems), or while the SPLR is in the in-frame state (for PLCP based transmission systems).

Figure 4 - HCS Verification State Diagram



9.9 RXFF Receive FIFO

The Receive FIFO (RXFF) provides FIFO management and the S/UNI-PDH receive cell interface. The receive FIFO contains four cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include filling the receive FIFO, indicating when the receive FIFO contains cells, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions.

When using the asynchronous FIFO interface (in the 84-pin PLCC, or in the 100-pin PQFP when SYFIFOB is tied high), the FIFO is automatically reset upon detection of an overrun or underrun condition. Up to four cells may be lost during the FIFO reset operation. FIFO overruns and underruns are indicated via a maskable interrupt and register bits. This asynchronous interface also indicates the FIFO status (RFIFOE), the start of cell (RSOC), the end of the cell header (REOH), and the end of the cell (REOC) when data is read from the receive FIFO using FRDB. The FIFO status changes from empty to full on write cell boundaries with timing

derived from the receive line clock (RCLK). The FIFO status changes from full to empty (or almost empty, when REMPTY4 is logic 1) on read cell boundaries with timing aligned to the FIFO read clock (FRDB).

The synchronous FIFO interface is provided in the 100-pin PQFP package when SYFIFOB is tied to logic 0. This interface is "UTOPIA" compliant and accepts a read clock (RFCLK) and read enable signal (RRDENB). The receive FIFO output bus (FRDATA[7:0]) can be tristated when RRDENB is logic 1 if enabled by the TSEN pin. The interface indicates the start of a cell (RSOC), the end of the cell header (REOH), the end of the cell (REOC), and the receive cell available status (RCA) when data is read from the receive FIFO (using the rising edges of RFCLK while RRDENB is logic 0). The RCA status changes from available to unavailable when the FIFO is 4 byte reads away from being empty (or when the FIFO is empty, when REMPTY4 is logic 0). This interface also indicates FIFO overruns and underruns via a maskable interrupt and register bits, but, unlike the asynchronous interface, further read accesses while RCA is logic 0 are ignored (i.e., the FIFO is not reset on FIFO underrun). The FIFO is still reset on FIFO overrun, causing up to 4 cells to be lost.

9.10 CPPM Cell and PLCP Performance Monitor

The Cell and PLCP Performance Monitor (CPPM) Block interfaces directly with the RXCP, SPLR, and TXCP to accumulate bit interleaved parity error events, framing octet error events, far end block error events, header check sequence error events, the number of received unassigned/idle cells, the number of received assigned cells, and the number of transmitted assigned cells in saturating counters. When the PLCP framer (SPLR) declares loss of frame or when the ATM cell delineator (ATMF) declares out of delineation, bit interleaved parity error events, framing octet error events, far end block error events, header check sequence error events are not counted.

When an accumulation interval is signalled by a write to the PMON register address space or a write to the CPPM register address space, the CPPM transfers the current counter values into holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

9.11 DS3 Transmitter

The DS3 Transmitter (T3-TRAN) Block integrates circuitry required to insert the overhead bits into a DS3 bit stream and produce a B3ZS-encoded signal. The T3-TRAN is directly compatible with the M23 and C-bit parity DS3 formats.

Status signals such as far end receive failure (FERF), the alarm indication signal, and the idle signal can be inserted when their transmission is enabled by internal register bits. FERF can also be automatically inserted on detection of any combination of LOS, OOF or RED, or AIS by the T3-FRMR.

A valid pair of P-bits is automatically calculated and inserted by the T3-TRAN. When C-bit parity mode is selected, the path parity bits, and far end block error (FEBE) indications are automatically inserted.

When enabled for C-bit parity operation, the FEAC channel is sourced by the XBOC bit-oriented code transmitter. The TNETOP bit in the S/UNI-PDH Data Link and FERF Control register controls the source of the path maintenance data link. If TNETOP is logic 0, the path maintenance data link messages are sourced by the XFDL data link transmitter. If TNETOP is a logic 1, the path maintenance data link messages are sourced from the TDLSIG input pin with an associated clock on TDLCLK. TDLSIG and TDLCLK are only available in the 100-pin PQFP package.

When enabled for M23 operation, the C-bits are forced to logic 1 with the exception of the C-bit Parity ID bit (first C-bit of the first M-subframe), which is forced to toggle every M-frame.

The T3-TRAN supports diagnostic modes in which it inserts parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, or all-zeros.

User control of each of the overhead bits in the DS3 frame is provided. Overhead bits may be inserted on a bit-by-bit basis from a user supplied data stream. An overhead clock (at 526 kHz) and a DS3 overhead alignment output are provided to allow for control of the user provided stream.

9.12 E3 Transmitter

The E3 Transmitter (E3-TRAN) Block integrates circuitry required to insert the overhead bits into an E3 bit stream and produce an HDB3-encoded signal. The E3-TRAN is directly compatible with the G.751 and G.832 framing formats.

The E3-TRAN generates the frame alignment signal and inserts it into the incoming serial stream based on either the G.751 or G.832 formats and an alignment pulse applied to it by the SPLT block. All overhead and status bits in each frame format can be individually controlled by register bits or by the transmit overhead stream. While in certain framing format modes, the E3-TRAN generates various overhead bytes according to the following:

- in G.832 E3 format, the E3-TRAN:

- inserts the BIP-8 byte calculated over the preceding frame;
- inserts the Trail Trace bytes through the Trail Trace Buffer (TTB) block;
- inserts the FERF bit via a register bit or, optionally, when the E3-FRMR declares OOF, or when the loss of cell delineation (LCD) defect is declared;
- inserts the FEBE bit, which is set to logic 1 when one or more BIP-8 errors are detected by the receive framer. If there are no BIP-8 errors indicated by the E3-FRMR, the E3-TRAN sets the FEBE bit to logic 0;
- inserts the Payload Type bits based on the register value set by the microprocessor;
- inserts the Tributary Unit multiframe indicator bits either via the TOH overhead stream or by register bit values set by the microprocessor;
- inserts the Timing Marker bit via a register bit;
- inserts the Network Operator byte from the XFDL block when the TNETOP bit in the S/UNI-PDH Data Link and FERF Control register is logic 1; otherwise, the byte is sourced by the overhead stream on TDLSIG with an associated clock on TDLCLK. TDLSIG and TDLCLK are only available in the 100-pin PQFP package. The Network Operator byte can be split into two nibbles: the upper nibble supporting the IEC for Tandem Connection operation , the lower nibble supporting a half rate datalink. The IEC bits are encoded as zero. S/UNI-PDH applications are not expected to require Tandem Connection; therefore, all 8 bits of the Network Operator byte are available for the datalink;
- inserts the General Purpose Communication Channel byte from the XFDL block when the TNETOP bit in the S/UNI-PDH Data Link and FERF Control register is logic 0; otherwise, the byte is sourced by the overhead stream on TDLSIG with an associated clock on TDLCLK. TDLSIG and TDLCLK are only available in the 100-pin PQFP package.

• in G.751 E3 mode, the E3-TRAN :
  - inserts the Remote Alarm Indication bit (bit 11 of the frame) either via a register bit or, optionally, when the E3-FRMR declares OOF;
  - inserts the National Use reserved bit (bit 12 of the frame) either as a fixed value through a register bit or from the XFDL block when the TNETOP bit in the S/UNI-PDH Data Link and FERF Control register is logic 0; otherwise, the bit is sourced by the overhead stream on TDLSIG with an associated clock on TDLCLK. TDLSIG and TDLCLK are only available in the 100-pin PQFP package.
  - optionally identifies the tributary justification bits and stuff opportunity bits as either overhead or payload to SPLT for payload mappings that take advantage of the full bandwidth.

Further, the E3-TRAN can provide insertion of bit errors in the framing pattern or in the parity bits, and insertion of single line code violations for diagnostic purposes.

9.13 XBOC Bit Oriented Code Generator

The Bit Oriented Code Generator (XBOC) Block transmits 63 of the possible 64 bit oriented codes (BOC) in the C-bit parity Far End Alarm and Control (FEAC) channel. A BOC is a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. The code to be transmitted is programmed by writing the XBOC Code Register. The 64th code (111111) is similar to the HDLC idle sequence and is used to disable the transmission of any bit oriented codes. When transmission is disabled, the FEAC channel is set to all ones.

9.14 XFDL Facility Data Link Transmitter

The Facility Data Link Transmitter (XFDL) provides a serial data link for the C-bit parity path maintenance data link in DS3, the serial Network Operator byte or the General Purpose datalink in G.832 E3, or the National Use bit datalink in G.751 E3. The XFDL is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) is appended, followed by flags. If the XFDL Transmit Data register underflows, an abort sequence is automatically transmitted.

When enabled, the XFDL continuously transmits flags (01111110). Data bytes to be transmitted are written into the XFDL Transmit Data Register. After the parallel-to-serial conversion of each data byte, an interrupt is generated to signal the microprocessor to write the next byte. After the last data frame byte, the FCS (if CRC insertion has been enabled), or a flag (if CRC insertion has not been enabled) is transmitted. The XFDL then returns to the transmission of flag sequences.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the XFDL Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDR signal.

When the XFDL is disabled, a logical 1 is inserted in the path maintenance data link.

9.15 SPLT SMDS PLCP Layer Transmitter

The SMDS PLCP Layer Transmitter (SPLT) Block integrates circuitry to support DS1, DS3, E1, and G.751 E3 based PLCP frame insertion.

The SPLT automatically inserts the framing (A1, A2) and path overhead identification (POHID) octets and provides registers or automatic generation of the F1, B1, G1, M2, M1 and C1 octets.

Registers are provided for the path user channel octet (F1) and the path status octet (G1). The bit interleaved parity octet (B1) and the FEBE subfield are automatically inserted.

The DQDB management information octets, M1 and M2 are generated. The type 0 and type 1 patterns described in TA-TSY-000772 are automatically inserted. The type 1 page counter may be reset using a register bit in the SPLT Configuration register. Note that this feature is not required for the ATM Forum compliant DS3 UNI. For this application, the M1 and M2 octets must be set to all zeros.

The cycle/stuff counter octet, C1, may be controlled using the C13/CADD input, or a fixed stuffing pattern may be inserted. A looped timing operating mode is provided where the transmit PLCP timing is derived from the received timing. In this mode, the C1 stuffing is generated based on the received stuffing pattern as determined by the SPLR block. When DS1 or E1 PLCP format is enabled, the pattern 00H is inserted.

When DS3 PLCP format is enabled, the C1 octet indicates the phase of the 375 µs nibble stuffing opportunity cycle. During frame one of the three frame cycle, the pattern FFH is inserted in the C1 octet, indicating a 13 nibble trailer length. During frame two, the pattern 00H is inserted, indicating a 14 nibble trailer length. During frame three, the pattern 66H or 99H is inserted, indicating a 13 or 14 nibble trailer length respectively. The nibble trailer is set to the binary value 1100.

When configured for G.751 E3 PLCP frame format, the C1 octet is used to indicate the number of octets stuffed in the trailer. The following table shows the C1 octet pattern for each of the possible octet stuff lengths:

Stuff Length	C1(Hex)
17	3B
18	4F
19	75
20	9D
21	A7

The SPLT block generates a stuff length pattern of 18, 19 or 20 octets determined by the phase alignment of the start of the G.751 E3 frame and the start of the E3 PLCP frame. The stuff length may be incremented or decremented by one depending on the value of the C13/CADD input.

The C13/CADD input can be provisioned to loop time the PLCP transmit frame to an externally applied 8 kHz reference.

The Zn, growth octets are set to 00H. The Zn octets may be inserted from an external device via the path overhead stream input, TPOH.

9.16 TXCP Transmit Cell Processor

The Transmit Cell Processor (TXCP) Block integrates circuitry to support ATM cell payload scrambling, header check sequence (HCS) generation, and idle/unassigned cell generation.

The TXCP scrambles the cell payload field using the self synchronizing scrambler with polynomial $x^{43} + 1$. The header portion of the cells is not scrambled. Note that cell payload scrambling is optional in the S/UNI-PDH, and is required by ITU-T Recommendation I.432. The ATM Forum DS3 UNI specification requires that cell payloads are unscrambled for the DS3 physical layer interface (however discussions are ongoing to make scrambling a requirement in the future).

The HCS is generated using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the calculated HCS octet as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432. The resultant octet optionally overwrites the HCS octet in the transmit cell. When the transmit FIFO is empty, the TXCP inserts idle/unassigned cells. The idle/unassigned cell header is fully programmable using five internal registers. Similarly, the 48 octet information field is programmed with an 8 bit repeating pattern using an internal register.

9.17 TXFF Transmit FIFO

The Transmit FIFO (TXFF) provides FIFO management and the S/UNI-PDH transmit cell interface. The transmit FIFO contains four cells. The FIFO depth may be programmed to four, three, two, or one cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include emptying cells from the transmit FIFO, indicating when the transmit FIFO is full, maintaining the transmit FIFO read and write pointers and detecting a FIFO overrun condition.

When using the asynchronous FIFO interface (in the 84-pin PLCC, or in the 100-pin PQFP when SYFIFOB is tied high), the FIFO is automatically reset upon detection of an overrun or underrun condition. Up to four cells may be lost during the FIFO reset operation. FIFO overruns are indicated via a maskable interrupt and a register bit. This asynchronous interface also expects a start of cell indication (TSOC) when the first octet of a 53 octet cell is written into the transmit FIFO. The transmit FIFO write pointer is reset to octet 1 of the 53 octet cell when TSOC is sampled high. During normal operation, TSOC should coincide with octet 1; however, if TSOC is sampled high during any other octet, the current cell write is aborted, and the FIFO write pointer is reset to octet 1 of the current cell. A TSOC out of sync event occurs when TSOC is sampled low during octet 1 of the 53 octet cell, or when TSOC is sampled high during any octet except octet 1. TSOC out of sync events are indicated via a maskable interrupt and a register bit. The asynchronous interface provides an external device with the indication of the full/empty transmit FIFO status (TFIFOFB). By default, the FIFO full indication is asserted when the FIFO is full and can accept no more writes (optionally, the full indication can be selected to indicate when the FIFO is almost full and no more than four writes can be accepted). The FIFO status changes from full to empty on read cell boundaries with timing derived from the transmit line clock (TICLK). The FIFO status changes from empty to full on write cell boundaries with timing aligned to the FIFO write clock (FWRB).

The synchronous FIFO interface is provided in the 100-pin PQFP package when SYFIFOB is tied to logic 0. This interface is “UTOPIA” compliant and accepts a write clock (TFCLK) and write enable signal (TWRENB), and the start of a cell (TSOC) indication when data is written to the transmit FIFO (using the rising edges of TFCLK). The interface provides the transmit cell available status (TCA) which can transition from available to unavailable when the transmit FIFO is near full and can accept no more than 4 more writes (when TFULL4 is logic 1) or when the FIFO is full and can accept no more writes (default). To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells by the FIFODP[1:0] bits of TXCP Control register. If the programmed depth is less than four, more than one cell may be written after TCA is asserted. This interface also indicates FIFO overruns and underruns via a maskable interrupt and register bits, but, unlike the asynchronous interface, further write accesses while TCA is logic 0 are ignored (i.e., the FIFO is not reset on FIFO overrun). Neither is the FIFO reset on FIFO underrun; the TXFF automatically transmits idle/unassigned cells until a full cell is available to be transmitted.

9.18 TTB Trail Trace Buffer

The Trail Trace Buffer (TTB) extracts and sources the trail trace message carried in the TR byte of the G.832 E3 stream. The message is used by the OS to prevent delivery of traffic from the wrong source and is 16 bytes in length. The 16-byte message is framed by the PTI Multiframe Alignment Signal (TMFAS = 'b10000000 00000000). One bit of the TMFAS is placed in the most significant bit of each message byte. In the receive direction, the trail trace message is extracted from the serial overhead stream output by the E3-FRMR. The extracted message is stored in the internal RAM for review by an external microprocessor. By default, the TTB will write the byte of a 16-byte message with its most significant bit set high to the first location in the RAM. The extracted trail trace message is checked for consistency between consecutive multiframes. A message received unchanged three or five times (programmable) is accepted for comparison with the copy previously written into the internal RAM by the external microprocessor. Alarms are raised to indicate reception of unstable and mismatched messages. In the transmit direction, the TTB sources the trail trace message from the internal RAM for insertion into the TR byte by the E3-TRAN.

The TTB also extracts the Payload Type label carried in the MA byte of the G.832 E3 stream. The label is used to ensure that the adaptation function at the trail termination sink is compatible with the adaptation function at the trail termination source. The Payload Type label is check for consistency between consecutive multiframes. A Payload Type label received unchanged for five frames is accepted for comparison with the copy previously written into the TTB by the external microprocessor. Alarms are raised to indicate reception of unstable and mismatched Payload Type label bits.

9.19 Microprocessor Interface

The Microprocessor Interface (MPIF) Block serves as the physical interface between the microprocessor and the internal blocks. The MPIF Block provides functions such as data bus buffering and address decoding. The MPIF Block allows for device level configuration of each block of the S/UNI-PDH device.

9.20 Normal Mode Register Memory Map

Address	Register
00H	S/UNI-PDH Configuration
01H	S/UNI-PDH Interrupt Enable
02H	S/UNI-PDH Interrupt Status
03H	S/UNI-PDH Control
04H	S/UNI-PDH Identification and Master Reset
05H	S/UNI-PDH Data Link Control
06H	RBOC Configuration/Interrupt Enable
07H	RBOC Interrupt Status
08H	DS3 FRMR Configuration
09H	DS3 FRMR Interrupt Enable
0AH	DS3 FRMR Interrupt Status
0BH	DS3 FRMR Status
0CH	RFDL Configuration
0DH	RFDL Enable/Status
0EH	RFDL Status
0FH	RFDL Data
10H	PMON Change of PMON Performance Meters
11H	PMON Interrupt Enable/Status
12H-13H	Reserved
14H	PMON Line Code Violation Event Count LSB
15H	PMON Line Code Violation Event Count MSB
16H	PMON Framing Bit Error Event Count LSB
17H	PMON Framing Bit Error Event Count MSB
18H	PMON Summed Excessive Zero Detect Count LSB
19H	PMON Summed Excessive Zero Detect Count MSB
1AH	PMON Parity Error Event Count LSB
1BH	PMON Parity Error Event Count MSB
1CH	PMON Path Parity Error Event Count LSB
1DH	PMON Path Parity Error Event Count MSB
1EH	PMON FEBE Event Count LSB
1FH	PMON FEBE Event Count MSB
20H	DS3 TRAN Configuration
21H	DS3 TRAN Diagnostics
22H-23H	Reserved
24H	XFDL Configuration
25H	XFDL Interrupt Status
26H	XFDL Transmit Data

27H	XBOC Code
28H	SPLR Configuration
29H	SPLR Interrupt Enable
2AH	SPLR Interrupt Status
2BH	SPLR Status
2CH	SPLT Configuration
2DH	SPLT Control
2EH	SPLT Diagnostics and G1 Octet
2FH	SPLT F1 Octet
30H	CPPM Loss of Clock Meters
31H	CPPM Change of CPPM Performance Meter
32H	CPPM B1 Error Count LSB
33H	CPPM B1 Error Count MSB
34H	CPPM Framing Error Event Count LSB
35H	CPPM Framing Error Event Count MSB
36H	CPPM FEBE Count LSB
37H	CPPM FEBE Count MSB
38H	CPPM HCS Error Count LSB
39H	CPPM HCS Error Count MSB
3AH	CPPM Idle/Unassigned Cell Count LSB
3BH	CPPM Idle/Unassigned Cell Count MSB
3CH	CPPM Receive Cell Count LSB
3DH	CPPM Receive Cell Count MSB
3EH	CPPM Transmit Cell Count LSB
3FH	CPPM Transmit Cell Count MSB
40H	RXCP Control
41H	RXCP Framing Control
42H	RXCP Interrupt Enable/Status
43H	RXCP Idle/Unassigned Cell Pattern: H1 octet
44H	RXCP Idle/Unassigned Cell Pattern: H2 octet
45H	RXCP Idle/Unassigned Cell Pattern: H3 octet
46H	RXCP Idle/Unassigned Cell Pattern: H4 octet
47H	RXCP Idle/Unassigned Cell Mask: H1 octet
48H	RXCP Idle/Unassigned Cell Mask: H2 octet
49H	RXCP Idle/Unassigned Cell Mask: H3 octet
4AH	RXCP Idle/Unassigned Cell Mask: H4 octet
4BH	RXCP User-Programmable Cell Pattern: H1 octet
4CH	RXCP User-Programmable Cell Pattern: H2 octet
4DH	RXCP User-Programmable Cell Pattern: H3 octet
4EH	RXCP User-Programmable Cell Pattern: H4 octet
4FH	RXCP User-Programmable Cell Mask: H1 octet

50H	RXCP User-Programmable Cell Mask: H2 octet
51H	RXCP User-Programmable Cell Mask: H3 octet
52H	RXCP User-Programmable Cell Mask: H4 octet
53H	RXCP HCS Control/Status
54H	RXCP LCD Count Threshold
55H-57H	Reserved
58H	TXCP Control
59H	TXCP Interrupt Enable/Status
5AH	TXCP Idle/Unassigned Cell Pattern: H1 octet
5BH	TXCP Idle/Unassigned Cell Pattern: H2 octet
5CH	TXCP Idle/Unassigned Cell Pattern: H3 octet
5DH	TXCP Idle/Unassigned Cell Pattern: H4 octet
5EH	TXCP Idle/Unassigned Cell Pattern: H5 octet
5FH	TXCP Idle/Unassigned Cell Payload
60H	E3 FRMR Framing Options
61H	E3 FRMR Maintenance Options
62H	E3 FRMR Framing Interrupt Enable
63H	E3 FRMR Framing Interrupt Indication and Status
64H	E3 FRMR Maintenance Event Interrupt Enable
65H	E3 FRMR Maintenance Event Interrupt Indication
66H	E3 FRMR Maintenance Event Status
67H	Reserved
68H	E3 TRAN Framing Options
69H	E3 TRAN Status and Diagnostic Options
6AH	E3 TRAN BIP-8 Error Mask
6BH	E3 TRAN Maintenance and Adaptation Options
6CH	TTB Control Register
6DH	TTB Trail Trace Identifier Status
6EH	TTB Indirect Address Register
6FH	TTB Indirect Data Register
70H	TTB Expected Payload Type Label Register
71H	TTB Payload Type Label Control/Status
72H	Reserved
73H	Reserved
74H	Sync FIFO Parity Control/Status
75H-7FH	Reserved
80H-FFH	*Reserved For Test Mode Registers*

For all register accesses, CSB must be low.

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-PDH. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[7]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-PDH to determine the programming state of the block.

3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-PDH operation unless otherwise noted.

Register 00H: S/UNI-PDH Configuration

Bit	Type	Function	Default
Bit 7	R/W	LLB	0
Bit 6	R/W	E3ENBL	0
Bit 5	R/W	FIFOBP	0
Bit 4	R/W	LOOPT	0
Bit 3	R/W	FRMRBP	0
Bit 2	R/W	DLB	0
Bit 1	R/W	PLB	0
Bit 0	R/W	CLB	0

CLB:
The CLB bit controls the cell loopback. When a logic 0 is written to CLB, cell loopback is disabled. When a logic 1 is written to CLB, cell loopback is enabled. While cell loopback is enabled, cells received by the S/UNI-PDH are written into the transmit FIFO. These cells also continue to be written to the receive FIFO. This bit must be used in conjunction with the LOOPT bit, otherwise transmit FIFO overflow may occur.

PLB:
The PLB bit controls the DS3 (or E3, if E3ENBL is logic 1) payload loopback. When a logic 0 is written to PLB, DS3 (or E3, if enabled) payload loopback is disabled. When a logic 1 is written to PLB, the DS3 (or E3, if enabled) overhead bits are regenerated and inserted into the received DS3 (or E3) stream and the resulting stream is transmitted. Setting the PLB bit disables the effect of the TICLK bit in the S/UNI-PDH Control register, thereby forcing flow-through timing.

DLB:
The DLB bit controls the diagnostic loopback. When a logic 0 is written to DLB, diagnostic loopback is disabled. When a logic 1 is written to DLB, the transmit data stream is looped in the receive direction. Depending on the S/UNI-PDH configuration, the loopback includes the DS3 or E3 framer (FRMR), the PLCP framer (SPLR), or the ATM Cell Delineator (ATMF). The DLB should not be set to a logic 1 when either the CLB, PLB or LLB bit is a logic 1. The DLB mode is not available when the S/UNI-PDH is used for E1 ATM direct-mapped applications.

FRMRBP:
The FRMRBP bit controls the bypassing of the internal DS3 or E3 framer. When a logic 0 is written to FRMRBP, the DS3 or E3 framer is activated, as selected by the E3ENBL bit. The S/UNI-PDH then receives and transmits an appropriately

formatted stream. When a logic 1 is written to FRMRBP, the DS3 or E3 transceiver is held reset, and the S/UNI-PDH receives and transmits a non-DS3/E3 formatted stream (for example a DS1 or E1 stream). When using diagnostic loopback in framer bypass mode, received cell errors may result if the E3 framer is enabled. Ensure that when FRMRBP is asserted that E3ENBL (in this register) is not asserted.

LOOPT:
The LOOPT bit selects the transmit timing source. When a logic 1 is written to LOOPT, the transmitter is loop-timed to the receiver. When loop timing is enabled, the receive clock (RCLK) is used as the transmit timing source. The transmit nibble stuffing is derived from the nibble stuffing in the receive PLCP frame (for DS3 or E3 PLCP frame transmission). The FIXSTUFF bit must be set to logic 0 if the LOOPT bit is set to logic 1. When a logic 0 is written to LOOPT, the transmit clock (TICLK) is used as the transmit timing source. The nibble stuffing is derived from the C13/CADD input, or is fixed internally (as determined by the FIXSTUFF bit in the SPLT Configuration Register (for DS3 or E3 PLCP frame transmission only). Setting the LOOPT bit disables the effect of the TICLK bit in the S/UNI-PDH Control register, thereby forcing flow-through timing. The LOOPT mode is not available when the S/UNI-PDH is used for E1 ATM direct-mapped applications. When the S/UNI-PDH is operating in DS-3 mode (E3ENBL =0) AND loop timing is enabled (LOOPT =1) then the FORMAT[0:1] bits in register 68H must both be programmed as logic 0. Otherwise cell corruption will occur.

FIFOBP:
The FIFOBP bit controls the bypassing of the receive and transmit FIFOs. When a logic 1 is written to FIFOBP, the receive and transmit FIFOs are bypassed, thereby minimizing the latency through the S/UNI-PDH. Note that the FIFOs may be bypassed only when PLCP formatted transmission frames (DS3, DS1, G.751 E3, or E1) are processed. When a logic 0 is written to FIFOBP, the receive and transmit FIFOs operate normally, and both PLCP based and non-PLCP based transmission frames may be processed

E3ENBL:
The E3ENBL bit controls which of the two transceivers is used for the transmission system sublayer. When a logic 1 is written to E3ENBL, the T3-FRMR and T3-TRAN are held reset and the E3-FRMR and E3-TRAN are enabled to source and sink G.751 or G.832 formatted E3 streams. When a logic 0 is written to E3ENBL, the E3-FRMR and E3-TRAN are held reset and the T3-FRMR and T3-TRAN are enable to source and sink DS3 formatted streams.

LLB:
The LLB bit controls the line loopback. When a logic 0 is written to LLB, line loopback is disabled. When a logic 1 is written to LLB, the stream received on RPOS/RDAT and RNEG/ROHM is looped to the TPOS/TDAT and TNEG/TOHM outputs. Note that the TPOS and TNEG outputs are timed to RCLK when LLB is logic 1. The LLB mode is not available when the S/UNI-PDH is used for E1 ATM direct-mapped applications.

Register 01H: S/UNI-PDH Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	SPLRE	0
Bit 6	R/W	TXCPE	0
Bit 5	R/W	RXCPE	0
Bit 4	R/W	RBOCE	0
Bit 3	R/W	FRMRE	0
Bit 2	R/W	PMONE	0
Bit 1	R/W	XFDLE	0
Bit 0	R/W	RFDLE	0

SPLRE, TXCPE, RXCPE, RBOCE, FRMRE, PMONE, XFDLE, RFDLE:
These bits are block interrupt enables. When a logic 0 is written to any of these bits, interrupts from the associated block are disabled, and are not reported on INTB. When a logic 1 is written to any of these bits, interrupts from the associated block are enabled, and may be reported on INTB. Note that interrupt enable registers are also contained in each block. The block level interrupt enable register, along with the bit corresponding to that block in this register must be written to enable interrupt generation.

Register 02H: S/UNI-PDH Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPLRI	X
Bit 6	R	TXCPI	X
Bit 5	R	RXCPI	X
Bit 4	R	RBOCI	X
Bit 3	R	FRMRI	X
Bit 2	R	PMONI	X
Bit 1	R	XFDLI	X
Bit 0	R	RFDLI	X

SPLRI, TXCPI, RXCPI, RBOCI, FRMRI, PMONI, XFDLI, RFDLI:
These bits are interrupt status indicators. These bits identify the block that is the source of a pending interrupt. This register is typically used by interrupt service routines to determine the source of a S/UNI-PDH interrupt.

Register 03H: S/UNI-PDH Control

Bit	Type	Function	Default
Bit 7	R/W	TICLK	0
Bit 6	R/W	8KREF	0
Bit 5	R/W	DLINV	0
Bit 4	R/W	RCLKINV	0
Bit 3	R/W	RPNINV	0
Bit 2	R/W	TUNI	0
Bit 1	R/W	TCLKINV	0
Bit 0	R/W	TPNINV	0

TPNINV:
The TPNINV bit provides polarity control for outputs TPOS/TDAT and TNEG/TOHM. When a logic 0 is written to TPNINV, the outputs are not inverted. When a logic 1 is written to TPNINV, the outputs are inverted. The TPNINV bit setting does not affect the loopback data in diagnostic loopback.

TCLKINV:
The TCLKINV bit provides polarity control for output TCLK. When a logic 0 is written to TCLKINV, TCLK is not inverted and outputs TPOS/TDAT and TNEG/TOHM are updated on the falling edge of TCLK. When a logic 1 is written to TCLKINV, TCLK is inverted and outputs TPOS/TDAT and TNEG/TOHM are updated on the rising edge of TCLK.

TUNI:
The TUNI bit enables the S/UNI-PDH to transmit unipolar or bipolar DS3 or E3 data streams. When a logic 1 is written to TUNI, the S/UNI-PDH transmits unipolar DS3 or E3 data on TPOS/TDAT. When TUNI is logic 1, the TNEG/TOHP output indicates the start of the DS3 M-Frame (the X1 bit) or the start of the E3 frame (bit 1 of the frame). When a logic 0 is written to TUNI, the S/UNI-PDH transmits B3ZS-encoded DS3 data or HDB3-encoded E3 data on TPOS/TDAT and TNEG/TOHM.

RPNINV:
The RPNINV bit provides polarity control for inputs RPOS/RDAT and RNEG/ROHM. When a logic 0 is written to RPNINV, the inputs are not inverted. When a logic 1 is written to RPNINV, the inputs are inverted. The RPNINV bit setting does not affect the loopback data in diagnostic loopback.

RCLKINV:
The RCLKINV bit provides polarity control for input RCLK. When a logic 0 is written to RCLKINV, RCLK is not inverted and inputs RPOS/RDAT and RNEG/ROHM are sampled on the rising edge of RCLK. When a logic 1 is written to RCLKINV, RCLK is inverted and inputs RPOS/RDAT and RNEG/ROHM are sampled on the falling edge of RCLK.

DLINV:
The DLINV bit provides polarity control for the DS3 C-bit Parity path maintenance data link which is located in the 3 C-bits of M-subframe 5. When a logic 1 is written to DLINV, the path maintenance data link is inverted before being processed. The rationale behind this bit is as follows: currently ANSI standard T1.107 specifies that the C-bits (which carry the path maintenance data link) be set to all zeros while the AIS maintenance signal is transmitted. The data link is obviously inactive during AIS transmission, and ideally the HDLC idle sequence (all ones) should be transmitted. By inverting the data link, the all zeros C-bit pattern becomes an idle sequence and the data link is terminated gracefully. Although this inversion is currently not specified in ANSI T1.107a, this bit is provided to safe-guard the S/UNI-PDH in case the inversion is required in the future.

8KREF:
The 8KREF bit selects the use of an 8 kHz PLCP frame reference signal. When the 8KREF bit is logic 1, an internal phase-frequency detector compares the transmit PLCP frame rate with the externally applied 8 kHz reference on the C13/CADD/8KREF input and adjusts the PLCP frame rate by taking control over the internal C13/CADD signal passed into the SPLT. When the 8KREF bit is logic 0, the C13/CADD input to the SPLT behaves normally and provides direct control of the SPLT stuffing.

If the LOOPT register bit is a logic 1 and the 8KREF bit is a logic 1, the RPOHFP output is used as the 8 kHz PLCP frame reference.

TICLK:
The TICLK bit selects the transmit clock used to update the TPOS/TDAT and TNEG/TOHM outputs. When a logic 0 is written to TICLK, the buffered version of the input transmit clock, TCLK, is used to update TPOS/TDAT and TNEG/TOHM on the edge selected by the TCLKINV bit. When a logic 1 is written to TICLK, TPOS/TDAT and TNEG/TOHM are updated on the rising edge of TICLK, eliminating the flow-through TCLK signal. The TICLK bit has no effect if the LOOPT, LLB or PLB bit is a logic 1.

Register 04H: S/UNI-PDH Identification and Master Reset

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[2]	0
Bit 5	R	TYPE[1]	1
Bit 4	R	TYPE[0]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

RESET:
The RESET bit allows software to asynchronously reset the S/UNI-PDH. The software reset is equivalent to setting the RSTB input pin low. When a logic 1 is written to RESET, the S/UNI-PDH is reset. When a logic 0 is written to RESET, the reset is removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

TYPE[2:0]:
The TYPE[2:0] bits allow software to identify this device as the S/UNI-PDH member of the S/UNI family of products. In its 84-pin PLCC package option, the S/UNI-PDH is pin compatible with the PM7321 PLPP device. The TYPE[2:0] bits can also be used to distinguish between the two devices. Note that versions of the PLPP exist that do not provide ID bits in the Master Reset register. This register should be written with the value 5EH and immediately read to determine the TYPE and ID; the PLPP will not return 21H.

ID[3:0]:
The ID[3:0] bits allows software to identify the version level of the S/UNI-PDH. This is the second version and returns ’b0001 when read.

Register 05H: S/UNI-PDH Data Link and FERF Control

Bit	Type	Function	Default
Bit 7	R/W	LCDEN	0
Bit 6	R/W	AISEN	0
Bit 5	R/W	REDEN	0
Bit 4	R/W	OOFEN	0
Bit 3	R/W	LOSEN	0
Bit 2	R/W	TNETOP	0
Bit 1	R/W	HCSCNTSEL	0
Bit 0	R/W	RNETOP	0

RNETOP:
The RNETOP bit enables the Network Operator Byte (NR) extracted from the G.832 E3 stream to be terminated by the internal HDLC receiver, RFDL. When RNETOP is logic 1, the NR byte is extracted from the G.832 stream and terminated by RFDL; the GC byte of the G.832 E3 stream is extracted and output on the RDLSIG pin for further processing externally. When RNETOP is logic 0, the GC byte is extracted from the G.832 stream and terminated by RFDL; the NR byte of the G.832 E3 stream is extracted and output on the RDLSIG pin for further processing externally.

For a G.751 E3 stream, National Use bit is presented on the RDLSIG pin if RNETOP is a logic 1. If RNETOP is a logic 0, the National Use bit is terminated internally by RFDL.

HCSCNTSEL:
The HCSCNTSEL bit determines the type of error accumulated by the CPPM HCS Error Count registers. If HCSCNTSEL is a logic 1, all correctable single bit header errors while the receive cell processor is in correction mode are accumulated. If HCSCNTSEL is a logic 0, uncorrectable header errors are accumulated. These include single bit errors while the receive cell processor is in detection mode.

TNETOP:
The TNETOP bit enables the Network Operator Byte (NR) inserted in the G.832 E3 stream to be sourced by the internal HDLC transmitter, XFDL. When TNETOP is logic 1, the NR byte is inserted into the G.832 stream through the XFDL block; the GC byte of the G.832 E3 stream is sourced by the TDLSIG pin. When TNETOP is logic 0, the GC byte is inserted into the G.832 stream through

the XFDL block; the NR byte of the G.832 E3 stream is sourced by the TDLSIG pin.

For G.751 streams, the National Use bit is sourced by the TDLSIG pin if TNETOP is logic 1. If TNETOP is logic 0, the National Use bit is sourced through the XFDL block.

If the S/UNI-PDH is configured for DS3 C-bit Parity operation, TNETOP determines the source of the Path Maintenance Datalink. When TNETOP is logic 1, the datalink inserted into the DS3 stream is sourced by the TDLSIG pin. When TNETOP is logic 0, the datalink is inserted into the DS3 stream through XFDL.

LOSEN:
The LOSEN bit enables the receive loss of signal indication to automatically generate a FERF indication in the transmit stream. This bit operates regardless of framer selected (DS3 or E3). When LOSEN is logic 1, assertion of the LOS indication by the framer causes a FERF (RAI in G.751 mode) to be transmitted by TRAN for the duration of the LOS assertion. When LOSEN is logic 0, assertion of the LOS indication does not cause transmission of a FERF.

OOFEN:
The OOFEN bit enables the receive out of frame indication to automatically generate a FERF indication (RAI in G.751 mode) in the transmit stream. This bit operates when the E3 framer is selected or when the DS3 framer is selected and the REDEN bit is logic 0. When OOFEN is logic 1, assertion of the OOF indication by the framer causes a FERF to be transmitted by TRAN for the duration of the OOF assertion. When OOFEN is logic 0, assertion of the OOF indication does not cause transmission of a FERF.

REDEN:
The REDEN bit enables the receive RED alarm (persistent out of frame) indication to automatically generate a FERF indication in the transmit stream. This bit operates only when the DS3 framer is selected; when the E3 framer is selected, this bit has no effect. When REDEN is logic 1, assertion of the RED indication by the framer causes a FERF to be transmitted by TRAN for the duration of the RED assertion. The OOFEN bit is internally forced to logic 0 when REDEN is logic 1. When REDEN is logic 0, assertion of the RED indication does not cause transmission of a FERF.

AISEN:
The AISEN bit enables the receive alarm indication signal to automatically

generate a FERF indication (RAI in G.751 mode) in the transmit stream. This bit operates regardless of framer selected (DS3 or E3). When AISEN is logic 1, assertion of the AIS indication by the framer causes a FERF to be transmitted by TRAN for the duration of the AIS assertion. When AISEN is logic 0, assertion of the AIS indication does not cause transmission of a FERF.

LCDEN:
The LCDEN bit enables the receive out of cell delineation indication to automatically generate a FERF indication (RAI in G.751 mode) in the transmit stream. This bit operates regardless of framer selected (DS3 or E3) but only in ATM mode. When LCDEN is logic 1, assertion of the LCD indication by the receive FIFO causes a FERF to be transmitted by the transmitter for the duration of the LCD assertion. When LCDEN is logic 0, assertion of the LCD indication does not cause transmission of a FERF.

Register 06H: RBOC Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	FEACE	0

FEACE:
The FEACE bit enables the generation of an interrupt when a valid far end alarm and control (FEAC) code is detected. When a logic 1 is written to FEACE, the interrupt generation is enabled.

AVC:
The AVC bit position selects the validation criterion used in determining a valid FEAC code. When a logic 0 is written to AVC, a FEAC code is validated when 8 out of the last 10 received codes are identical. The FEAC code is removed when 2 out of the last 10 received code do not match the validated code.

When a logic 1 is written to AVC, a FEAC code is validated when 4 out of the last 5 received codes are identical. The FEAC code is removed when a single received FEACs does not match the validated code.

IDLE:
The IDLE bit enables the generation of an interrupt when a validated FEAC is removed. When a logic 1 is written to IDLE, the interrupt generation is enabled.

Register 07H: RBOC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	IDLI	X
Bit 6	R	FEACI	X
Bit 5	R	FEAC[5]	X
Bit 4	R	FEAC[4]	X
Bit 3	R	FEAC[3]	X
Bit 2	R	FEAC[2]	X
Bit 1	R	FEAC[1]	X
Bit 0	R	FEAC[0]	X

FEAC[5:0]:
The FEAC[5:0] bits contain the received far end alarm and control channel codes. The FEAC[5:0] bits are set to all ones ("111111") when no code has been validated.

FEACI:
The FEACI bit is set to logic 1 when a new FEAC code is validated. The FEAC code value is contained in the FEAC[5:0] bits. The FEACI bit position is set to logic 0 when this register is read.

IDLI:
The IDLI bit is set to logic 1 when a validated FEAC code is removed. The FEAC[5:0] bits are set to all ones when the code is removed. The IDLI bit position is set to logic 0 when this register is read.

Register 08H: DS3 FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	AISPAT	1
Bit 6	R/W	FDET	0
Bit 5	R/W	MBDIS	0
Bit 4	R/W	M3O8	0
Bit 3	R/W	UNI	0
Bit 2	R/W	REFR	0
Bit 1	R/W	AISC	0
Bit 0	R/W	CBE	0

CBE:
The CBE bit enables the DS3 C-bit parity application. When a logic 1 is written to CBE, C-bit parity mode is enabled. When a logic 0 is written to CBE, the DS3 M23 format is selected. While the C-bit parity application is enabled, C-bit parity error events, far end block errors are accumulated.

AISC:
The AISC bit controls the algorithm used to detect the alarm indication signal (AIS). When a logic 1 is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic 0 is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic 0 is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

REFR:
The REFR bit initiates a DS3 reframe. When a logic 1 is written to REFR, the S/UNI-PDH is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low to high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

UNI:
The UNI bit configures the S/UNI-PDH to accept either dual-rail or single-rail receive DS3 streams. When a logic 1 is written to UNI, the S/UNI-PDH accepts a single-rail DS3 stream on RPOS/RDAT. The S/UNI-PDH accumulates line code violations on the RNEG/ROHM input. When a logic 0 is written to UNI, the S/UNI-PDH accepts B3ZS-encoded dual-rail data on RPOS/RDAT and RNEG/ROHM.

M3O8:
The M3O8 bit controls the DS3 out of frame decision criteria. When a logic 1 is written to M3O8, DS3 out of frame is declared when 3 of 8 framing bits (F-bits) are in error. When a logic 0 is written to M3O8, the 3 of 16 framing bits in error criteria is used, as recommended in ANSI T1.107

MBDIS:
The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic 1, M-bit errors are disabled from causing an OOF; the loss of frame criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is set to logic 0, errors in either M-bits or F-bits are enabled to cause an OOF. When MBDIS is logic 0, an OOF can occur when one or more M-bit errors occur in 3 out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit is exceeded.

FDET:
The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic 1, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic 0, the detection time is 13.5 ms.

AISPAT:
The AISPAT bit controls the pattern used to detect the alarm indication signal (AIS). When a logic 1 is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010... is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic 0 is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

Register 09H: DS3 FRMR Interrupt Enable (ACE=0)

Bit	Type	Function	Default
Bit 7	R/W	COFAE	0
Bit 6	R/W	REDE	0
Bit 5	R/W	CBITE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	IDLE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	LOSE	0

LOSE:
The LOSE bit enables interrupt generation when a DS3 loss of signal defect is declared or removed. The interrupt is enabled when a logic 1 is written.

OOFE:
The OOFE bit enables interrupt generation when a DS3 out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

AISE:
The AISE bit enables interrupt generation when the DS3 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

IDLE:
The IDLE bit enables interrupt generation when the DS3 IDLE maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

FERFE:
The FERFE bit enables interrupt generation when a DS3 far end receive failure defect is declared or removed. The interrupt is enabled when a logic 1 is written.

CBITE:
The CBITE bit enables interrupt generation when the S/UNI-PDH detects a change of state in the DS3 application identification channel. The interrupt is enabled when a logic 1 is written.

REDE:
The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV

bit location of the DS3 FRMR Status register. When REDE is set to logic 1, the interrupt output, INTB, is set low when the state of the RED indication changes.

COFAE:
The COFAE bit enables interrupt generation when the S/UNI-PDH detects a DS3 change of frame alignment. The interrupt is enabled when a logic 1 is written.

Register 09H: DS3 FRMR Additional Configuration Register (ACE=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	AISONES	0
Bit 4	R/W	BPVO	0
Bit 3	R/W	EXZSO	0
Bit 2	R/W	EXZDET	0
Bit 1	R/W	SALGO	0
Bit 0	R/W	DALGO	0

DALGO:
The DALGO bit determines the criteria used to decode a valid B3ZS signature. When DALGO is set to logic 1, a valid B3ZS signature is declared and 3 zeros substituted whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen. When the DALGO bit is set to logic 0, a valid B3ZS signature is declared and the 3 zeros are substituted whenever a zero followed by a bipolar violation is observed.

SALGO:
The SALGO bit determines the criteria used to establish a valid B3ZS signature used to map BPVs to line code violation indications. Any BPV that is not part of a valid B3ZS signature is indicated as an LCV. When the SALGO bit is set to logic 1, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation is observed. When SALGO is set to logic 0, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen.

EXZDET:
The EXZDET bit determines the type of zero occurrences to be included in the LCV indication. When EXZDET is set to logic 1, the occurrence of an excessive zero generates a single pulse indication that is used to indicate an LCV. When EXZDET is set to logic 0, every occurrence of 3 consecutive zeros generates a pulse indication that is used to indicate an LCV. For example, if a sequence of 15 consecutive zeros were received, with EXZDET=1 only a single LCV would be indicated for this string of excessive zeros; with EXZDET=0, five LCVs would be indicated for this string (i.e. one LCV for every 3 consecutive zeros).

EXZSO:
The EXZSO bit enables only summed zero occurrences to be accumulated in the

PMON EXZS Count Registers. When EXZSO is set to logic 1, any excessive zeros occurrences over an 85 bit period increments the PMON EXZS counter by one. When EXZSO is set to logic 0, summed LCVs are accumulated in the PMON EXZS Count Registers. A summed LCV is defined as the occurrence of either BPVs not part of a valid B3ZS signature or 3 consecutive zeros (or excessive zeros if EXZDET=1) occurring over an 85 bit period; each summed LCV occurrence increment the PMON EXZS counter by one.

BPVO:
The BPVO bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPVO is set to logic 1, only BPVs not part of a valid B3ZS signature generate an LCV indication and increment the PMON LCV counter. When BPVO is set to logic 0, both BPVs not part of a valid B3ZS signature, and either 3 consecutive zeros or excessive zeros generate an LCV indication and increment the PMON LCV counter.

AISONES:
The AISONES bit controls the pattern used to detect the alarm indication signal (AIS) when both AISPAT and AISC bits in DS3 FRMR Configuration register (08H) are logic 0; if either AISPAT or AISC are logic 1, the AISONES bit is ignored. When a logic 0 is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111...) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored. When a logic 1 is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111...) signal is observed for a period of time before declaring AIS. In this case all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized below:

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010… pattern; overhead bits ignored.
0	1	X	Framed DS3 stream containing C-bits all logic 0; payload bits ignored.
1	1	X	Framed DS3 stream containing repeating 1010… pattern in the payload, C-bits all logic 0, and X-Bits =1. This can be detected by setting both AISPAT and AISC high and declaring AIS only when AISV=1 and FERFV=0 (Register 0BH)
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

Register 0AH: DS3 FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	X
Bit 6	R	REDI	X
Bit 5	R	CBITI	X
Bit 4	R	FERFI	X
Bit 3	R	IDLI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0	R	LOSI	X

LOSI:
The LOSI bit is set to logic 1 when a loss of signal defect is detected or removed. The LOSI bit position is set to logic 0 when this register is read.

OOFI:
The OOFI bit is set to logic 1 when an out of frame defect is detected or removed. The OOFI bit position is set to logic 0 when this register is read.

AISI:
The AISI bit is set to logic 1 when the DS3 AIS maintenance signal is detected or removed. The AISI bit position is set to logic 0 when this register is read.

IDLI:
The IDLI bit is set to logic 1 when the DS3 IDLE maintenance signal is detected or removed. The IDLI bit position is set to logic 0 when this register is read.

FERFI:
The FERFI bit is set to logic 1 when a FERF defect is detected or removed. The FERFI bit position is set to logic 0 when this register is read.

CBITI:
The CBITI bit is set to logic 1 when a change of state is detected in the DS3 application identification channel. The CBITI bit position is set to logic 0 when this register is read.

REDI:
The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3

FRMR Status register. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.

COFAI:
The COFAI bit is set to logic 1 when a change of frame alignment is detected. A COFA is generated when a new DS3 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic 0 when this register is read.

Register 0BH: DS3 FRMR Status

Bit	Type	Function	Default
Bit 7	R/W	ACE	0
Bit 6	R	REDV	X
Bit 5	R	CBITV	X
Bit 4	R	FERFV	X
Bit 3	R	IDLV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0	R	LOSV	X

LOSV:
The LOSV bit indicates the current loss of signal defect state. LOSV is a logic 1 when a sequence of 175 zeros is detected on the B3ZS encoded DS3 receive stream. LOSV is a logic 0 when a signal with a ones density greater than 33% for 175 ± 1 bit periods is detected.

OOFV:
The OOFV bit indicates the current DS3 out of frame defect state. When the S/UNI-PDH has lost frame alignment and is searching for the new alignment, OOFV is set to logic 1. When the S/UNI-PDH has found frame alignment, the OOFV bit is set to logic 0.

AISV:
The AISV bit indicates the alarm indication signal state. When the S/UNI-PDH detects the AIS maintenance signal, AISV is set to logic 1.

IDLV:
The IDLV bit indicates the IDLE signal state. When the S/UNI-PDH detects the IDLE maintenance signal, IDLV is set to logic 1.

FERFV:
The FERFV bit indicates the current far end receive failure defect state. When the S/UNI-PDH detects an M-frame with the X1 and X2 bits both set to zero, FERFV is set to logic 1. When the S/UNI-PDH detects an M-frame with the X1 and X2 bits both set to one, FERFV is set to logic 0.

CBITV:
The CBITV bit indicates the application identification channel (AIC) state. CBITV

is set to logic 1 (indicating the presence of the C-bit parity application) when the AIC bit is set high for 63 consecutive M-frames. CBITV is set to logic 0 (indicating the presence of the M23 or SYNTRAN applications) when AIC is set low for 2 or more M-frames in the last 15.

REDV:
The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic 1, the DS3 FRMR frame alignment acquisition circuitry has been out of frame for 2.23ms (or for 13.5ms when FDET is logic 0). When the REDV bit is logic 0, the frame alignment circuitry has found frame (i.e. OOFV=0) for 2.23ms (or 13.5ms if FDET=0).

ACE:
The ACE bit selects the Additional Configuration Register. This register is located at address 09H, and is only accessible when the ACE bit is set to logic 1. When ACE is set to logic 0, the Interrupt Enable register is accessible at address 09H.

Register 0CH: RFDL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN:
The EN bit controls the overall operation of the RFDL Block. When a logic 1 is written to EN, the RFDL is enabled to receive HDLC messages on the selected maintenance data link. When a logic 0 is written to EN, the RFDL is disabled. When the RDFL is disabled, the receive data link FIFO and interrupts are cleared. The programming of the RFDL Enable/Status Register is not affected. When the RFDL is enabled, it will immediately begin searching for HDLC flag sequences.

TR:
The TR bit terminates the reception of the current maintenance data link message. When a logic 1 is written to TR, the RFDL empties the receive data link FIFO, clears all HDLC related interrupts, and begins searching for a new HDLC flag sequence. The RFDL handles the TR input in the same manner as if the EN bit had been cleared and then set. The TR bit is self-clearing; after being set, it will be cleared to logic zero after one cycle of the RDLCLK (Receive Datalink Clock).

Register 0DH: RFDL Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTC1	0
Bit 1	R/W	INTC0	0
Bit 0	R	INT	X

INTC1, INTC0:
INTC1 and INTC0 control the generation of HDLC related interrupt as follows: The contents of the RFDL Enable/Status register should only be changed when the RFDL is disabled to prevent any erroneous interrupt generation.

INTC1	INTC0	Description
0	0	Disable interrupts (All HDLC sources)
0	1	Enable INTB when FIFO receives data
1	0	Enable INTB when FIFO has 2 bytes of data
1	1	Enable INTB when FIFO has 3 bytes of data

INT:
The INT bit indicates the status of the internal HDLC interrupt. Interrupts are generated depending on the FIFO fill status, end of message (EOM) detection, FIFO overrun, abort sequence detection, and first HDLC flag sequence detection. The interrupt is cleared by an RFDL Receive Data Register read that empties the FIFO, unless the cause of the interrupt was due to a FIFO overrun. A FIFO overrun interrupt is cleared on an RFDL Status Register read.

Register 0EH: RFDL Status

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	FLG	X
Bit 4	R	EOM	X
Bit 3	R	CRC	X
Bit 2	R	NVB2	X
Bit 1	R	NVB1	X
Bit 0	R	NVB0	X

NVB[2:0]:
The NVB[2:0] bit positions indicate the number of valid bits in the Receive Data Register. It is possible that not all of the bits in the Receive Data Register are valid when the last message data byte is read since the frame can be any number of bits in length and not necessarily an integral number of bytes. The Receive Data Register is filled from the MSB to the LSB bit position, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0]. An NVB[2:0] value of 000B indicates that only the MSB in the register is valid. NVB[2:0] is only valid when the EOM bit is a logic 1, the FLG bit is a logic 1, and the OVR bit is a logic 0.

CRC:
The CRC bit is set to a logic 1 if a CCITT-CRC error was detected in the last received message. The CRC bit is only valid when EOM is a logic 1 and FLG is a logic 1 and OVR is a logic 0.

EOM:
The EOM bit indicates the end of a path maintenance message. EOM is set to a logic 1 when:

1) The last byte in the message is being read from the RFDL Receive Data Register,

2) An abort sequence is detected and the byte, written to the FIFO due to the detection of the abort sequence, is being read from the RFDL Receive Data Register,

3) The first HDLC flag sequence has been detected and the byte, written into the FIFO when the RFDL changes from the idle state to the active state, is being

read from the RFDL Receive Data Register,

4) Immediately on detection of FIFO overrun.

The EOM bit is passed through the FIFO with the data so that the end of message status corresponds to the data just read from the RFDL Receive Data Register.

FLG:
The FLG bit is set to a logic 1 when the RFDL detects the presence of the LAPD flag sequence (01111110). FLG is set to a logic 0 when the LAPD abort sequence (01111111) is detected in the data or when the RFDL is disabled. The FLG bit is passed through the FIFO with the data so that the flag status corresponds to the data just read from the RFDL Receive Data Register.

OVR:
The OVR bit is set to a logic 1 when a FIFO overflow is detected. OVR is set to a logic 0 when the RFDL status register is read. While OVR is high, the RFDL and FIFO are held in the reset state, causing the FLG and EOM bits to be reset.

FE:
The FE bit is set to a logic 1 when the last FIFO byte is read. FE is set to a logic 0 when the FIFO is loaded with new data. If the RFDL Receive Data Register is read while the FIFO is empty, then a FIFO underrun condition occurs. The underrun condition is reflected in the RFDL Status Register by forcing all bits to logic 0 for the first read immediately following the RFDL Receive Data Register read which caused the underrun condition.

Register 0FH: RFDL Receive Data

Bit	Type	Function	Default
Bit 7	R	RD7	X
Bit 6	R	RD6	X
Bit 5	R	RD5	X
Bit 4	R	RD4	X
Bit 3	R	RD3	X
Bit 2	R	RD2	X
Bit 1	R	RD1	X
Bit 0	R	RD0	X

RD[7:0]:
The RD[7:0] bits contain the path maintenance data link message. RD0 corresponds to the first bit of the serial byte received on the C-bit parity Path Maintenance Data Link channel. This register is actually a 4 level FIFO. If the FIFO is not empty, the FE bit in the RFDL Status Register is a logic 0.

A read of the this register increments the FIFO read pointer. If the register read causes a FIFO underrun, then the pointer is inhibited from incrementing. The underrun condition will be signalled in the next RFDL Status Register read by returning all zeros. When a FIFO overrun is detected, an interrupt is generated and the FIFO is reset until the RFDL Status Register is read.

Register 10H: S/UNI-PDH Change of PMON Performance Meters

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	LCVCH	X
Bit 4	R	FERRCH	X
Bit 3	R	EXZS_IECCH	X
Bit 2	R	PERRCH	X
Bit 1	R	CPERRCH	X
Bit 0	R	FEBECH	X

FEBECH:
The FEBECH bit is set to logic 1 if one or more FEBE events have occurred during the latest PMON accumulation interval.

CPERRCH:
The CPERRCH bit is set to logic 1 if one or more path parity error events have occurred during the latest PMON accumulation interval.

PERRCH:
The PERRCH bit is set to logic 1 if one or more parity error events have occurred during the latest PMON accumulation interval.

EXZS_IECCH:
The EXZS_IECCH bit is set to logic 1 if one or more summed line code violation events in DS3 mode or one or more IEC events in G.832 mode have occurred during the latest PMON accumulation interval.

FERRCH:
The FERRCH bit is set to logic 1 if one or more F-bit or M-bit error events have occurred during the latest PMON accumulation interval.

LCVCH:
The LCVCH bit is set to logic 1 if one or more line code violation events have occurred during the latest PMON accumulation interval.

Register 11H: PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	X
Bit 0	R	OVR	X

OVR:
The OVR bit indicates the overrun status of the PMON holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

INTR:
The INTR bit indicates the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read.

INTE:
The INTE bit enables the generation of an interrupt when the PMON counter values are transferred to the holding registers. When a logic 1 is written to INTE, the interrupt generation is enabled.

Register 14H: PMON Line Code Violation Event Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 15H: PMON Line Code Violation Event Count MSB

Bit	Type	Function	Default
Bit 7	R	LCV[15]	X
Bit 6	R	LCV[14]	X
Bit 5	R	LCV[13]	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

LCV[15:0]:
LCV[15:0] represents the number of DS3 or E3 line code violation errors that have been detected since the last time the LCV counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON or CPPM register addresses. Such a write transfers the internally accumulated count to the LCV Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 16H: PMON Framing Bit Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

Register 17H: PMON Framing Bit Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FERR[9]	X
Bit 0	R	FERR[8]	X

FERR[9:0]:
FERR[9:0] represents the number of DS3 F-bit and M-bit errors, or E3 framing pattern errors, that have been detected since the last time the framing error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON or CPPM register addresses. Such a write transfers the internally accumulated count to the Framing Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 18H: PMON Summed Excessive Zero Detect and Incoming Error Count LSB

Bit	Type	Function	Default
Bit 7	R	EXZS/IEC[7]	X
Bit 6	R	EXZS/IEC[6]	X
Bit 5	R	EXZS/IEC[5]	X
Bit 4	R	EXZS/IEC[4]	X
Bit 3	R	EXZS/IEC[3]	X
Bit 2	R	EXZS/IEC[2]	X
Bit 1	R	EXZS/IEC[1]	X
Bit 0	R	EXZS/IEC[0]	X

Register 19H: PMON Summed Excessive Zero Detect and Incoming Error Count MSB

Bit	Type	Function	Default
Bit 7	R	EXZS/IEC[15]	X
Bit 6	R	EXZS/IEC[14]	X
Bit 5	R	EXZS/IEC[13]	X
Bit 4	R	EXZS/IEC[12]	X
Bit 3	R	EXZS/IEC[11]	X
Bit 2	R	EXZS/IEC[10]	X
Bit 1	R	EXZS/IEC[9]	X
Bit 0	R	EXZS/IEC[8]	X

EXZS/IEC[15:0]:
In T3 mode, EXZS[15:0] represents the number of summed Excessive Zeros (EXZS) that occurred during the previous accumulation interval. One or more excessive zeros occurrences within an 85 bit DS3 information block is counted as one summed excessive zero. Excessive zeros are accumulated by this register only when the EXZSO and EXZDET are logic 1 in the DS3 FRMR Additional Configuration Register. This register accumulates summed line code violations when the EXZSO is logic 0. The count of summed line code violations is defined as the number of DS3 information blocks (85 bits) that contain one or more line code violations since the last time the summed LCV counter was polled.

When the S/UNI-PDH is configured for E3 G.832 with Tandem Connection, these registers indicate the number of IEC errors encoded in the Network Operator byte that occurred during the previous accumulation interval. The IEC is encoded in binary. A binary value of 1111 for IEC is equivalent to 15 IECs, not 4 IECs. It is not envisioned that the Tandem Connection mode will be used in S/UNI-PDH applications. This counter is forced to zero when the S/UNI-PDH is configured for E3 G.751.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON or CPPM register addresses. Such a write transfers the internally accumulated count to the Summed Excessive Zeros Detect Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 1AH: PMON Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Register 1BH: PMON Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7	R	PERR[15]	X
Bit 6	R	PERR[14]	X
Bit 5	R	PERR[13]	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[15:0]:
PERR[15:0] represents the number of DS3 P-bit errors, or the number of E3 G.832 BIP-8 errors, that have been detected since the last time the parity error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON or CPPM register addresses. Such a write transfers the internally accumulated count to the Parity Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 1CH: PMON Path Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	CPERR[7]	X
Bit 6	R	CPERR[6]	X
Bit 5	R	CPERR[5]	X
Bit 4	R	CPERR[4]	X
Bit 3	R	CPERR[3]	X
Bit 2	R	CPERR[2]	X
Bit 1	R	CPERR[1]	X
Bit 0	R	CPERR[0]	X

Register 1DH: PMON Path Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	CPERR[13]	X
Bit 4	R	CPERR[12]	X
Bit 3	R	CPERR[11]	X
Bit 2	R	CPERR[10]	X
Bit 1	R	CPERR[9]	X
Bit 0	R	CPERR[8]	X

CPERR[13:0]:
CPERR[13:0] represents the number of DS3 path parity errors that have been detected since the last time the DS3 path parity error counter was polled. This counter is forced to zero when the S/UNI-PDH is configured for all E3 configurations.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON or CPPM register addresses. Such a write transfers the internally accumulated count to the Path Parity Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 1EH: PMON FEBE Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 1FH: PMON FEBE Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

FEBE[13:0]:
FEBE[13:0] represents the number of DS3 or E3 G.832 far end block errors that have been detected since the last time the FEBE error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON or CPPM register addresses. Such a write transfers the internally accumulated count to the FEBE Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost.

Register 20H: DS3 TRAN Configuration

Bit	Type	Function	Default
Bit 7	R/W	CBTRAN	0
Bit 6	R/W	AIS	0
Bit 5	R/W	IDL	0
Bit 4	R/W	FERF	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	CBIT	0

CBIT:
The CBIT bit enables the DS3 C-bit parity application. When CBIT is written with a logic 1, C-bit parity is enabled, and the S/UNI-PDH modifies the C-bits as required to include the path maintenance data link, the FEAC channel, the far end block error indication, and the path parity. When CBIT is written with a logic 0, the M23 application is selected, and each C-bit is set to logic 1 by the S/UNI-PDH except for the first C-bit of the frame, which is forced to toggle every frame. Note that the C-bits may be modified as required using the DS3 overhead access port (TOH) regardless of the setting of this bit.

FERF:
The FERF bit enables insertion of the far end receive failure maintenance signal in the DS3 stream. When FERF is written with a logic 1, the X1 and X2 overhead bit positions are set to logic 0. When FERF is written with a logic 0, the X1 and X2 overhead bit positions in the DS3 stream are set to logic 1.

IDL:
The IDL bit enables insertion of the idle maintenance signal in the DS3 stream. When IDL is written with a logic 1, the DS3 payload is overwritten with the repeating pattern 1100.... The DS3 overhead bit insertion (X, P, M F, and C) continues normally. When IDL is written with a logic 0, the idle signal is not inserted.

AIS:
The AIS bit enables insertion of the AIS maintenance signal in the DS3 stream. When AIS is written with a logic 1, the DS3 payload is overwritten with the repeating pattern 1010.... The DS3 overhead bit insertion (X, P, M and F) continues normally. The values inserted in the C-bits during AIS transmission are

controlled by the CBTRAN bit in this register. When AIS is written with a logic 0, the AIS signal is not inserted.

CBTRAN:
The CBTRAN bit controls the C-bit values during AIS transmission. When CBTRAN is written with a logic 0, the C-bits are overwritten with zeros during AIS transmission as specified in ANSI T1.107. When CBTRAN is written with a logic 1, C-bit insertion continues normally (as controlled by the CBIT bit in this register) during AIS transmission.

Reserved:
The reserved bit must be programmed to logic 0 for proper operation.

Register 21H: DS3 TRAN Diagnostic

Bit	Type	Function	Default
Bit 7	R/W	DLOS	0
Bit 6	R/W	DLCV	0
Bit 5		Unused	X
Bit 4	R/W	DFERR	0
Bit 3	R/W	DMERR	0
Bit 2	R/W	DCPERR	0
Bit 1	R/W	DPERR	0
Bit 0	R/W	DFEBE	0

DFEBE:
The DFEBE bit controls the insertion of far end block errors in the DS3 stream. When DFEBE is written with a logic 1, and the C-bit parity application is enabled, the three C-bits in M-subframe 4 are set to a logic 0. When DFEBE is written with a logic 0, FEBEs are indicated based on receive framing bit errors and path parity errors.

DPERR:
The DPERR bit controls the insertion of parity errors (P-bit errors) in the DS3 stream. When DPERR is written with a logic 1, the P-bits are inverted before insertion. When DPERR is written with a logic 0, the parity is calculated and inserted normally.

DCPERR:
The DCPERR bit controls the insertion of path parity errors in the DS3 stream. When DCPERR is written with a logic 1 and the C-bit parity application is enabled, the three C-bits in M-subframe 3 are inverted before insertion. When DCPERR is written with a logic 0, the path parity is calculated and inserted normally.

DMERR:
The DMERR bit controls the insertion of M-bit framing errors in the DS3 stream. When DMERR is written with a logic 1, the M-bits are inverted before insertion. When DMERR is written with a logic 0, the M-bits are inserted normally. Setting the DMERR bit is sufficient to cause a DS-3 framer to lose frame, but may not be sufficient to keep it out of frame due to the possibility of a mimic M-bit pattern formed with neighboring X- bits or P-bits (if they are logic 0).

DFERR:
The DFERR bit controls the insertion of F-bit framing errors in the DS3 stream. When DFERR is written with a logic 1, the F-bits are inverted before insertion. When DFERR is written with a logic 0, the F-bits are inserted normally.

DLCV:
The DLCV bit controls the insertion of a single line code violation in the DS3 stream. When DLCV is written with a logic 1, a line code violation is inserted by generating an incorrect polarity of violation in the next B3ZS signature. The data being transmitted must therefore contain periods of three consecutive zeros in order for the line code violation to be inserted. For example, line code violations may not be inserted when transmitting AIS, but may be inserted when transmitting the idle signal. DLCV is automatically cleared upon insertion of the line code violation.

DLOS:
The DLOS bit controls the insertion of loss of signal in the DS3 stream. When DLOS is written with a logic 1, the data on outputs TPOS/TDAT and TNEG/TOHM is forced to continuous zeros.

Register 24H: XFDL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	EOM	0
Bit 3	R/W	INTE	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	0
Bit 0	R/W	EN	0

EN:
The EN bit controls the overall operation of the XFDL Block. When a logic 1 is written to EN, the XFDL is enabled to transmit HDLC messages on the selected maintenance data link. When a logic 0 is written to EN, the XFDL is disabled. When the XDFL is disabled, the all ones sequence is inserted in the selected maintenance data link.

CRC:
The CRC enable bit controls the generation of the CCITT-CRC frame check sequence (FCS). When a logic 1 is written to CRC, the CCITT-CRC frame check sequence is appended to the end of each message. When a logic 0 is written to CRC, the FCS is not appended to the end of the message.

ABT:
The ABT bit controls the transmission of the HDLC abort code. Setting the ABT bit to a logic 1 causes the 11111110 code to be transmitted after the last byte from the XFDL Transmit Data Register is transmitted. Aborts are continuously sent until this bit is reset to a logic 0.

INTE:
The INTE bit enables the generation of an interrupt when the transmit path maintenance data link requires servicing. When a logic 1 is written to INTE, the interrupt generation is enabled.

EOM:
The EOM bit indicates that the byte of data in the XFDL Transmit Data Register is the last byte of the current data link message. If the CRC bit is set to a logic 1, then the 16-bit FCS word is appended to the last byte and a continuous stream

of HDLC flag sequences is transmitted. The EOM bit is automatically cleared before transmission of the next data link message begins.

Register 25H: XFDL Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	INT	X
Bit 0	R/W	UDR	0

UDR:
The UDR bit indicates when the XFDL has underrun the data in the XFDL Transmit Data Register. The UDR bit is set to a logic 1 if the parallel to serial conversion of the last byte in the data register has completed before the next byte has been written. Once an underrun has occurred, the XFDL transmits an abort sequence followed by a flag, and waits to transmit the next valid data byte. If the UDR bit is still set after the transmission of the flag the XFDL will continuously transmit the all-ones idle pattern. The UDR bit is cleared by writing a logic 0 to the UDR bit position in this register.

INT:
The INT bit indicates that the XFDL is ready to accept a new data byte for transmission. The INT bit is set to a logic 1 when the previous byte in the XFDL Transmit Data Register has been loaded into the parallel to serial converter and a new byte can be written into the register. The INT bit is set to a logic 0 while data is in the XFDL Transmit Data Register.

Register 26H: XFDL Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD7	X
Bit 6	R/W	TD6	X
Bit 5	R/W	TD5	X
Bit 4	R/W	TD4	X
Bit 3	R/W	TD3	X
Bit 2	R/W	TD2	X
Bit 1	R/W	TD1	X
Bit 0	R/W	TD0	X

TD[7:0]:
The TD[7:0] bits contain the path maintenance data link message. TD0 corresponds to the first bit of the serial byte transmitted on the path maintenance data link channel. The XFDL signals when the next data byte is required by setting the INT bit in the XFDL Interrupt Status Register to a logic 1. When INT is set to a logic 1, the XFDL Transmit Data Register must be written with the next message byte within 4 data bit periods to prevent the occurrence of an underrun. At a nominal 28.2 kbit/s data link rate this period corresponds to 142 µs.

Register 27H: XBOC Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	FEAC[5]	1
Bit 4	R/W	FEAC[4]	1
Bit 3	R/W	FEAC[3]	1
Bit 2	R/W	FEAC[2]	1
Bit 1	R/W	FEAC[1]	1
Bit 0	R/W	FEAC[0]	1

FEAC[5:0]:
FEAC[5:0] contain the six bit code that is transmitted on the far end alarm and control channel (FEAC). The transmitted code consists of a sixteen bit sequence that is repeated continuously. The sequence consists of 8 ones followed by a zero, followed by the six bit code sequence transmitted in order FEAC0, FEAC1, ..., FEAC5, followed by a zero. The all ones sequence is inserted in the FEAC channel when FEAC[5:0] is written with all ones.

Register 28H: SPLR Configuration

Bit	Type	Function	Default
Bit 7	R/W	FORM[1]	0
Bit 6	R/W	FORM[0]	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	REFRAME	0
Bit 2	R/W	PLCPEN	0
Bit 1		Unused	X
Bit 0	R/W	EXT	0

EXT:
The EXT bit disables the internal transmission system sublayer timeslot counter from identifying DS1, DS3, E1, or E3 overhead bits. The EXT bit allows transmission formats that are unsupported by the internal timeslot counter to be supported using the RNEG/ROHM input. When a logic 0 is written to EXT, input transmission system overhead (for DS1, DS3, E1, and G.751 E3 formats) is indicated using the internal timeslot counter. This counter is synchronized to the transmission system frame alignment using the RNEG/ROHM (for non DS3/E3 formats), or by the integral framer block (for the DS3 or G.751 E3 format).

When a logic 1 is written to EXT, indications on RNEG/ROHM identify each transmission system overhead bit. The EXT bit must be written to logic 1 for G.832 E3 format.

PLCPEN:
The PLCPEN bit enables PLCP framing. When a logic 1 is written to PLCPEN, PLCP framing is enabled. The PLCP format is specified by the FORM[1:0] bits in this register. When a logic 0 is written to PLCPEN, PLCP related functions in the SPLR block are disabled. PLCPEN must be programmed to logic 0 for G.832 E3 format. When switching from transmission of PLCP formatted cells to direct ATM, the S/UNI-PDH may transmit the bytes with the nibbles swapped. This situation can be avoided if direct mode is selected by doing a software reset (Bit 7 Register 04H) which forces the SUNI-PDH into the default direct ATM mode.

REFRAME:
The REFRAME bit is used to trigger reframing. When a logic 1 is written to REFRAME, the S/UNI-PDH is forced out of PLCP frame and a new search for frame alignment is initiated. Note that only a logic 0 to logic 1 transition of the

REFRAME bit triggers reframing; multiple write operations are required to ensure such a transition.

FORM[1:0]:
The FORM[1:0] bits select the PLCP frame format as shown below:

FORM[1]	FORM[0]	PLCP Framing Format
0	0	DS3
0	1	E3
1	0	DS1
1	1	E1

The FORM[1:0] bits also determine the alignment of the payload with the transport overhead. Selecting the DS-3 value of 00B (default) provides nibble alignment of the payload and overhead. If byte alignment is required, for example when using an external framer, the FORM[1:0] bits should be set to a value of 10B in both the SPLT and SPLR Configuration registers.

Reserved:
The reserved bit must be programmed to logic 0 for proper operation.

Register 29H: SPLR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	FEBEE	0
Bit 5	R/W	COLSSE	0
Bit 4	R/W	BIPEE	0
Bit 3	R/W	FEE	0
Bit 2	R/W	YELE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:
The OOFE bit enables interrupt generation when a PLCP out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

LOFE:
The LOFE bit enables interrupt generation when a PLCP loss of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

YELE:
The YELE bit enables interrupt generation when a PLCP yellow alarm defect is declared or removed. The interrupt is enabled when a logic 1 is written.

FEE:
The FEE bit enables interrupt generation when the S/UNI-PDH detects a PLCP framing octet error. The interrupt is enabled when a logic 1 is written.

BIPEE:
The BIPEE bit enables interrupt generation when the S/UNI-PDH detects a PLCP bit interleaved parity error. The interrupt is enabled when a logic 1 is written.

COLSSE:
The COLSSE bit enables interrupt generation when the S/UNI-PDH detects a change of PLCP link status. The interrupt is enabled when a logic 1 is written.

FEBEE:
The FEBEE bit enables interrupt generation when the S/UNI-PDH detects a PLCP far end block error. The interrupt is enabled when a logic 1 is written.

Register 2AH: SPLR Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FEBEI	X
Bit 5	R	COLSSI	X
Bit 4	R	BIPEI	X
Bit 3	R	FEI	X
Bit 2	R	YELI	X
Bit 1	R	LOFI	X
Bit 0	R	OOFI	X

OOFI:
The OOFI bit is set to logic 1 when a PLCP out of frame defect is detected or removed. The OOF defect state is contained in the SPLR Status Register. The OOFI bit position is set to logic 0 when this register is read.

LOFI:
The LOFI bit is set to logic 1 when a PLCP loss of frame defect is detected or removed. The LOF defect state is contained in the SPLR Status Register. The LOFI bit position is set to logic 0 when this register is read.

YELI:
The YELI bit is set to logic 1 when a PLCP yellow alarm defect is detected or removed. The yellow alarm defect state is contained in the SPLR Status Register. The YELI bit position is set to logic 0 when this register is read.

FEI:
The FEI bit is set to logic 1 when a PLCP framing octet error is detected. A framing octet error is generated when one or more errors are detected in the framing alignment octets (A1, and A2), or the path overhead identification octets. The FEI bit position is set to logic 0 when this register is read.

BIPEI:
The BIPEI bit is set to logic 1 when a PLCP bit interleaved parity (BIP) error is detected. BIP errors are detected using the B1 byte in the PLCP path overhead. The BIPEI bit position is set to logic 0 when this register is read.

COLSSI:
The COLSSI bit is set to logic 1 when a PLCP change of link status signal code

is detected. The link status signal code is contained in the path status octet (G1). Link status signal codes are required in systems implementing the IEEE-802.6 DQDB protocol. A change of link status event occurs when two consecutive and identical link status codes are received that differ from the current code. The COLSSI bit position is set to logic 0 when this register is read.

FEBEI:
The FEBEI bit is set to logic 1 when a PLCP far end block error (FEBE) is detected. FEBE errors are indicated in the PLCP path status octet (G1). The FEBEI bit position is set to logic 0 when this register is read.

Register 2BH: SPLR Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LSS[2]	X
Bit 5	R	LSS[1]	X
Bit 4	R	LSS[0]	X
Bit 3		Unused	X
Bit 2	R	YELV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:
The OOFV bit indicates the current PLCP out of frame defect state. When an error is detected in both the A1 and A2 octets or when an error is detected in two consecutive path overhead identifier octets, OOFV is set to logic 1. When the S/UNI-PDH has found two valid, consecutive sets of A1 and A2 octets with two valid and sequential path overhead identifier octets, the OOFV bit is set to logic 0.

LOFV:
The LOFV bit indicates the current PLCP loss of frame defect state. The loss of frame defect state is an integrated version of the out of frame defect state. The declaration/removal times for the loss of frame defect state depends on the selected PLCP format, and are summarized in the table below:

PLCP Format	Declaration (ms)	Removal (ms)
DS3	1	12
G.751 E3	1.12	10
DS1	25	250
E1	20	200

If the OOF defect state is transient, the LOF counter is decremented at a rate 1/12 (DS3 PLCP) or 1/10 (DS1 or E1 PLCP) or 1/9 (G.751 E3 PLCP) of the incrementing rate.

YELV:
The YELV bit indicates the current PLCP yellow alarm defect state. YELV is set

to a logic 1 when ten or more consecutive frames are received with the yellow bit (contained in the path status octet) set to a logic 1. YELV is set to a logic 0 when ten or more consecutive frames are received with the yellow bit (contained in the path status octet) set to a logic 0.

LSS[2:0]:
The LSS[2:0] bits contain the current link status signal code. Link status signal codes are required in systems implementing the IEEE-802.6 DQDB protocol. LSS[2:0] is updated when two consecutive and identical link status signal codes are received.

Register 2CH: SPLT Configuration

Bit	Type	Function	Default
Bit 7	R/W	FORM[1]	0
Bit 6	R/W	FORM[0]	0
Bit 5	R/W	M1TYPE	0
Bit 4	R/W	M2TYPE	0
Bit 3	R/W	FIXSTUFF	0
Bit 2	R/W	PLCPEN	0
Bit 1		Unused	X
Bit 0	R/W	EXT	0

EXT:
The EXT bit disables the internal transmission system sublayer timeslot counter from identifying DS1, DS3, E1 or G.751 E3 overhead bits. The EXT bit allows transmission formats that are unsupported by the internal timeslot counter to be supported using the TIOHM input. When a logic 0 is written to EXT, input transmission system overhead (for DS1, DS3, E1 and G.751 E3 formats) is indicated using the internal timeslot counter. This counter flywheels to create the appropriate transmission system alignment. This alignment is indicated on the TNEG/TOHM output. When a logic 1 is written to EXT, indications on TIOHM identify each transmission system overhead bit. These indications flow through the S/UNI-PDH and appear on the TNEG/TOHM output where they mark the transmission system overhead placeholder positions in the TPOS/TDAT stream. The EXT bit must be set to logic 1 for G.832 E3 format.

PLCPEN:
The PLCPEN bit enables PLCP frame insertion. When a logic 1 is written to PLCPEN, PLCP framing is inserted. The PLCP format is specified by the FORM[1:0] bits in this register. When a logic 0 is written to PLCPEN, PLCP related functions in the SPLT block are disabled. The PLCPEN bit must be set to logic 0 for G.832 E3 format. When switching from transmission of PLCP formatted cells to direct ATM, the S/UNI-PDH may transmit the bytes with the nibbles swapped. This situation can be avoided if direct mode is selected by doing a software reset (Bit 7 Register 04H) which forces the SUNI-PDH into the default direct ATM mode.

FIXSTUFF:
The FIXSTUFF bit controls the transmit PLCP frame octet/nibble stuffing used for DS3 and G.751 E3 PLCP frame formats. When a logic 0 is written to FIXSTUFF, stuffing is determined by the C13/CADD input. When a logic 1 is written to

FIXSTUFF and the DS3 PLCP frame format is enabled, a nibble is stuffed into the 13 nibble trailer twice every three stuff opportunities (i.e. 13, 14, 14 nibbles). This stuff ratio provides for a nominal PLCP frame rate of 125.0002366 µs (an error of 1.9 ppm). When the G.751 E3 PLCP frame format is enabled, 18, 19 or 20 octets are stuffed into the trailer depending on the alignment of the G.751 E3 frame, and the G.751 E3 PLCP frame. This yields a nominal PLCP frame rate of 125 µs. The FIXSTUFF bit must be set to logic 0 if the LOOPT bit in the SUNI-PDH Configuration register is set to logic 1. When using the 8 kHz reference input (i.e., the 8KREF bit is logic 1 in the S/UNI-PDH Control Register), the FIXSTUFF bit must be set to logic 0.

M2TYPE:
The M2TYPE bit selects the type of code transmitted in the M2 octet. These codes are required in systems implementing the IEEE-802.6 DQDB protocol. When a logic 0 is written to M2TYPE, the fixed pattern type 0 code is transmitted in the M2 octet. When a logic 1 is written to M2TYPE, the 1023 cyclic code pattern (starting with B6 hexadecimal and ending with 8D hexadecimal) is transmitted in the M2 octet. Please refer to TA-TSY-000772, Issue 3 and Supplement 1, for details on the codes.

M1TYPE:
The M1TYPE bit selects the type of code transmitted in the M1 octet. These codes are required in systems implementing the IEEE-802.6 DQDB protocol. When a logic 0 is written to M1TYPE, the fixed pattern type 0 code is transmitted in the M1 octet. When a logic 1 is written to M1TYPE, the 1023 cyclic code pattern (starting with B6 hexadecimal and ending with 8D hexadecimal) is transmitted in the M1 octet. Please refer to TA-TSY-000772, Issue 3 and Supplement 1, for details on the codes.

FORM[1:0]:
The FORM[1:0] bits select the PLCP frame format as shown below:

FORM[1]	FORM[0]	PLCP Framing Format
0	0	DS3
0	1	E3
1	0	DS1
1	1	E1

The FORM[1:0] bits also determine the alignment of the payload with the transport overhead even if an external framer is used (EXT bit is set to logic 1). Selecting the DS-3 value of 00B (default) provides nibble alignment of the

payload and overhead. If byte alignment is required, for example when using an external framer, the FORM[1:0] bits should be set to a value of 10B in both the SPLT and SPLR Configuration registers.

Register 2DH: SPLT Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SRCZN	0
Bit 5	R/W	SRCF1	0
Bit 4	R/W	SRCB1	0
Bit 3	R/W	SRCG1	0
Bit 2	R/W	SRCM1	0
Bit 1	R/W	SRCM2	0
Bit 0	R/W	SRCC1	0

SRCC1:
The SRCC1 bit value ORed with input TPOHINS selects the source for the C1 octet on a bit by bit basis. If the OR results in a logic 0, the C1 bit position is derived internally as specified by the FIXSTUFF bit in the SPLT Configuration Register. If the OR results in a logic 1, the C1 bit position is inserted with the value sampled on TPOH.

SRCM2:
The SRCM2 bit value ORed with input TPOHINS selects the source for the M2 octet on a bit by bit basis. If the OR results in a logic 0, the M2 bit position is derived internally as specified by the M2TYPE bit in the SPLT Configuration Register. If the OR results in a logic 1, the M2 bit position is inserted with the value sampled on TPOH.

SRCM1:
The SRCM1 bit value ORed with input TPOHINS selects the source for the M1 octet on a bit by bit basis. If the OR results in a logic 0, the M1 bit position is derived internally as specified by the M1TYPE bit in the SPLT Configuration Register. If the OR results in a logic 1, the M1 bit position is inserted with the value sampled on TPOH.

SRCG1:
The SRCG1 bit value ORed with input TPOHINS selects the source for the G1 octet on a bit by bit basis. If the OR results in a logic 0, the G1 bit position is derived internally as required. If the OR results in a logic 1, the G1 bit position is inserted with the value sampled on TPOH.

SRCB1:
The SRCB1 bit value ORed with input TPOHINS selects the source for the B1 octet on a bit by bit basis. If the OR results in a logic 0, the internally calculated bit interleaved parity value is inserted in the B1 bit position. If the OR results in a logic 1, the B1 bit position is inserted with the value sampled on TPOH.

SRCF1:
The SRCF1 bit value ORed with input TPOHINS selects the source for the F1 octet on a bit by bit basis. If the OR results in a logic 0, the F1 bit position is determined by the SPLT F1 Octet Register. If the OR results in a logic 1, the F1 bit position is inserted with the value sampled on TPOH.

SRCZN:
The SRCZN bit value ORed with input TPOHINS selects the source for the Zn octets (where n=1 to 4 for the DS1 or E1 PLCP frame formats, n=1 to 6 for the DS3 PLCP frame format, and n=1 to 3 for the G.751 E3 PLCP frame format) on a bit by bit basis. If the OR results in a logic 0, the Zn bit position is forced to a logic 0. If the OR results in a logic 1, the Zn bit position is inserted with the value sampled on TPOH.

Register 2EH: SPLT Diagnostics and G1 Octet

Bit	Type	Function	Default
Bit 7	R/W	DPFRM	0
Bit 6	R/W	DAFRM	0
Bit 5	R/W	DB1	0
Bit 4	R/W	DFEBE	0
Bit 3	R/W	YEL	0
Bit 2	R/W	LSS[2]	0
Bit 1	R/W	LSS[1]	0
Bit 0	R/W	LSS[0]	0

LSS[2:0]:
The LSS[2:0] bits control the value inserted in the link status signal code bit positions of the path status octet (G1). These bits should be written with logic 0 when implementing an ATM Forum UNI-compliant DS3 interface.

YEL:
The YEL bit controls the yellow signal bit position in the path status octet (G1). When a logic 1 is written to YEL, the PLCP yellow alarm signal is transmitted.

DFEBE:
The DFEBE bit controls the insertion of far end block errors in the PLCP frame. When DFEBE is written with a logic 1, a single FEBE is inserted each PLCP frame. When DFEBE is written with a logic 0, FEBEs are indicated based on receive PLCP bit interleaved parity errors.

DB1:
The DB1 bit controls the insertion of bit interleaved parity (BIP) errors in the PLCP frame. When DB1 is written with a logic 1, a single BIP error is inserted in each PLCP frame. When DB1 is written with a logic 0, the bit interleaved parity is calculated and inserted normally.

DAFRM:
The DAFRM bit controls the insertion of frame alignment pattern errors. When DAFRM is written with a logic 1, a single bit error is inserted in each A1 octet, and in each A2 octet. When DAFRM is written with a logic 0, the frame alignment pattern octets are inserted normally.

DPFRM:
The DPFRM bit controls the insertion of parity errors in the path overhead identification (POHID) octets. When DPFRM is written with a logic 1, a parity error is inserted in each POHID octet. When DPFRM is written with a logic 0, the POHID octets are inserted normally.

Register 2FH: SPLT F1 Octet

Bit	Type	Function	Default
Bit 7	R/W	F1[7]	0
Bit 6	R/W	F1[6]	0
Bit 5	R/W	F1[5]	0
Bit 4	R/W	F1[4]	0
Bit 3	R/W	F1[3]	0
Bit 2	R/W	F1[2]	0
Bit 1	R/W	F1[1]	0
Bit 0	R/W	F1[0]	0

F1[7:0]:
The F1[7:0] bits contain the value inserted in the path user channel octet (F1). F1[7] is the most significant bit, and is transmitted first. F1[0] is the least significant bit and is the last bit transmitted in the octet.

Register 30H: CPPM Loss of Clock Meters

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	LOTC	X
Bit 0	R	LORC	X

LORC:
The LORC bit is set to logic 1 if insufficient edges have occurred on RCLK since the last read of this register. A logic 1 in this bit position normally indicates a board level interconnect failure. The LORC bit position is set to logic 1 when this register is read. LORC is subsequently cleared after detecting 8 cycles of RCLK (if Diagnostic Loopback is not asserted) or 8 cycles of TICLK (if Diagnostic Loopback is asserted). Note that LORC will remain asserted when the S/UNI-PDH is in FIFO bypass mode.

LOTC:
The LOTC bit is set to logic 1 if no edges have occurred on TICLK (or RCLK if LOOPT is set to logic 1) since the last read of this register. A logic 1 in this bit position normally indicates a board level interconnect failure. The LOTC bit position is set to logic 1 when this register is read. LOTC is subsequently cleared after detecting 8 cycles of TICLK (or RCLK if LOOPT is set).

Register 31H: CPPM Change of CPPM Performance Meters

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	TCELLCH	X
Bit 5	R	RCELLCH	X
Bit 4	R	UICELLCH	X
Bit 3	R	HCSECH	X
Bit 2	R	FEBECH	X
Bit 1	R	FECH	X
Bit 0	R	BIPECH	X

BIPECH:
The BIPECH bit is set to logic 1 if one or more PLCP bit interleaved parity error events have occurred since the last CPPM accumulation interval.

FECH:
The FECH bit is set to logic 1 if one or more PLCP frame alignment pattern octet errors, or path overhead identification octet errors have occurred since the last CPPM accumulation interval.

FEBECH:
The FEBECH bit is set to logic 1 if one or more PLCP far end block error events have occurred since the last CPPM accumulation interval.

HCSECH:
The HCSECH bit is set to logic 1 if one or more header check sequence error events have occurred since the last CPPM accumulation interval.

UICELLCH:
The UICELLCH bit is set to logic 1 if one or more idle/unassigned cells have been dropped (filtered) since the last CPPM accumulation interval.

RCELLCH:
The RCELLCH bit is set to logic 1 if one or more cells has been written to the receive cell FIFO since the last CPPM accumulation interval.

TCELLCH:
The TCELLCH bit is set to logic 1 if one or more cells has been read from the transmit cell FIFO since the last CPPM accumulation interval.

Register 32H: CPPM B1 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	B1E[7]	X
Bit 6	R	B1E[6]	X
Bit 5	R	B1E[5]	X
Bit 4	R	B1E[4]	X
Bit 3	R	B1E[3]	X
Bit 2	R	B1E[2]	X
Bit 1	R	B1E[1]	X
Bit 0	R	B1E[0]	X

Register 33H: CPPM B1 Error Count MSB

Bit	Type	Function	Default
Bit 7	R	B1E[15]	X
Bit 6	R	B1E[14]	X
Bit 5	R	B1E[13]	X
Bit 4	R	B1E[12]	X
Bit 3	R	B1E[11]	X
Bit 2	R	B1E[10]	X
Bit 1	R	B1E[9]	X
Bit 0	R	B1E[8]	X

B1E[15:0]:
B1E[15:0] represents the number of PLCP bit interleaved parity (BIP) errors that have been detected since the last time the B1 error counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses. Such a write transfers the internally accumulated count to the B1 Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 50 RCLK periods (1.2 µs for the DS3 bit rate; 1.45µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. B1 errors are not accumulated when the S/UNI-PDH has declared a PLCP loss of frame defect state.

Register 34H: CPPM Framing Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FE[7]	X
Bit 6	R	FE[6]	X
Bit 5	R	FE[5]	X
Bit 4	R	FE[4]	X
Bit 3	R	FE[3]	X
Bit 2	R	FE[2]	X
Bit 1	R	FE[1]	X
Bit 0	R	FE[0]	X

Register 35H: CPPM Framing Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	FE[11]	X
Bit 2	R	FE[10]	X
Bit 1	R	FE[9]	X
Bit 0	R	FE[8]	X

FE[11:0]:
FE[11:0] represents the number of PLCP framing pattern octet errors and path overhead identification octet errors that have been detected since the last time the framing error event counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses. Such a write transfers the internally accumulated count to the Framing Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 50 RCLK periods (1.2 µs for the DS3 bit rate; 1.45µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. Framing error errors are not accumulated when the S/UNI-PDH has declared a PLCP loss of frame defect state.

Register 36H: CPPM FEBE Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 37H: CPPM FEBE Count MSB

Bit	Type	Function	Default
Bit 7	R	FEBE[15]	X
Bit 6	R	FEBE[14]	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

FEBE[15:0]:
FEBE[15:0] represents the number of PLCP far end block errors (FEBE) that have been detected since the last time the FEBE error counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses. Such a write transfers the internally accumulated count to the FEBE Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 50 RCLK periods (1.2 µs for the DS3 bit rate; 1.45µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. FEBE errors are not accumulated when the S/UNI-PDH has declared a PLCP loss of frame defect state.

Register 38H: CPPM HCS Error Count LSB

Bit	Type	Function	Default
Bit 7	R	HCSE[7]	X
Bit 6	R	HCSE[6]	X
Bit 5	R	HCSE[5]	X
Bit 4	R	HCSE[4]	X
Bit 3	R	HCSE[3]	X
Bit 2	R	HCSE[2]	X
Bit 1	R	HCSE[1]	X
Bit 0	R	HCSE[0]	X

Register 39H: CPPM HCS Error Count MSB

Bit	Type	Function	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R	HCSE[11]	
Bit 2	R	HCSE[10]	
Bit 1	R	HCSE[9]	
Bit 0	R	HCSE[8]	

HCSE[11:0]:
HCSE[11:0] represents the number of header check sequence (HCS) errors that have been detected since the last time the HCSE error counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses. Such a write transfers the internally accumulated count to the HCSE Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 50 RCLK periods (1.2 µs for the DS3 bit rate; 1.45µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. HCS errors are not accumulated when the S/UNI-PDH has declared a PLCP loss of frame defect state (when the PLCP layer is enabled), or when the S/UNI-PDH has declared an out of cell delineation defect state (when direct cell delineation is enabled for non-PLCP based transmission formats) .

The type of HCS error accumulated is determined by the HCSCNTSEL bit of S/UNI-PDH Data Link and FERF Control register. If HCSCNTSEL is a logic 1 and configured with HCS error correction disabled (HECEN=0 in register 53H), single bit errors are not counted when in HCS detection mode. If HCSCNTSEL is a logic 1 and configured with HCS error correction enabled (HECEN=1 in register 53H), single bit errors are counted in both correction mode and detection mode.

If HCSCNTSEL is a logic 0, uncorrectable header errors are accumulated. These include single bit errors while the receive cell processor is in detection mode. The S/UNI-PDH transitions from the SYNC to the HUNT state on receipt of 7 consecutive cells with incorrect HCS values, and will indicate "Out of Cell Delineation" (RXCP Control Register 40H). However, the S/UNI-PDH does not correctly count the number of uncorrectable HCS errors received when the transition from SYNC to HUNT occurs. The uncorrectable HCS error count value

will be one less that the correct value. Software should take this into account if a transition from SYNC to HUNT has occurred.

Register 3AH: CPPM Idle/Unassigned Cell Count LSB

Bit	Type	Function	Default
Bit 7	R	UICELL[7]	X
Bit 6	R	UICELL[6]	X
Bit 5	R	UICELL[5]	X
Bit 4	R	UICELL[4]	X
Bit 3	R	UICELL[3]	X
Bit 2	R	UICELL[2]	X
Bit 1	R	UICELL[1]	X
Bit 0	R	UICELL[0]	X

Register 3BH: CPPM Idle/Unassigned Cell Count MSB

Bit	Type	Function	Default
Bit 7	R	UICELL[15]	X
Bit 6	R	UICELL[14]	X
Bit 5	R	UICELL[13]	X
Bit 4	R	UICELL[12]	X
Bit 3	R	UICELL[11]	X
Bit 2	R	UICELL[10]	X
Bit 1	R	UICELL[9]	X
Bit 0	R	UICELL[8]	X

UICELL[15:0]:
UICELL[15:0] represents the number of idle/unassigned cells that have been dropped since the last time the idle/unassigned cell counter was polled. Note that this counter operates only when idle/unassigned cell filtering is enabled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses. Such a write transfers the internally accumulated count to the Idle/Unassigned Cell Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 50 RCLK periods (1.2 µs for the DS3 bit rate; 1.45µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost.

Register 3CH: CPPM Receive Cell Count LSB

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 3DH: CPPM Receive Cell Count MSB

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

RCELL[15:0]:
RCELL[15:0] represents the aggregate number of cells that have been written to the receive FIFO since the last time the receive cell counter was polled. Note that this count represents the number of error-free, assigned cells that have been received when idle/unassigned cell filtering and HCS error filtering are enabled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses. Such a write transfers the internally accumulated count to the Receive Cell Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 50 RCLK periods (1.2 µs for the DS3 bit rate; 1.45µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost. Cells are not passed through the S/UNI-PDH when a PLCP loss of frame defect state is declared (when the PLCP layer is enabled), or when an out of cell delineation defect state is declared (when direct cell delineation is enabled for non-PLCP based transmission formats) .

Register 3EH: CPPM Transmit Cell Count LSB

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 3FH: CPPM Transmit Cell Count MSB

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

TCELL[15:0]:
TCELL[15:0] represents the aggregate number of assigned cells that have been transmitted since the last time the transmit cell counter was polled. The counter (and all other counters in the CPPM) is polled by writing to any of the CPPM register addresses. Such a write transfers the internally accumulated count to the Transmit Cell Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer occurs within 50 RCLK periods (1.2 µs for the DS3 bit rate; 1.45µs for the E3 bit rate) of the write. The transfer and reset is carried out in a manner that coincident events are not lost.

Register 40H: RXCP Control

Bit	Type	Function	Default
Bit 7	R/W	HCSPASS	0
Bit 6	R/W	HCSDQDB	0
Bit 5	R/W	HCSADD	0
Bit 4	R/W	HCK	0
Bit 3	R/W	BLOCK	0
Bit 2	R/W	DSCR	0
Bit 1	R	OOCDV	X
Bit 0	R/W	FIFORST	0

FIFORST:
The FIFORST bit is used to reset the receive FIFO. When a logic 1 is written to FIFORST, the FIFO is immediately emptied, and incoming assigned cells are ignored. When a logic 0 is written to FIFORST, the receive FIFO operates normally.

OOCDV:
The OOCDV bit indicates the current out of cell delineation defect state. This bit is valid when the ATM Cell Delineator (ATMF) Block is enabled. The ATMF block is enabled (using the DELIN bit in the RXCP Framing Control Register) when delineating cells in a non-PLCP based transmission format. When an HCS error is detected in seven consecutive cells, OOCDV is set to logic 1. When six consecutive cells containing no HCS errors are detected, OOCDV is set to logic 0.

DSCR:
The DSCR bit controls cell payload descrambling using the self-synchronizing polynomial $x^{43} + 1$. Payload descrambling can be enabled for PLCP based and non-PLCP based transmission systems. When a logic 1 is written to DSCR, payload descrambling is enabled. When a logic 0 is written to DSCR, payload descrambling is disabled.

BLOCK:
The BLOCK bit enables idle/unassigned and user-programmable cell filtering. When a logic 1 is written to BLOCK, idle/unassigned cells or user-programmed cells corresponding to the pattern specified in the Idle/Unassigned Cell Pattern and User-programmable Cell Pattern Registers, and their associated Cell Mask Registers, are blocked. When a logic 0 is written to BLOCK, only idle/unassigned cells or user-programmed cells corresponding to the pattern specified in the

Idle/Unassigned Cell Pattern and User-programmable Cell Pattern Registers, and their associated Cell Mask Registers, are passed through the FIFO.

HCK:
The HCK bit controls a FIFO data path integrity check. The integrity check consists of inserting either an alternating AAH/55H pattern, or a fixed 55H pattern, in the HCS octet location as selected by the FIXPAT bit in the RXCP Framing Control register. The AA/55H pattern alternates with each cell written to the FIFO. An external device reading cells from the receive FIFO verifies that either the alternating or the fixed pattern is present in the cell stream. Any pattern discrepancy indicates a failure in the receive data path. When a logic 1 is written to HCK, the data path integrity check is enabled, and the HCS octet location is overwritten with the alternating pattern. When a logic 0 is written to HCK, the received HCS value is passed unaltered through the FIFO.

HCSADD:
The HCSADD bit enables the addition of the coset polynomial $x^6 + x^4 + x^2 + 1$ to the received HCS octet before comparison with the calculated result as required by the ATM Forum UNI specification. When a logic 1 is written to HCSADD, the coset polynomial is added to the HCS. When a logic 0 is written to HCSADD, the unmodified HCS value is compared with the calculated result.

HCSDQDB:
The HCSDQDB bit controls the cell header octets included in the HCS calculation. When a logic 1 is written to HCSDQDB, header octets two, three, and four are included in the HCS calculation as required by the IEEE-802.6 DQDB specification. When a logic 0 is written to HCSDQDB, all four header octets are included in the HCS calculation as required by the ATM Forum UNI specification, and the ITU-T Recommendation I.432.

HCSPASS:
The HCSPASS bit enables cells containing HCS errors to be passed through the receive FIFO. When a logic 1 is written to HCSPASS, cells containing detectable HCS errors are written to the receive FIFO. When a logic 0 is written to HCSPASS, cells containing detectable HCS errors are dropped. Note that all cells are dropped while a loss of frame defect is detected (for PLCP based transmission systems), or while an out of cell delineation defect is detected (for non-PLCP based transmission systems).

Register 41H: RXCP Framing Control

Bit	Type	Function	Default
Bit 7	R/W	REMPTY4	0
Bit 6	R/W	LCDE	0
Bit 5	R	LCDI	X
Bit 4	R	LCD	X
Bit 3	R/W	FIXPAT	0
Bit 2	R/W	DETHYST[1]	0
Bit 1	R/W	DETHYST[0]	0
Bit 0	R/W	DELIN	0

DELIN:
The DELIN bit enables the ATM Cell Delineator (ATMF) Block. HCS-based cell delineation is provided for non-PLCP based transmission systems (i.e. G.832 E3, or G.804-formatted DS3, DS1 and E1). When a logic 1 is written to DELIN, HCS-based cell delineation is enabled. When a logic 0 is written to DELIN, PLCP based transmission formats may be processed. PLCP based transmission format selection is controlled by the SPLR Configuration Register.

DETHYST[1:0]:
The DETHYST[1:0] bits control the cell acceptance threshold after an HCS error is detected. This feature is enabled when the HCSPASS bit in the RXCP Control Register is written with a logic 0. Upon detecting an HCS error, cells continue to be dropped until a number of consecutive cells are received that contain no HCS errors. The number of consecutive cells is indicated below:

DETHYST[1:0]	Cell Acceptance Threshold
00	The first cell containing an error-free HCS
01	The second consecutive cell containing no HCS errors.
10	The fourth consecutive cell containing no HCS errors.
11	The eighth consecutive cell containing no HCS errors.

FIXPAT:
The FIXPAT bit enables the insertion of a fixed 55H pattern into the HCS when the FIFO data path integrity check is enabled by the HCK bit in the RXCP Control register. When FIXPAT is logic 1, the pattern forced into the HCS byte exiting the FIFO is 55H. When FIXPAT is logic 0, the pattern force in the HCS byte is an alternating AAH/55H pattern which alternate every cell.

LCD:
The LCD bit indicates the state of the Loss of Cell Delineation indication. When LCD is logic 1, an out of cell delineation (OCD) defect has persisted for 4ms. When LCD is logic 0, no OCD has persisted for 4ms.

LCDI:
The LCDI bit is set to logic 1 when the state of loss of cell delineation (LCD) has changed. The LCDI bit position is set to logic 0 when this register is read.

LCDE:
The LCDE bit enables the generation of an interrupt when the LCD state changes. When a logic 1 is written to the LCDE bit position, the interrupt generation is enabled.

REMPTY4:
The REMPTY4 bit selects the amount of advance indication given on the receive cell available (RCA) signal. When REMPTY4 is logic 1, RCA is deasserted when the receive FIFO is almost empty and can accept no more than four byte read requests before underflowing. When REMPTY4 is logic 0, RCA is deasserted to logic 0 when the receive FIFO is empty and can accept no more read requests before underflowing (if a read request is made while RCA is low, an underflow indication is asserted but the read request is ignored).

Register 42H: RXCP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	OOCDE	0
Bit 6	R/W	HCSE	0
Bit 5	R/W	FIFOE	0
Bit 4	R	OOCDI	X
Bit 3	R	UHCSI	X
Bit 2	R	COCAI	X
Bit 1	R	FOVRI	X
Bit 0	R	FUDRI	X

FUDRI:
When the SYFIFOB input is a logic 1, the FUDRI bit is set to logic 1 when a read is attempted when the receive FIFO is empty. The FUDRI bit position is set to logic 0 when this register is read.

FOVRI:
The FOVRI bit is set to logic 1 when the receive FIFO has overrun. The FOVRI bit position is set to logic 0 when this register is read.

COCAI:
The COCAI bit is only valid if the PLCP framer is enabled (DELIN bit = 0, register 41H). The COCAI bit is set to logic 1 when a change of cell alignment (COCA) is detected. A COCA is generated when a new cell alignment is determined that differs from the last known cell alignment. The COCAI bit position is set to logic 0 when this register is read. Note that during the loss of frame state the last known cell alignment is retained, so this bit will only be set upon removal of the loss of frame if the new cell alignment differs from the old. The COCAI bit can also be set due to a receive FIFO overrun or underrun condition. A receive FIFO overrun is indicated by the FOVRI bit in register 42H, and underrun condition is indicated by the FUDRI bit in register 42H. Underrun or overrun of the receive FIFO results in a FIFO reset (including the FIFO write pointer). This can cause a change of cell alignment. The COCAI bit position is set to logic 0 when this register is read.

UHCSI:
The UHCSI bit is set to logic 1 when an uncorrectable header check sequence (HCS) error is detected. The UHCSI bit position is set to logic 0 when this register is read.

OOCDI:
The OOCDI bit is set to logic 1 when an out of cell delineation (OOCD) defect is detected or removed. The OOCD defect state is contained in the RXCP Control Register. The OOCDI bit position is set to logic 0 when this register is read.

FIFOE:
The FIFOE bit enables the generation of an interrupt when the S/UNI-PDH detects a receive FIFO overrun, a FIFO underrun, or a change of cell alignment (COCA). When a logic 1 is written to FIFOE, the interrupt generation is enabled.

HCSE:
The HCSE bit enables the generation of an interrupt when the S/UNI-PDH detects an HCS error. When a logic 1 is written to HCSE, the interrupt generation is enabled.

OOCDE:
The OOCDE bit enables the generation of an interrupt when an out of cell delineation defect is declared or removed. When a logic 1 is written to OOFE, the interrupt generation is enabled.

Register 43H: RXCP Idle/Unassigned Cell Pattern: H1 octet

Bit	Type	Function	Default
Bit 7	R/W	CP[7]	0
Bit 6	R/W	CP[6]	0
Bit 5	R/W	CP[5]	0
Bit 4	R/W	CP[4]	0
Bit 3	R/W	CP[3]	0
Bit 2	R/W	CP[2]	0
Bit 1	R/W	CP[1]	0
Bit 0	R/W	CP[0]	0

CP[7:0]:
The CP[7:0] bits contain the idle/unassigned cell header pattern to match in the first octet (H1) of the received cell in conjunction with the H1 octet mask. The BLOCK bit, in the RXCP Control Register, determines whether to block or pass cells matching this pattern. This register should be set to 00H when filtering the standard idle/unassigned cell pattern.

Register 44H: RXCP Idle/Unassigned Cell Pattern: H2 octet

Bit	Type	Function	Default
Bit 7	R/W	CP[7]	0
Bit 6	R/W	CP[6]	0
Bit 5	R/W	CP[5]	0
Bit 4	R/W	CP[4]	0
Bit 3	R/W	CP[3]	0
Bit 2	R/W	CP[2]	0
Bit 1	R/W	CP[1]	0
Bit 0	R/W	CP[0]	0

CP[7:0]:
The CP[7:0] bits contain the idle/unassigned cell header pattern to match in the second octet (H2) of the received cell in conjunction with the H2 octet mask. The BLOCK bit, in the RXCP Control Register, determines whether to block or pass cells matching this pattern. This register should be set to 00H when filtering the standard idle/unassigned cell pattern.

Register 45H: RXCP Idle/Unassigned Cell Pattern: H3 octet

Bit	Type	Function	Default
Bit 7	R/W	CP[7]	0
Bit 6	R/W	CP[6]	0
Bit 5	R/W	CP[5]	0
Bit 4	R/W	CP[4]	0
Bit 3	R/W	CP[3]	0
Bit 2	R/W	CP[2]	0
Bit 1	R/W	CP[1]	0
Bit 0	R/W	CP[0]	0

CP[7:0]:
The CP[7:0] bits contain the idle/unassigned cell header pattern to match in the third octet (H3) of the received cell in conjunction with the H3 octet mask. The BLOCK bit, in the RXCP Control Register, determines whether to block or pass cells matching this pattern. This register should be set to 00H when filtering the standard idle/unassigned cell pattern.

Register 46H: RXCP Idle/Unassigned Cell Pattern: H4 octet

Bit	Type	Function	Default
Bit 7	R/W	CP[7]	0
Bit 6	R/W	CP[6]	0
Bit 5	R/W	CP[5]	0
Bit 4	R/W	CP[4]	0
Bit 3	R/W	CP[3]	0
Bit 2	R/W	CP[2]	0
Bit 1	R/W	CP[1]	0
Bit 0	R/W	CP[0]	0

CP[7:0]:
The CP[7:0] bits contain the idle/unassigned cell header pattern to match in the fourth octet (H4) of the received cell in conjunction with the H4 octet mask. The BLOCK bit, in the RXCP Control Register, determines whether to block or pass cells matching this pattern. By default, unassigned cells are transmitted. This register should be set to 01H to filter idle cells.

Register 47H: RXCP Idle/Unassigned Cell Mask: H1 octet

Bit	Type	Function	Default
Bit 7	R/W	CPM[7]	0
Bit 6	R/W	CPM[6]	0
Bit 5	R/W	CPM[5]	0
Bit 4	R/W	CPM[4]	0
Bit 3	R/W	CPM[3]	0
Bit 2	R/W	CPM[2]	0
Bit 1	R/W	CPM[1]	0
Bit 0	R/W	CPM[0]	0

CPM[7:0]:
The CPM[7:0] bits contain the idle/unassigned cell header mask for the first octet (H1) of the received cell. This mask is applied to the H1 octet pattern. A logic 1 in any CPM[n] bit enables the corresponding bit in the H1 Idle/Unassigned Cell Pattern Register to be compared with the received H1 octet. A logic 0 causes the masking of the corresponding bit. This register should be set to FFH when filtering the standard unassigned cell pattern.

Register 48H: RXCP Idle/Unassigned Cell Mask: H2 octet

Bit	Type	Function	Default
Bit 7	R/W	CPM[7]	0
Bit 6	R/W	CPM[6]	0
Bit 5	R/W	CPM[5]	0
Bit 4	R/W	CPM[4]	0
Bit 3	R/W	CPM[3]	0
Bit 2	R/W	CPM[2]	0
Bit 1	R/W	CPM[1]	0
Bit 0	R/W	CPM[0]	0

CPM[7:0]:
The CPM[7:0] bits contain the idle/unassigned cell header mask for the second octet (H2) of the received cell. This mask is applied to the H2 octet pattern. A logic 1 in any CPM[n] bit enables the corresponding bit in the H2 Idle/Unassigned Cell Pattern Register to be compared with the received H2 octet. A logic 0 causes the masking of the corresponding bit. This register should be set to FFH when filtering the standard unassigned cell pattern.

Register 49H: RXCP Idle/Unassigned Cell Mask: H3 octet

Bit	Type	Function	Default
Bit 7	R/W	CPM[7]	0
Bit 6	R/W	CPM[6]	0
Bit 5	R/W	CPM[5]	0
Bit 4	R/W	CPM[4]	0
Bit 3	R/W	CPM[3]	0
Bit 2	R/W	CPM[2]	0
Bit 1	R/W	CPM[1]	0
Bit 0	R/W	CPM[0]	0

CPM[7:0]:
The CPM[7:0] bits contain the idle/unassigned cell header mask for the third octet (H3) of the received cell. This mask is applied to the H3 octet pattern. A logic 1 in any CPM[n] bit enables the corresponding bit in the H3 Idle/Unassigned Cell Pattern Register to be compared with the received H3 octet. A logic 0 causes the masking of the corresponding bit. This register should be set to FFH when filtering the standard unassigned cell pattern.

Register 4AH: RXCP Idle/Unassigned Cell Mask: H4 octet

Bit	Type	Function	Default
Bit 7	R/W	CPM[7]	0
Bit 6	R/W	CPM[6]	0
Bit 5	R/W	CPM[5]	0
Bit 4	R/W	CPM[4]	0
Bit 3	R/W	CPM[3]	0
Bit 2	R/W	CPM[2]	0
Bit 1	R/W	CPM[1]	0
Bit 0	R/W	CPM[0]	0

CPM[7:0]:
The CPM[7:0] bits contain the idle/unassigned cell header mask for the fourth octet (H4) of the received cell. This mask is applied to the H4 octet pattern. A logic 1 in any CPM[n] bit enables the corresponding bit in the H4 Idle/Unassigned Cell Pattern Register to be compared with the received H4 octet. A logic 0 causes the masking of the corresponding bit. This register should be set to FFH when filtering the standard unassigned cell pattern.

Register 4BH: RXCP User-Programmable Match Pattern: H1 octet

Bit	Type	Function	Default
Bit 7	R/W	UPH1[7]	0
Bit 6	R/W	UPH1[6]	0
Bit 5	R/W	UPH1[5]	0
Bit 4	R/W	UPH1[4]	0
Bit 3	R/W	UPH1[3]	0
Bit 2	R/W	UPH1[2]	0
Bit 1	R/W	UPH1[1]	0
Bit 0	R/W	UPH1[0]	0

UPH1[7:0]:
This register contains the pattern to match in the first octet (H1) of the received cell in conjunction with User-Programmable Match Mask for H1. The BLOCK bit, in the RXCP Configuration/ Control register, determines whether to pass or discard cells matching this pattern.

Register 4CH: RXCP User-Programmable Match Pattern: H2 octet

Bit	Type	Function	Default
Bit 7	R/W	UPH2[7]	0
Bit 6	R/W	UPH2[6]	0
Bit 5	R/W	UPH2[5]	0
Bit 4	R/W	UPH2[4]	0
Bit 3	R/W	UPH2[3]	0
Bit 2	R/W	UPH2[2]	0
Bit 1	R/W	UPH2[1]	0
Bit 0	R/W	UPH2[0]	0

UPH2[7:0]:
This register contains the pattern to match in the second octet (H2) of the received cell in conjunction with the User-Programmable Match Mask for H2. The BLOCK bit, in the RXCP Configuration/Control register, determines whether to pass or discard cells matching this pattern.

Register 4DH: RXCP User-Programmable Match Pattern: H3 octet

Bit	Type	Function	Default
Bit 7	R/W	UPH3[7]	0
Bit 6	R/W	UPH3[6]	0
Bit 5	R/W	UPH3[5]	0
Bit 4	R/W	UPH3[4]	0
Bit 3	R/W	UPH3[3]	0
Bit 2	R/W	UPH3[2]	0
Bit 1	R/W	UPH3[1]	0
Bit 0	R/W	UPH3[0]	0

UPH3[7:0]:
This register contains the pattern to match in the third octet (H3) of the received cell in conjunction with the User-Programmable Match Mask for H3. The BLOCK bit, in the RXCP Configuration/Control register, determines whether to pass or discard cells matching this pattern.

Register 4EH: RXCP User-Programmable Match Pattern: H4 octet

Bit	Type	Function	Default
Bit 7	R/W	UPH4[7]	0
Bit 6	R/W	UPH4[6]	0
Bit 5	R/W	UPH4[5]	0
Bit 4	R/W	UPH4[4]	0
Bit 3	R/W	UPH4[3]	0
Bit 2	R/W	UPH4[2]	0
Bit 1	R/W	UPH4[1]	0
Bit 0	R/W	UPH4[0]	0

UPH4[7:0]:
This register contains the pattern to match in the fourth octet (H4) of the received cell in conjunction with the User-Programmable Match Mask for H4. The BLOCK bit, in the RXCP Configuration/Control register, determines whether to pass or discard cells matching this pattern.

Register 4FH: RXCP User-Programmable Match Mask: H1 octet

Bit	Type	Function	Default
Bit 7	R/W	UPMH1[7]	0
Bit 6	R/W	UPMH1[6]	0
Bit 5	R/W	UPMH1[5]	0
Bit 4	R/W	UPMH1[4]	0
Bit 3	R/W	UPMH1[3]	0
Bit 2	R/W	UPMH1[2]	0
Bit 1	R/W	UPMH1[1]	0
Bit 0	R/W	UPMH1[0]	0

UPMH1[7:0]:
This register contains the mask pattern for the first octet (H1) of a received cell. This mask is applied to User-Programmable Match Pattern for H1. A one in any UPMH1[n] bit enables the corresponding bit in the Match Pattern register to be compared. A zero causes the masking of the corresponding bit.

Register 50H: RXCP User-Programmable Match Mask: H2 octet

Bit	Type	Function	Default
Bit 7	R/W	UPMH2[7]	0
Bit 6	R/W	UPMH2[6]	0
Bit 5	R/W	UPMH2[5]	0
Bit 4	R/W	UPMH2[4]	0
Bit 3	R/W	UPMH2[3]	0
Bit 2	R/W	UPMH2[2]	0
Bit 1	R/W	UPMH2[1]	0
Bit 0	R/W	UPMH2[0]	0

UPMH2[7:0]:
This register contains the mask pattern for the second octet (H2) of a received cell. This mask is applied to User-Programmable Match Pattern for H2. A one in any UPMH2[n] bit enables the corresponding bit in the Match Pattern register to be compared. A zero causes the masking of the corresponding bit.

Register 51H: RXCP User-Programmable Match Mask 2: H3 octet

Bit	Type	Function	Default
Bit 7	R/W	UPMH3[7]	0
Bit 6	R/W	UPMH3[6]	0
Bit 5	R/W	UPMH3[5]	0
Bit 4	R/W	UPMH3[4]	0
Bit 3	R/W	UPMH3[3]	0
Bit 2	R/W	UPMH3[2]	0
Bit 1	R/W	UPMH3[1]	0
Bit 0	R/W	UPMH3[0]	0

UPMH3[7:0]:
This register contains the mask pattern for the third octet (H3) of a received cell. This mask is applied to User-Programmable Match Pattern for H3. A one in any UPMH3[n] bit enables the corresponding bit in the Match Pattern register to be compared. A zero causes the masking of the corresponding bit.

Register 52H: RXCP User-Programmable Match Mask 2: H4 octet

Bit	Type	Function	Default
Bit 7	R/W	UPMH4[7]	0
Bit 6	R/W	UPMH4[6]	0
Bit 5	R/W	UPMH4[5]	0
Bit 4	R/W	UPMH4[4]	0
Bit 3	R/W	UPMH4[3]	0
Bit 2	R/W	UPMH4[2]	0
Bit 1	R/W	UPMH4[1]	0
Bit 0	R/W	UPMH4[0]	0

UPMH4[7:0]:
This register contains the mask pattern for the fourth octet (H4) of a received cell. This mask is applied to User-Programmable Match Pattern for H4. A one in any UPMH4[n] bit enables the corresponding bit in the Match Pattern register to be compared. A zero causes the masking of the corresponding bit.

Register 53H: RXCP HCS Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CHCSI	X
Bit 0	R/W	HECEN	0

HECEN:
When logic 0, the HECEN bit disables the HCS error correction routine. When logic 1, the HCS error correction routine is run to correct HCS single-bit errors.

CHCSI:
When logic 1, the CHCSI bit indicates that an interrupt due to the reception of a correctable header check sequence (HCS). This bit is reset immediately after a read to this register.

Register 54H: RXCP LCD Count Threshold

Bit	Type	Function	Default
Bit 7	R/W	LCDC[7]	1
Bit 6	R/W	LCDC[6]	0
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	1
Bit 3	R/W	LCDC[3]	0
Bit 2	R/W	LCDC[2]	1
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[7:0]:
The LCDC[7:0] bits represent the half number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation of declared (LCD). Likewise, LCD is not deasserted until receive cell processor is in cell delineation for the twice the contents of LCDC[7:0] cell periods.

The LCDC[7:0] bits determine the LCD integration time. The default value of 180 sets the cell threshold to 360. This translates to the following:

Format	Average cell period	Default LCD integration period
DS3 Direct Mapping	9.59 µs	3.45 ms
E3 G.751 Direct Mapping	13.9 µs	5.00 ms
E3 G.832	12.5 µs	4.50 ms
DS1 Direct Mapping	276 µs	99.4 ms
E1 Direct Mapping	213.7 µs	76.9 ms

Register 58H: TXCP Control

Bit	Type	Function	Default
Bit 7	R/W	HCSINS	0
Bit 6	R/W	HCSDQDB	0
Bit 5	R/W	HCSADD	0
Bit 4	R/W	FIFODP[1]	0
Bit 3	R/W	FIFODP[0]	0
Bit 2	R/W	SCR	0
Bit 1	R/W	DHCS	0
Bit 0	R/W	FIFORST	0

FIFORST:
The FIFORST bit is used to reset the transmit FIFO. When a logic 1 is written to FIFORST, the FIFO is immediately emptied, and idle/unassigned cells are transmitted. When a logic 0 is written to FIFORST, the transmit FIFO operates normally.

DHCS:
The DHCS bit controls the insertion of header check sequence (HCS) errors in the transmit stream. When a logic 1 is written to DHCS, a single HCS error is inserted in each transmitted cell. When a logic 0 is written to DHCS, the HCS is calculated and inserted normally.

SCR:
The SCR bit controls cell payload scrambling using the self synchronizing polynomial $x^{43} + 1$. Payload scrambling can be enabled for PLCP based and non-PLCP based transmission systems. When a logic 1 is written to SCR, payload scrambling is enabled. When a logic 0 is written to SCR, payloads are transmitted unscrambled.

FIFODP[1:0]:
The FIFODP[1:0] bits determine the transmit FIFO cell depth. FIFO depth control may be important in systems where the cell latency through the S/UNI-PDH must be minimized. When the FIFO is filled to the specified depth, the transmit FIFO full signal, TFIFOFB/TCA is logic 0. TIFOFB/TCA is asserted only after a complete cell has been read out; therefore, the current cell being read is included in the count. The selectable FIFO cell depths are shown in the following table:

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

Note that FIFODP[1:0] only affects when TFIFOFB/TCA is asserted. All four cells of the FIFO may be filled before an over flow is declared.

It is not recommended that the FIFO depth be set to 1 cell. If a cell write is initiated only when TFIFOFB/TCA is asserted to logic 1, half the bandwidth is lost to idle/unassigned cells. For minimum latency and maximum throughput, set the FIFO depth to 2 cells.

HCSADD:
The HCSADD bit has meaning only when HCSINS is asserted. The HCSADD bit enables the addition of the coset polynomial $x^6 + x^4 + x^2 + 1$ to the HCS octet before transmission as required by the ATM Forum UNI specification. When a logic 1 is written to HCSADD, the coset polynomial is added to the HCS. When a logic 0 is written to HCSADD, the calculated HCS value is inserted, unmodified into the transmit cell.

HCSDQDB:
The HCSDQDB bit controls the cell header octets included in the HCS calculation. When a logic 1 is written to HCSDQDB, header octets two, three, and four are included in the HCS calculation as required by the IEEE-802.6 DQDB specification. When a logic 0 is written to HCSDQDB, all four header octets are included in the HCS calculation as required by the ATM Forum UNI specification, and the ITU-T Recommendation I.432.

HCSINS:
The HCSINS bit controls the insertion of the calculated header check sequence (HCS) in the transmit stream. When a logic 1 is written to HCSINS, the calculated HCS overwrites the HCS placeholder octet position in the cell that is read from the transmit FIFO. When a logic 0 is written to HCSINS, the value passed through the FIFO in the HCS placeholder octet position is inserted unmodified in the transmit cell. The HCS value is calculated and inserted externally when HCSINS is a logic 0.

Register 59H: TXCP Interrupt Enable/Status and Control

Bit	Type	Function	Default
Bit 7	R/W	FIXPAT	0
Bit 6	R/W	HCKE	0
Bit 5	R/W	FIFOE	0
Bit 4	R/W	TFULL4	0
Bit 3	R	HCKI	X
Bit 2	R	COCAI	X
Bit 1	R	FOVRI	X
Bit 0		Unused	X

FOVRI:
The FOVRI bit is set to logic 1 when the transmit FIFO has overrun. The FOVRI bit position is set to logic 0 when this register is read.

COCAI:
The COCAI bit is set to logic 1 when a change of cell alignment (COCA) is detected. Start of cell indications are indicated by the TSOC input, and are expected during the first octet of the 53 octet data structure written to the transmit FIFO. If the FIFOs internal cell counter indicates that TSOC does not coincide with the first octet or is not present during the first octet, COCAI is set to logic 1. The COCAI bit position is set to logic 0 when this register is read.

HCKI:
The HCKI bit is set to logic 1 when a FIFO data path integrity error is detected. An external device must insert either an alternating AAH/55H or a fixed 55H pattern in the HCS octet placeholder location (the AAH/55H pattern alternates with each cell written to the transmit FIFO). The S/UNI-PDH verifies that either alternating or fixed pattern is present in the data structure read from the transmit FIFO. Any pattern discrepancy indicates a failure in the transmit data path, and causes HCKI to be set to a logic 1. The HCKI bit position is set to logic 0 when this register is read.

TFULL4:
The TFULL4 bit selects the amount of advance indication given on the transmit cell available (TFIFOFB/TCA) signal. When TFULL4 is logic 1, TFIFOFB/TCA is deasserted to logic 0 when the transmit FIFO is almost full and can accept no more than four bytes before reaching the depth specified by the FIFODP[1:0] register bits. When TFULL4 is logic 0, TCA is deasserted to logic 0 when the current FIFO access writes the last octet of a cell which fills the FIFO to the

specified depth (If the programmed depth is four and SYFIFOB is a logic 0, a write request made while TFIFOFB/TCA is low results in an overflow indication, but the write request is ignored. If SYFIFOB is a logic 1, this write request resets the FIFO, resulting in the loss of up to 4 cells).

FIFOE:
The FIFOE bit enables the generation of an interrupt when the S/UNI-PDH detects a transmit FIFO overrun, or a change of cell alignment (COCA). When a logic 1 is written to FIFOE, the interrupt generation is enabled.

HCKE:
The HCKE bit enables the generation of an interrupt when the S/UNI-PDH detects a FIFO datapath integrity error. When a logic 1 is written to HCKE, the interrupt generation is enabled.

FIXPAT:
The FIXPAT bit selects the pattern used when FIFO data path integrity checking is enabled. When FIXPAT is logic 1, the HCS octet placeholder location is checked for the fixed 55H pattern. When FIXPAT is logic 0, the HCS octet placeholder location is checked for an alternating AAH/55H pattern which alternates with each cell written to the transmit FIFO.

Register 5AH: TXCP Idle/Unassigned Cell Pattern: H1 octet

Bit	Type	Function	Default
Bit 7	R/W	H1[7]	0
Bit 6	R/W	H1[6]	0
Bit 5	R/W	H1[5]	0
Bit 4	R/W	H1[4]	0
Bit 3	R/W	H1[3]	0
Bit 2	R/W	H1[2]	0
Bit 1	R/W	H1[1]	0
Bit 0	R/W	H1[0]	0

H1[7:0]:
The H1[7:0] bits contain the cell header pattern inserted in the first octet (H1) of the idle/unassigned cell. Idle/unassigned cells are inserted when the S/UNI-PDH detects that the transmit FIFO contains no outstanding cells. H1[7] is the most significant bit and is the first bit transmitted. H1[0] is the least significant bit. This register should be set to 00H when transmitting the standard idle/unassigned cell pattern.

Register 5BH: TXCP Idle/Unassigned Cell Pattern: H2 octet

Bit	Type	Function	Default
Bit 7	R/W	H2[7]	0
Bit 6	R/W	H2[6]	0
Bit 5	R/W	H2[5]	0
Bit 4	R/W	H2[4]	0
Bit 3	R/W	H2[3]	0
Bit 2	R/W	H2[2]	0
Bit 1	R/W	H2[1]	0
Bit 0	R/W	H2[0]	0

H2[7:0]:
The H2[7:0] bits contain the cell header pattern inserted in the second octet (H2) of the idle/unassigned cell. Idle/unassigned cells are inserted when the S/UNI-PDH detects that the transmit FIFO contains no outstanding cells. H2[7] is the most significant bit and is the first bit transmitted. H2[0] is the least significant bit. This register should be set to 00H when transmitting the standard idle/unassigned cell pattern.

Register 5CH: TXCP Idle/Unassigned Cell Pattern: H3 octet

Bit	Type	Function	Default
Bit 7	R/W	H3[7]	0
Bit 6	R/W	H3[6]	0
Bit 5	R/W	H3[5]	0
Bit 4	R/W	H3[4]	0
Bit 3	R/W	H3[3]	0
Bit 2	R/W	H3[2]	0
Bit 1	R/W	H3[1]	0
Bit 0	R/W	H3[0]	0

H3[7:0]:
The H3[7:0] bits contain the cell header pattern inserted in the third octet (H3) of the idle/unassigned cell. Idle/unassigned cells are inserted when the S/UNI-PDH detects that the transmit FIFO contains no outstanding cells. H3[7] is the most significant bit and is the first bit transmitted. H3[0] is the least significant bit. This register should be set to 00H when transmitting the standard idle/unassigned cell pattern.

Register 5DH: TXCP Idle/Unassigned Cell Pattern: H4 octet

Bit	Type	Function	Default
Bit 7	R/W	H4[7]	0
Bit 6	R/W	H4[6]	0
Bit 5	R/W	H4[5]	0
Bit 4	R/W	H4[4]	0
Bit 3	R/W	H4[3]	0
Bit 2	R/W	H4[2]	0
Bit 1	R/W	H4[1]	0
Bit 0	R/W	H4[0]	0

H4[7:0]:
The H4[7:0] bits contain the cell header pattern inserted in the fourth octet (H4) of the idle/unassigned cell. Idle/unassigned cells are inserted when the S/UNI-PDH detects that the transmit FIFO contains no outstanding cells. H4[7] is the most significant bit and is the first bit transmitted. H4[0] is the least significant bit. By default, unassigned cells are transmitted. This register should be set to 01H to transmit idle cells.

Register 5EH: TXCP Idle/Unassigned Cell Pattern: H5 octet

Bit	Type	Function	Default
Bit 7	R/W	H5[7]	0
Bit 6	R/W	H5[6]	0
Bit 5	R/W	H5[5]	0
Bit 4	R/W	H5[4]	0
Bit 3	R/W	H5[3]	0
Bit 2	R/W	H5[2]	0
Bit 1	R/W	H5[1]	0
Bit 0	R/W	H5[0]	0

H5[7:0]:
The H5[7:0] bits contain the cell header pattern inserted in the fifth octet (H5, the HCS octet) of the idle/unassigned cell. Idle/unassigned cells are inserted when the S/UNI-PDH detects that the transmit FIFO contains no outstanding cells. H5[7] is the most significant bit and is the first bit transmitted. H5[0] is the least significant bit. This register should be written with the correct header check sequence value corresponding to the patterns written to the H1 - H4 octet Idle/Unassigned Cell Pattern Registers.

Register 5FH: TXCP Idle/Unassigned Cell Payload

Bit	Type	Function	Default
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	0
Bit 5	R/W	PAYLD[5]	0
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	0
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	0
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]:
The PAYLD[7:0] bits contain the pattern inserted in the idle/unassigned cell payload. Idle/unassigned cells are inserted when the S/UNI-PDH detects that the transmit FIFO contains no outstanding cells. PAYLD[7] is the most significant bit and is the first bit transmitted. PAYLD[0] is the least significant bit.

Register 60H: E3 FRMR Framing Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	UNI	0
Bit 3	R/W	FORMAT[1]	0
Bit 2	R/W	FORMAT[0]	0
Bit 1	R/W	REFRDIS	0
Bit 0	R/W	REFR	0

REFR:
A transition from logic 0 to logic 1 in the REFR bit position forces the E3 Framer to initiate a search for frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to initiate subsequent searches for frame alignment.

REFRDIS:
The REFRDIS bit disables reframing under the consecutive framing bit error condition once frame alignment has been found, leaving reframing to be initiated only by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur when four consecutive framing patterns are received in error.

FORMAT[1:0]:
The FORMAT[1:0] bits determine the framing mode used for pattern matching when finding frame alignment and for generating the output status signals. Each time the FORMAT[1:0] bits are reprogrammed (modes changed) a reframe command should be issued (see REFR bit above) . Switching between G.751 and G.832 modes without forcing a reframe could cause framer lockup. The FORMAT[1:0] bits select one of two framing formats:

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

UNI:
The UNI bit selects the mode of the receive data interface. When UNI is logic 1, the E3-FRMR expects unipolar data on the RDAT input and accepts line code violation indications on the ROHM input. When UNI is logic 0, the E3-FRMR expects bipolar data on the RPOS and RNEG inputs and decodes the pulses according to the HDB3 line code.

Reserved:
The Reserved bit must be programmed to logic 0 for proper operation.

Register 61H: E3 FRMR Maintenance Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	WORDBIP	0
Bit 4	R/W	TANDEM	0
Bit 3	R/W	WORDERR	0
Bit 2	R/W	PYLD&JUST	0
Bit 1	R/W	FERFDET	0
Bit 0	R/W	TMARKDET	0

TMARKDET:
The TMARKDET bit determines the persistency check performed on the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TMARKDET is logic 1, the Timing Marker bit must be in the same state for 5 consecutive frames before the TIMEMK status is changed to that state. When TMARKDET is logic 0, the Timing Marker bit must be in the same state for 3 consecutive frames. When a framing mode other than G.832 is selected, the setting of the TMARKDET bit is ignored.

FERFDET:
The FERFDET bit determines the persistency check performed on the Far End Receive Failure (FERF) bit (bit 1 of the G.832 Maintenance and Adaptation byte) or on the Remote Alarm indication (RAI) bit (bit 11 of the frame in G.751 mode). When FERFDET is logic 1, the FERF, or RAI, bit must be in the same state for 5 consecutive frames before the FERF/RAI status is changed to that state. When FERFDET is logic 0, the FERF, or RAI, bit must be in the same state for 3 consecutive frames.

PYLD&JUST:
The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing mode G.751 is indicated as overhead or payload. When PYLD&JUST is logic 1, the justification service bits and the tributary justification bits are indicated as payload to the SPLR. When PYLD&JUST is logic 0, the justification service and tributary justification bits are indicated as overhead to SPLR. For G.751 applications, this bit must be set to logic 1 for correct cell mapping.

WORDERR:
The WORDERR bit selects whether the framing bit error indication pulses

accumulated in PMON indicate all bit errors in the framing pattern or only one error for one or more errors in the framing pattern. When WORDERR is logic 1, the FERR indication to PMON pulses once per frame, accumulating one error for one or more framing bit errors occurred. When WORDERR is logic 0, the FERR indication to PMON pulses for each and every framing bit error that occurs; PMON accumulates all framing bit errors.

TANDEM:
The TANDEM bit selects whether the NETOP output is used for Tandem Connection Maintenance. When TANDEM is logic 1, bits 1 to 4 of the G.832 format Network Requirement overhead byte are used as an incoming error count and bits 5 to 8 as a communications channel. When TANDEM is logic 0, the NR byte output is used as a communications channel for bits 1 to 8.

WORDBIP:
The WORDBIP bit selects whether the parity bit error indication pulses to the E3-TRAN block indicate all bit errors in the BIP-8 pattern or only one error for one or more errors in the BIP-8 pattern. When WORDBIP is logic 1, the parity error indication to the E3 TRAN block pulses once per frame, indicating that one or more parity bit errors occurred. When WORDBIP is logic 0, the parity error indication to the E3-TRAN block pulses for each and every parity bit error that occurs. For G.832 applications, this bit should be set to logic 1.

Register 62H: E3 FRMR Framing Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CZDE	0
Bit 3	R/W	LOSE	0
Bit 2	R/W	LCVE	0
Bit 1	R/W	COFAE	0
Bit 0	R/W	OOFE	0

OOFE:
The OOFE bit is an interrupt enable. When OOFE is logic 1, a change of state of the OOF status generates an interrupt and sets the INTB output to logic 0. When OOFE is logic 0, changes of state of the OOF status are disabled from causing interrupts on the INTB output.

COFAE:
The COFAE bit is an interrupt enable. When COFAE is logic 1, a change of frame alignment generates an interrupt and sets the INTB output to logic 0. When COFAE is logic 0, changes of frame alignment are disabled from causing interrupts on the INTB output.

LCVE:
The LCVE bit is an interrupt enable. When LCVE is logic 1, detection of a line code violation generates an interrupt and sets the INTB output to logic 0. When LCVE is logic 0, occurrences of line code violations are disabled from causing interrupts on the INTB output.

LOSE:
The LOSE bit is an interrupt enable. When LOSE is logic 1, a change of state of the loss-of-signal generates an interrupt and sets the INTB output to logic 0. When LOSE is logic 0, occurrences of loss-of-signal are disabled from causing interrupts on the INTB output.

CZDE:
The CZDE bit is an interrupt enable. When CZDE is logic 1, detection of four consecutive zeros in the HDB3-encoded stream generates an interrupt and sets

the INTB output to logic 0. When CZDE is logic 0, occurrences of consecutive zeros are disabled from causing interrupts on the INTB output.

Register 63H: E3 FRMR Framing Interrupt Indication and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	CZDI	X
Bit 5	R	LOSI	X
Bit 4	R	LCVI	X
Bit 3	R	COFAI	X
Bit 2	R	OOFI	X
Bit 1	R	LOS	X
Bit 0	R	OOF	X

OOF:
The OOF bit indicates the current state of the E3-FRMR. When OOF is logic 1, the E3-FRMR is out of frame alignment and actively searching for the new alignment. While OOF is high all status indications and overhead extraction continue with the previous known alignment. When OOF is logic 0, the E3-FRMR has found a valid frame alignment and is operating in a maintenance mode, indicating framing bit errors, and extracting and processing overhead bits. During reset, OOF is set to logic 1, but the setting may change prior to the register being read.

LOS:
The LOS bit indicates the current state of the Loss-Of-Signal detector. When LOS is logic 1, the E3-FRMR has received 32 consecutive RCLK cycles with no occurrences of bipolar data on RPOS and RNEG. When LOS is logic 0, the FRMR is receiving valid bipolar data. When the E3-FRMR has declared loss of signal, the LOS indication is set to logic 0 (deasserted) when the E3-FRMR has received 32 consecutive RCLK cycles containing no occurrences of 4 consecutive zeros. The LOS bit is forced to logic 0 if the UNI bit is logic 1. During reset, LOS is set to logic 0, but the setting may change prior to the register being read.

OOFI:
A logic 1 OOFI bit indicates a change in the OOF status. The OOFI bit is cleared to logic 0 upon the completion of the register read. When OOFI is logic 0, it indicates that no OOF state change has occurred since the last time this register was read.

COFAI:
The COFAI bit indicates that a change of frame alignment between the previous

alignment and the newly found alignment has occurred. When COFAI is logic 1, the last high-to-low transition on the OOF signal resulted in the new frame alignment differing from the previous one. The COFAI bit is cleared to logic 0 upon the completion of the register read. When COFAI is logic 0, it indicates that no change in frame alignment has occurred when OOF went low.

LCVI:
The LCVI bit indicates that a line code violation has occurred. When LCVI is logic 1, a line code violation on the RPOS and RNEG inputs was detected since the last time this register was read. The LCVI bit is cleared to logic 0 upon the completion of the register read. When LCVI is logic 0, it indicates that no line code violation was detected since the last register read. When the UNI bit in the Framing Options register is logic 1, the LCVI is forced to logic 0.

LOSI:
The LOSI bit indicates that a state transition occurred on the LOS status signal. When LOSI is logic 1, a high-to-low or low-to-high transition occurred on the LOS status signal since the last time this register was read. The LOSI bit is cleared to logic 0 upon the completion of the register read. When LOSI is logic 0, it indicates that no state change has occurred on LOS since the last time this register was read. When the UNI bit in the Framing Options register is logic 1, the LOSI is forced to logic 0.

CZDI:
The CZDI bit indicates that four consecutive zeros in the HDB3-encoded stream have been detected. CZDI is asserted to a logic 1, whenever the CZD signal is asserted. The CZDI bit is cleared to a logic 0 upon the completion of the register read. When CZDI is logic 0, it indicates that no occurrences of four consecutive zeros was detected since the last register read. When the UNI bit in the Framing Options register is logic 1, the CZDI indication is forced to logic 0.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The indication bits (bits 2,3,4,5,6 of this register) are cleared to logic 0 after the register is read; the INTB output is also cleared to logic 1 if the interrupt was generated by any of these five events.

Register 64H: E3 FRMR Maintenance Event Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	FERRE	0
Bit 6	R/W	PERRE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	FEBEE	0
Bit 2	R/W	PTYPEE	0
Bit 1	R/W	TIMEMKE	0
Bit 0	R/W	NATUSEE	0

NATUSEE:
The NATUSEE bit is an interrupt enable. When NATUSEE is logic 1, an interrupt is generated on the INTB output when the National Use bit (bit 12 of the frame in G.751 E3 mode) changes state. When NATUSEE is logic 0, changes in state of the National Use bit does not cause an interrupt on INTB.

TIMEMKE:
The TIMEMKE bit is an interrupt enable. When TIMEMKE is logic 1, an interrupt is generated on the INTB output when the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) changes state after the selected persistency check is applied. When TIMEMKE is logic 0, changes in state of the Timing Marker bit does not cause an interrupt on INTB.

PTYPEE:
The PTYPEE bit is an interrupt enable. When PTYPEE is logic 1, an interrupt is generated on the INTB output when the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) change state. When PTYPEE is logic 0, changes in state of the Payload Type bits does not cause an interrupt on INTB.

FEBEE:
The FEBEE bit is an interrupt enable. When FEBEE is logic 1, an interrupt is generated on the INTB output when the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) changes state. When FEBEE is logic 0, changes in state of the FEBE bit does not cause an interrupt on INTB.

FERFE:
The FERFE bit is an interrupt enable. When FERFE is logic 1, an interrupt is generated on the INTB output when the Far End Receive Failure indication bit

(bit 1 of the G.832 Maintenance and Adaptation byte), or when the Remote Alarm indication bit (bit 11 of the frame in G.751) changes state after the selected persistency check is applied. When FERFE is logic 0, changes in state of the FERF or RAI bit does not cause an interrupt on INTB.

AISDE:
The AISDE bit is an interrupt enable. When AISDE is logic 1, an interrupt is generated on the INTB output when the AISD indication changes state. When AISDE is logic 0, changes in state of the AISD signal does not cause an interrupt on INTB.

PERRE:
The PERRE bit is an interrupt enable. When PERRE is logic 1, an interrupt is generated on the INTB output when a BIP-8 error (in G.832 mode) is detected. When PERRE is logic 0, occurrences of BIP-8 errors do not cause an interrupt on INTB.

FERRE:
The FERRE bit is an interrupt enable. When FERRE is logic 1, an interrupt is generated on the INTB output when a framing bit error is detected. When FERRE is logic 0, occurrences of framing bit errors do not cause an interrupt on INTB.

Register 65H: E3 FRMR Maintenance Event Interrupt Indication

Bit	Type	Function	Default
Bit 7	R	FERRI	0
Bit 6	R	PERRI	0
Bit 5	R	AISDI	0
Bit 4	R	FERFI	0
Bit 3	R	FEBEI	0
Bit 2	R	PTYPEI	0
Bit 1	R	TIMEMKI	0
Bit 0	R	NATUSEI	0

NATUSEI:
The NATUSEI bit is a transition Indication. When NATUSEI is logic 1, a change of state of the National Use bit (bit 12 of the frame in G.751 E3 mode) has occurred. When NATUSEI is logic 0, no change of state of the National Use bit has occurred since the last time this register was read.

TIMEMKI:
The TIMEMKI bit is a transition indication. When TIMEMKI is logic 1, a change in state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte) has occurred. When TIMEMKI is logic 0, no changes in the state of the Timing Marker bit occurred since the last time this register was read.

PTYPEI:
The PTYPEI bit is a transition indication. When PTYPEI is logic 1, a change of state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte) has occurred. When PTYPEI is logic 0, no changes in the state of the Payload Type bits has occurred since the last time this register was read.

FEBEI:
The FEBEI bit is a transition indication. When FEBEI is logic 1, a change of state of the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte) has occurred. When FEBEI is logic 0, no changes in the state of the FEBE bit has occurred since the last time this register was read.

FERFI:
The FERFI bit is a transition indication. When FERFI is logic 1, a change of state of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or when the Remote Alarm indication bit (bit 12 of the frame in

G.751) has occurred. When FERFI is logic 0, no changes in the state of the FERF/RAI bit has occurred since the last time this register was read.

AISDI:
The AISDI bit is a transition indication. When AISDI is logic 1, a change in state of the AISD indication has occurred. When AISDI is logic 0, no changes in the state of the AISD signal has occurred since the last time this register was read.

PERRI:
The PERRI bit is an event indication. When PERRI is logic 1, the occurrence of one or more BIP-8 errors (in G.832 mode) has been detected. When PERRI is logic 0, no occurrences of BIP-8 errors have occurred since the last time this register was read.

FERRI:
The FERRI bit is an event indication. When FERRI is logic 1, the occurrence of one or more framing bit error has been detected. When FERRI is logic 0, no occurrences of framing bit errors have occurred since the last time this register was read.

The transition/event interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the activity of the maintenance events. The contents of this register are cleared to logic 0 after the register is read; the INTB output is also cleared to logic 1 if the interrupt was generated by any of the Maintenance Event outputs.

Register 66H: E3 FRMR Maintenance Event Status

Bit	Type	Function	Default
Bit 7	R	AISD	X
Bit 6	R	FERF/RAI	X
Bit 5	R	FEBE	X
Bit 4	R	PTYPE[2]	X
Bit 3	R	PTYPE[1]	X
Bit 2	R	PTYPE[0]	X
Bit 1	R	TIMEMK	X
Bit 0	R	NATUSE	X

NATUSE:
The NATUSE bit reflects the state of the extracted National Use bit (bit 12 of the frame in G.751 E3 mode).

TIMEMK:
The TIMEMK bit reflects the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte).

PTYPE[2:0]:
The PTYPE[2:0] bits reflect the state of the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte). These bits are not latched and should be read 2 or 3 times in rapid succession to ensure a coherent binary value.

FEBE:
The FEBE bit reflects the state of the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte).

FERF/RAI:
The FERF/RAI bit reflects the value of the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the Remote Alarm indication bit (bit 11 of the frame in G.751) when the value has been the same for either 3 or 5 consecutive frames.

AISD:
The AISD bit reflects the state of the AIS detection circuitry. When AISD is logic 1, less than 8 zeros (in G.832 mode), or less than 5 zeros (in G.751 mode), were detected during one complete frame period while the FRMR is out of frame alignment. When AISD is logic 0, 8 or more zeros (in G.832 mode), or 5 or more

zeros (in G.751 mode), were detected during one complete frame period, or the FRMR has found frame alignment.

Register 68H: E3 TRAN Framing Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TANDEM	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	FORMAT[1]	0
Bit 0	R/W	FORMAT[0]	0

FORMAT[1:0]:
The FORMAT[1:0] bits determine the framing mode used for framing pattern when generating the formatted output data stream. The FORMAT[1:0] bits select one of two framing formats:

FORMAT[1]	FORMAT[0]	Framing Format Selected
0	0	G.751 E3 format
0	1	G.832 E3 format
1	0	Reserved
1	1	Reserved

When the S/UNI-PDH is operating in modes other than E3 G.832, the FORMAT[0:1] bits should both be programmed as logic 0. Otherwise cell or data corruption may occur.

Reserved :
The Reserved bit must be programmed to logic 0 for correct operation.

TANDEM:
The TANDEM bit selects whether Tandem Connection is used when the transmitter is configured for G.832. When TANDEM is logic 1 and the FORMAT[1:0]=01 binary (i.e., G.832 E3 format), zeros are inserted into bits 1-4 of the Network Operator byte and the data provided by XFDL or the TDLSIG input is inserted into bits 5-8 of the Network Operator byte. When TANDEM is logic 0 and the FORMAT[1:0]=01 binary, the incoming error count is ignored and the data provided by XFDL or the TDLSIG input is inserted into bits 1-8 of the Network Operator byte. When the FORMAT[1:0] bits select any other format than G.832, the TANDEM register bit is ignored. It is not expected that Tandem

Connection is used in most S/UNI-PDH applications; this bit should be programmed to logic 0.

Register 69H: E3 TRAN Status and Diagnostic Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	PYLD&JUST	0
Bit 5	R/W	CPERR	0
Bit 4	R/W	DFERR	0
Bit 3	R/W	DLCV	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TAIS	0
Bit 0	R/W	NATUSE	1

NATUSE:
The NATUSE bit determines the default value of the National Use bit inserted into the G.751 E3 frame overhead. The value of the NATUSE bit is logically ORed with the bit collected once per frame from the TDLSIG input (if TNETOP is set to logic 1) or from the internal HDLC transmitter (if TNETOP is set to logic 0). When NATUSE is logic 1, the National Use bit (bit 12 in G.751) is forced to logic 1 regardless of the bit input from the internal HDLC transmitter or TDLSIG. When NATUSE is logic 0, the National Use bit is set to the value sampled on the TDLSIG input, or from the internal HDLC transmitter. If the TRAN is configured for G.832 mode, this bit is ignored.

TAIS:
When TAIS is logic 1, the output data stream (TPOS/TNEG in bipolar mode, TDAT in unipolar mode) is forced to logic 1 to indicate AIS. When TAIS is logic 0, the TDAT stream is allowed to function normally.

Reserved:
The Reserved bit must be programmed to logic 0 for proper operation.

DLCV:
The DLCV bit selects whether a line code violation is generated for diagnostic purposes. When DLCV changes from logic 0 to logic 1, single LCV is generated; in HDB3, the LCV is generated by causing a bipolar violation pulse of the same polarity to the previous bipolar violation. To generate another LCV, the DLCV register bit must first be written to logic 0 and then to logic 1 again.

DFERR:
The DFERR bit selects whether the framing pattern is corrupted for diagnostic

purposes. When DFERR is logic 1, the framing pattern inserted into the output data stream is inverted. When DFERR is logic 0, the unaltered framing pattern inserted into the output data stream.

CPERR:
The CPERR bit enables continuous generation of BIP-8 errors for diagnostic purposes. When CPERR is logic 1, the calculated BIP-8 value is continuously inverted according to the error mask specified by the BIP-8 Error Mask register and inserted into the G.832 EM byte. When CPERR is logic 0, the calculated BIP-8 value is altered only once, according to the error mask specified by the BIP-8 Error Mask register, and inserted into the EM byte.

PYLD&JUST:
The PYLD&JUST bit selects whether the justification service bits and the tributary justification bits in framing modes G.751 is indicated as overhead or payload. When PYLD&JUST is logic 1, the justification service bits and the tributary justification bits are indicated as payload. When PYLD&JUST is logic 0, the justification service and tributary justification bits are indicated as overhead. For G.751 applications, this bit must be set to logic 1 for correct cell mapping.

Register 6AH: E3 TRAN BIP-8 Error Mask

Bit	Type	Function	Default
Bit 7	R/W	MBIP[7]	0
Bit 6	R/W	MBIP[6]	0
Bit 5	R/W	MBIP[5]	0
Bit 4	R/W	MBIP[4]	0
Bit 3	R/W	MBIP[3]	0
Bit 2	R/W	MBIP[2]	0
Bit 1	R/W	MBIP[1]	0
Bit 0	R/W	MBIP[0]	0

MBIP[7:0]:
The MBIP[7:0] bits act as an error mask to cause the transmitter to insert up to 8 BIP-8 errors. The contents of this register are XORed with the calculated BIP-8 byte and inserted into the G.832 EM byte of the frame. A logic 1 in any MBIP bit position causes that bit position in the EM byte to be inverted. Writing this register with a mask value causes that mask to be applied only once; if continuous BIP-8 errors are desired, the CPERR bit in the Status and Diagnostic Options register can be used.

Register 6BH: E3 TRAN Maintenance and Adaptation Options

Bit	Type	Function	Default
Bit 7	R/W	FERF/RAI	0
Bit 6	R/W	FEBE	0
Bit 5	R/W	PTYPE[2]	0
Bit 4	R/W	PTYPE[1]	0
Bit 3	R/W	PTYPE[0]	0
Bit 2	R/W	TUMFRM[1]	0
Bit 1	R/W	TUMFRM[0]	0
Bit 0	R/W	TIMEMK	0

TIMEMK:
The TIMEMK bit determines the state of the Timing Marker bit (bit 8 of the G.832 Maintenance and Adaptation byte). When TIMEMK is set to logic 1, the Timing Marker bit in the MA byte is set to logic 1. When TIMEMK is set to logic 0, the Timing Marker bit in the MA byte is set to logic 0.

TUMFRM[1:0]:
The TUMFRM[1:0] bits reflect the value to be inserted in the Tributary Unit Multiframe bits (bits 6, and 7 of the G.832 Maintenance and Adaptation byte). These bits are logically ORed with the TUMFRM[1:0] overhead signals from the TOH input before being inserted in the MA byte.

PTYPE[2:0]:
The PTYPE[2:0] bits reflect the value to be inserted in the Payload Type bits (bits 3,4,5 of the G.832 Maintenance and Adaptation byte).

FEBE:
The FEBE bit reflects the value to be inserted in the Far End Block Error indication bit (bit 2 of the G.832 Maintenance and Adaptation byte). The FEBE bit value is logically ORed with the FEBE indications generated by the FRMR for any detected BIP-8 errors. When the FEBE bit is logic 1, bit 2 of the G.832 MA byte is set to logic 1; when the FEBE bit is logic 0, any BIP-8 error indications from the FRMR causes bit 2 of the MA byte to be set to logic 1.

FERF/RAI:
The FERF/RAI bit reflects the value to be inserted in the Far End Receive Failure indication bit (bit 1 of the G.832 Maintenance and Adaptation byte), or the value of the Remote Alarm indication bit (bit 11 of the frame in G.751). The FERF/RAI

bit is logically ORed with the XFERF/XRAI bit position in the overhead stream. When the OR of the two signals is logic 1, the FERF or RAI bit in the frame is set to logic 1; when neither signal is logic 1, the FERF or RAI bit is set to logic 0.

Register 6CH: TTB Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

LEN16:
The path trace message length bit (LEN16) selects the length of the message to be 16 bytes or 64 bytes. The LEN16 bit must be programmed to logic 1 for proper operation in G.832 applications.

NOSYNC:
The NOSYNC bit disables synchronization to the Trail Trace message. When NOSYNC is set high, synchronization is disabled and the bytes of the Trail Trace message are captured by the TTB in a circular buffer. When NOSYNC is set low, the TTB synchronizes to the byte with the most significant bit set high and places that byte in the first location in the capture buffer page.

TNULL:
The transmit null (TNULL) bit controls the insertion of all-zeros into the outgoing Trail Trace message. The null insertion should be used when microprocessor accesses that change the outgoing trail trace message are being performed. When TNULL is set high, an all-zeros byte is inserted to the transmit stream. When this bit is set low, the contents of the transmit trace buffer are sent.

PER5:
The receive trace identifier persistency bit (PER5) controls the number of times that persistency check is made in order to accept the received message. When this bit is set high, five identical message required in order to accept the message. When this bit set low, three unchanged consecutive messages are required.

RTIMIE:
The receive trace identifier mismatch interrupt enable (RTIMIE) controls the

activation of the interrupt output when comparison between the accepted trace identifier message and the expected trace identifier message changes state from match to mismatch and vice versa. When RTIMIE is set high, changes in match state will activate the interrupt output. When RTIMIE set low, trail trace message match state changes will not affect INTB.

RTIUIE:

The receive trace identifier unstable interrupt enable (RTIUIE) control the activation of the interrupt output when the receive trace identifier message changes state from stable to unstable and vice versa. When RTIUIE is set high, changes in the state of the trail trace message unstable indication will activate the interrupt output. When RTIUIE set low, trail trace unstable state changes will not effect INTB.

RRAMACC:

The receive RAM access (RRAMACC) control bit is used by the microprocessor to identify that the access from the microprocessor is to the receive trace buffers (addresses 0 - 127) or to the transmit trace buffer (addresses 128 - 191). When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

Register 6DH: TTB Trail Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

RTIMV:
The receive trace identifier mismatch value status bit (RTIMV) is set high when the accepted message differs from the expected message. RTIMV is set low when the accepted message is equal to the expected message. A mismatch is not declared if the accepted trail trace message string is all-zeros.

RTIMI:
The receive trace identifier mismatch indication status bit (RTIMI) is set high when match/mismatch status of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read.

RTIUV:
The receive trace identifier unstable value status bit (RTIUV) is set high when 8 messages that differ from its immediate predecessor are received. RTIUV is set low and the unstable message count is reset when 3 or 5 (depending on PER5 control bit) consecutive identical messages are received.

RTIUI:
The receive trace identifier unstable indication status bit (RTIUV) is set high when the stable/unstable status of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read.

BUSY:
The BUSY bit reports whether a previously initiated indirect read or write to the trail trace RAM has been completed. BUSY is set high upon writing to the TTB Indirect Address register, and stays high until the access has completed. At this point, BUSY is set low. This register should be polled to determine when either

new data is available in the TTB Indirect Data register after an indirect read, or when the TTB is ready to accept another write access.

Register 6EH: TTB Indirect Address

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

A[6:0]:
The indirect read address bits (A[6:0]) indexes into the trail trace identifier buffers. When RRAMACC is set high, decimal addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive G.832 E3 stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor. When RRAMACC is set low, decimal addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted in the TR bytes of the G.832 E3 transmit stream. In this case A[6] is a don't care (I.e., address 0 and address 64 are indexes to the same location in the buffer). Note that only the first 16 addresses need to be written with the trail trace message to be transmitted.

RWB:
The access control bit (RWB) selects between an indirect read or write access to the static page of the trail trace message buffer. Writing to this indirect address register initiates an external microprocessor access to the static page of the trail trace message buffer. When RWB is set high, a read access is initiated. The data read is available upon completion of the access in the TTB Indirect Data register. When RWB is set low, a write access is initiated. The data in the TTB Indirect Data register will be written to the addressed location in the static page.

Register 6FH: TTB Indirect Data

Bit	Type	Function	Default
Bit 7	R/W	D[7]	X
Bit 6	R/W	D[6]	X
Bit 5	R/W	D[5]	X
Bit 4	R/W	D[4]	X
Bit 3	R/W	D[3]	X
Bit 2	R/W	D[2]	X
Bit 1	R/W	D[1]	X
Bit 0	R/W	D[0]	X

D[7:0]:
The indirect data bits (D[7:0]) contain either the data read from a message buffer after an indirect read operation has completed, or the data to be written to the RAM for an indirect write operation. Note that the write data must be set up in this register before an indirect write is initiated. Data read from this register reflects the value written until the completion of a subsequent indirect read operation.

Register 70H: TTB Expected Payload Type Label

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	EXPLD[2]	0
Bit 1	R/W	EXPLD[1]	0
Bit 0	R/W	EXPLD[0]	0

EXPLD[2:0]:
The EXPLD[2:0] bits contain the expected payload type label bits of the G.832 E3 Maintenance and Adaptation (MA) byte. The EXPLD[2:0] bits are compared with the received payload type label extracted from the receive stream. A payload type label mismatch (PLDM) is declared if the received payload type bits differs from the expected payload type. If enabled, an interrupt is asserted upon declaration and removal of PLDM.

For compatibility with old equipment that inserts 000B for unequipped or 001B for equipped, regardless of the payload type, the receive payload type label mismatch mechanism is based on the following table:

Expected	Received	Action
000	000	Match
000	001	Mismatch
000	XXX	Mismatch
001	000	Mismatch
001	001	Match
001	XXX	Match
XXX	000	Mismatch
XXX	001	Match
XXX	XXX	Match
XXX	YYY	Mismatch

Note:

XXX, YYY = anything except 000B or 001B, and XXX is not equal to YYY.

Reserved:
The reserved bits must be written to logic 0 for proper operation.

Register 71H: TTB Payload Type Label Control/Status:

Bit	Type	Function	Default
Bit 7	R/W	RPLDUIE	0
Bit 6	R/W	RPLDMIE	0
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	RPLDUI	X
Bit 2	R	RPLDUV	X
Bit 1	R	RPLDMI	X
Bit 0	R	RPLDMV	X

RPLDMV:
The receive payload type label mismatch status bit (RPLDMV) reports the match/mismatch status between the expected and the received payload type label. RPLDMV is set high when the received payload type bits differ from the expected payload type written to the TTB Expected Payload Type Label Register. The PLDMV bit is set low when the received payload type matches the expected payload type.

RPLDMI:
The receive payload type label mismatch interrupt status bit (RPLDMI) is set high when the match/mismatch status between the received and the expected payload type label changes state. This bit (and the interrupt) is cleared when this register is read.

RPLDUV:
The receive payload type label unstable status bit (RPLDUV) reports the stable/unstable status of the payload type label bits in the receive stream. RPLDUV is set high when 5 labels that differ from its immediate predecessor are received. RPLDUV is set low and the unstable label count is reset when 5 consecutive identical labels are received.

RPLDUI:
The receive payload type label unstable interrupt status bit (RPLDUI) is set high when the stable/unstable status of the path signal label changes state. This bit (and the interrupt) is cleared when this register is read.

RPLDMIE:
The receive payload type label mismatch interrupt enable bit (RPLDMIE) controls

the activation of the interrupt output when the comparison between received and the expected payload type label changes state from match to mismatch and vice versa. When RPLDMIE is set high, changes in match state activates the interrupt output. When RPLDMIE is set low, changes from match to mismatch or mismatch to match will not generate an interrupt.

RPLDUIE:
The receive payload type label unstable interrupt enable bit (RPLDUIE) controls the activation of the interrupt output when the received payload type label changes state from stable to unstable and vice versa. When RPLDUIE is set high, changes in stable state activates the interrupt output. When RPLDUIE is set low, changes in the stable state will not generate and interrupt.

Register 74H: Sync FIFO Parity Control/Status:

Bit	Type	Function	Default
Bit 7	R/W	TBE	0
Bit 6	R	TBI	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	REVEN	0
Bit 2	R/W	TEVEN	0
Bit 1	R/W	TPERRE	0
Bit 0	R	TPERRI	0

TPERRI:
When the TPERRI bit is logic 1, it indicates that a parity error was detected on the incoming transmit FIFO interface. When TPERRI is logic 0, no parity error was detected. The TPERRI bit should be ignored when the S/UNI-PDH is packaged in the 84-pin PLCC.

TPERRE:
The TPERRE bit is an interrupt enable. When TPERRE is logic 1, a parity error detected on the transmit FIFO interface causes a microprocessor interrupt to be generated. When TPERRE is logic 0, a parity error does not cause an interrupt.

TEVEN:
The TEVEN bit selects the type of parity calculated and compared on the transmit synchronous FIFO interface. When TEVEN is logic 1, even parity is calculated across the FWDATA[7:0] bus and compared to the incoming parity bit on TXPRTY. If there is a mismatch, the parity error indication, TPERRI, is forced to logic 1, and an interrupt is generated, if enabled. When TEVEN is logic 0, odd parity is calculated across FWDATA[7:0] and compared to TXPRTY. Again, a parity error is indicated if there is a mismatch. Signals RXPRTY and TXPRTY are only available in the 100-pin PQFP. In the 84-pin PLCC, parity error indications on TPERRI should be ignored.

REVEN:
The REVEN bit selects the type of parity calculated and output on the receive synchronous FIFO interface. When REVEN is logic 1, even parity is calculated across the FRDATA[7:0] bus and indicated on the outgoing parity bit, RXPRTY. When REVEN is logic 0, odd parity is calculated across FRDATA[7:0] and indicated on RXPRTY. Signals RXPRTY and TXPRTY are only available in the 100-pin PQFP.

TBI:
The TBI bit indicates there is an unserviced interrupt indication associated with the trail trace buffer (TTB). The TBI bit is suppressed if the interrupt enable bits of the TTB block are all logic 0.

TBE:
The TBE bit enables the trail trace buffer as an interrupt source. If TBE is a logic 1, the trail trace buffer interrupt is enabled, and may be reported on INTB. Note that interrupt enable bits contained in the TTB block must also be set to a logic 1 to enable interrupt generation.

10.1 Basic Operating Modes

The following table suggests some of the S/UNI-PDH registers settings (in hexadecimal) for basic modes of operation. ADM stands for ATM Direct Mapping, and PLCP stands for Physical Layer Convergence Protocol. The '--' symbol indicates a "don't care" value.

Mode of Operation	S/UNI-PDH Registers (hexadecimal)											
	00	08	20	28	2C	40	41	58	60	61	68	69
E3 G.832 ADM	40	--	--	41	41	2C	01	A4	04	20	01	00
E3.G.751 ADM	40	--	--	40	40	2C	01	A4	00	04	00	41
T3 C-bit ADM	00	01	01	00	00	2C	01	A4	--	--	--	--
T3 M23 ADM	00	00	00	00	00	2C	01	A4	--	--	--	--
E1 ADM	08	--	--	C0	C0	2C	01	A4	--	--	--	--
T1 ADM	08	--	--	80	80	2C	01	A4	--	--	--	--
E3 G.751 PLCP	40	--	--	44	44	2C	00	A4	00	04	00	41
T3 C-bit PLCP	00	01	01	04	04	2C	00	A4	--	--	--	--
T3 M23 PLCP	00	00	00	04	04	2C	00	A4	--	--	--	--
E1 PLCP	08	--	--	C4	C4	2C	00	A4	--	--	--	--
T1 PLCP	08	--	--	84	84	2C	00	A4	--	--	--	--
Ext.Framer ADM	08	--	--	81	81	2C	01	A4	--	--	--	--

When configured for ATM Direct Mapping with the addition of the Coset Polynomial to the HCS byte (reg 40H and 58H, HCSADD=1):

- The TXCP Idle/Unassigned Cell Pattern Registers (5AH through 5EH) must be programmed as follows:
  00H, 00H, 00H, 01H, 52H for IDLE or
  00H, 00H, 00H, 00H, 55H for UNASSIGNED
- The TXCP Idle/Unassigned Cell Payload (reg 5FH) must be programmed to 6AH

The LEN16 bit in register 6CH must be programmed to logic 1 in E3 G.832 applications.

The RXCP Idle/Unassigned Cell Pattern Registers (43H through 46H), RXCP Idle/Unassigned Cell Mask Registers (47H through 4AH), RXCP User Programmable Match Pattern Registers (4BH through 4EH) and RXCP User Programmable Match Mask Registers (4FH through 52H) need to be programmed

to allow correct filtering. If no user programmable match pattern is required the registers could be configured as follows:

- 00H,00H,00H,01H (Idle) for the Idle/Unassigned Cell Pattern Registers
- FFH,FFH,FFH,FFH for the Idle/Unassigned Cell Mask Registers
- 00H,00H,00H,00H (Unassigned) for User Programmable Match Pattern Registers
- FFH,FFH, FFH,FFH for the User Programmable Match Mask Registers

S/UNI-PDH register 00H controls the various loopback or bypass modes. The following table shows what value must be logically OR'ed with the previous table's register 00H value to place the S/UNI-PDH in the specified loopback or bypass mode:

Loopback or Bypass Mode	OR Value (hex)	Note
Line Loopback	80	3
Payload Loopback	02	
Cell Loopback	11	
Diagnostic Loopback	04	1,3
FIFO Bypass	20	2

Note:

1) Diagnostic loopback should not be set when either cell, payload or line loopback is set.
2) FIFO bypass requires PLCP formatted transmission frames.
3) These loopback modes are not available for E1 direct-mapped operation.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-PDH. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[7]) is high.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the S/UNI-PDH are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Test Mode Register Memory Map

Address	Register
00H-7FH	*Reserved for Normal Mode Registers*
80H	Master Test
81H	PDH Test Register 0
82H-85H	Reserved
86H	RBOC Test Register 0
87H	RBOC Test Register 1
88H	DS3 FRMR Test Register 0
89H	DS3 FRMR Test Register 1
8AH	DS3 FRMR Test Register 2
8BH	DS3 FRMR Test Register 3
8CH	RFDL Test Register 0
8DH	RFDL Test Register 1
8EH-8FH	Reserved
90H	PMON Test Register 0
91H	PMON Test Register 1
92H-9FH	Reserved
A0H	DS3 TRAN Test Register 0
A1H	DS3 TRAN Test Register 1
A2H	DS3 TRAN Test Register 2
A3H	Reserved
A4H	XFDL Test Register 0
A5H	XFDL Test Register 1

A6H	XBOC Test Register 0
A7H	XBOC Test Register 1
A8H	SPLR Test Register 0
A9H	SPLR Test Register 1
AAH	SPLR Test Register 2
ABH	Reserved
ACH	SPLT Test Register 0
ADH	SPLT Test Register 1
AEH	SPLT Test Register 2
AFH	SPLT Test Register 3
B0H	CPPM Test Register 0
B1H	CPPM Test Register 1
B2H	CPPM Test Register 2
B3H-BFH	Reserved
C0H	RXCP Test Register 0
C1H	RXCP Test Register 1
C2H	RXCP Test Register 2
C3H	RXCP Test Register 3
C4H-D7H	Reserved
D8H	TXCP Test Register 0
D9H	TXCP Test Register 1
DAH	TXCP Test Register 2
DBH-DFH	Reserved
E0H	E3 FRMR Test Register 0
E1H	E3 FRMR Test Register 1
E2H	E3 FRMR Test Register 2
E3H-E7H	Reserved
E8H	E3 TRAN Test Register 0
E9H	E3 TRAN Test Register 1
EAH	E3 TRAN Test Register 2
EBH	Reserved
ECH	TTB Test Register 0
EDH	TTB Test Register 1
EEH	TTB Test Register 2
EFH-FFH	Reserved

Notes on Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused bits should be masked off by software when read.

2. Writeable register bits are not initialized upon reset unless otherwise noted.

Address 80H Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-PDH test features. All bits, except PMCTST, are reset to zero by a reset of the S/UNI-PDH.

HIZIO,HIZDATA:
The HIZIO and HIZDATA bits control the tristate modes of the S/UNI-PDH. While the HIZIO bit is a logic 1, all output pins of the S/UNI-PDH except the data bus are held in a high-impedance state. The microprocessor interface remains active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

IOTST:
The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the S/UNI-PDH for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

DBCTRL:
The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. The DBCTRL bit only has effect when if the IOTST or PMCTST bit is a logic 1. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-PDH to drive the data bus while holding the CSB pin low tristates the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:
The PMCTST bit is used to configure the S/UNI-PDH for PMC's manufacturing

tests. When PMCTST is set to logic 1, the S/UNI-PDH microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB to logic 1.

11.1 Test Mode 0

In test mode 0, the S/UNI-PDH allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the IOTST bit in the Master Test Register is set to logic 1 and the following addresses must be written with 00H: 87H, 89H, 8DH, 91H, A1H, A5H, A7H, A9H, ADH, B1H, C1H and D9H. Also, to enable input and output signals to propagate through the Interface blocks, the value 20H must be written to address 00H, the value 40H must be written to address 01H, and the value 00H must be written to addresses 03H through 05H.

84 PIN PLCC

Reading the following address locations returns the values for the indicated inputs. Note, for inputs RNEG/ROHM and RPOS/RDAT, input RCLK must transition high twice before reads.

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
88H						RNEG /ROHM	RPOS /RDAT	RCLK	
A2H							TOH	TOHINS	1
ACH	TSOC	TIOHM	TICLK	TPOH	TPOHINS				
AEH	FWDATA7	FWDATA6	FWDATA5	FWDATA4	FWDATA3	FWDATA2	FWDATA1	FWDATA0	
AFH								C13/CADD	
C3H								FRDB	
D8H							FWRB		2

Note 1: TOHINS must be logic 1 to observe changes on TOH.

Note 2: FIFOBP bit in register address 00H must be logic 0 to observe FWRB.

Writing the following address locations followed by a high transition on input RCLK forces the outputs to the value in the corresponding bit position:

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
8AH			ROH					ROHCLK	
8BH				ROHFP					
A0H					TPOS /TDAT	TNEG /TOHM		TCLK	1
A2H							TOHFP	TOHCLK	
A8H		FRDATA	RFIFOE /FRCLK	RSOC	RPOHCLK	RPOH	RPOHFP	REOC /OOF	2
AAH	REOH /LOF								
ACH					TFIFOFB /FWCLK	TPOHFP	TPOHCLK		
C0H				RCELL					3
D8H							TCEL	INTB	3

Note 1: TCLK bit must be toggled high to place data on TPOS/TDAT and TNEG/TOHM outputs.

Note 2: The content of the FRDATA bit is shifted into FRDATA[7:0] output and all the bits of FRDATA[7:0] output are shifted by 1 bit position towards the high order bits on the falling edge of a clock derived from RCLK/2. FRDATA[7] is shifted out and discarded. Bit 7 of A8H must be set to logic 0 to enable the shift register clock.

Note 3: FIFOBP bit in register address 00H must be logic 0 to enable RCELL and TCELL to be output.

Note 4: A logic 0 must be written in Bit 0 of Register D8H in order to force INTB to a TTL high. A logic 1 must be written to force it to TTL low.

100 PIN PQFP

Reading the following address locations returns the values for the indicated inputs. Note, for inputs RNEG/ROHM and RPOS/RDAT, input RCLK must transition high twice before reads.

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
81H						DATA_HZ	CNTL_HZ	TSEN	1,2
88H						RNEG /ROHM	RPOS /RDAT	RCLK	
A2H	TDLSIG						TOH	TOHINS	3,4
ACH	TSOC	TIOHM	TICLK	TPOH	TPOHINS				
AEH	FWDATA7	FWDATA6	FWDATA5	FWDATA4	FWDATA3	FWDATA2	FWDATA1	FWDATA0	
AFH								C13/CADD	
C3H								FRDB	
D8H							FWRB		5
DAH								TWRENB	

Note 1: DATA_HZ and CNTL_HZ are not external input signals. They are internal signals whose states can be read through this test register to facilitate device testability and characterization.

Note 2: During IOTST, input TSEN can only be monitored. Internally, TSEN is effectively forced to logic 0. This deactivates the tristatability of FRDATA [7:0], RXPRTY, REOC, REOH and RSOC.

Note 3: TNETOP bit in register address 05H must be logic 1 to observe TDLSIG.

Note 4: TOHINS must be logic 1 to observe changes on TOH.

Note 5: FIFOBP bit in register address 00H must be logic 0 to observe FWRB.

Writing the following address locations followed by a high transition on input RCLK forces the outputs to the value in the corresponding bit position:

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
8AH			ROH					ROHCLK	
8BH				ROHFP			RDLCLK	RDLSIG	
A0H					TPOS /TDAT	TNEG /TOHM		TCLK	1
A2H							TOHFP	TOHCLK	
A8H		FRDATA	RFIFOE /FRCLK	RSOC	RPOHCLK	RPOH	RPOHFP	REOC /OOF	2
AAH	REOH /LOF								
ACH					TFIFOFB /FWCLK	TPOHFP	TPOHCLK		
C0H				RCELL					3
C3H		LCD							
D8H							TCELL	INTB	3

Note 1: TCLK bit must be toggled high to place data on TPOS/TDAT and TNEG/TOHM outputs.

Note 2: The content of the FRDATA bit is shifted into FRDATA[7:0] output and all the bits of FRDATA[7:0] output are shifted by 1 bit position towards the high order bits on the falling edge of a clock derived from RCLK/2. FRDATA[7] is shifted out and discarded. Bit 7 of A8H must be set to logic 0 to enable the shift register clock.

Note 3: FIFOBP bit in register address 00H must be logic 0 to enable RCELL and TCELL to be output.

Note 4: A logic 0 must be written in Bit 0 of Register D8H in order to force INTB to a TTL high. A logic 1 must be written to force it to TTL low.

12 OPERATION

12.1 PLCP Frame Formats

The S/UNI-PDH provides support for four different PLCP frame formats: the DS3 PLCP format, the DS1 frame format, the G.751 E3 frame format, and the E1 frame format. The structure of each of these formats is quite similar, and is illustrated in figures 5 to 8.

Figure 5 - DS3 PLCP Frame Format

A1	A2	P11	Z6	ATM Cell	
A1	A2	P10	Z5	ATM Cell	
A1	A2	P9	Z4	ATM Cell	
A1	A2	P8	Z3	ATM Cell	
A1	A2	P7	Z2	ATM Cell	PLCP Frame Rate 125 µsec
A1	A2	P6	Z1	ATM Cell	
A1	A2	P5	F1	ATM Cell	
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	Trailer
Framing (3 octets)			POH	53 octets	13 or 14 nibbles

The DS3 PLCP frame provides the transmission of 12 ATM cells every 125 µs. The PLCP frame is nibble aligned to the overhead bits in the DS3 frame; however, there is no relationship between the start of the PLCP frame and the start of the DS3 M-frame. A trailer is inserted at the end of each PLCP frame. The number of nibbles inserted (13 or 14) is varied continuously such that the resulting PLCP frame rate can be locked to an 8 kHz reference.

Figure 6 - DS1 PLCP Frame Format

A1	A2	P9	Z4	ATM Cell	PLCP Frame Rate 3 ms
A1	A2	P8	Z3	ATM Cell	
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	
A1	A2	P5	F1	ATM Cell	
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	Trailer
Framing (3 octets)			POH	53 octets	6 octets

The DS1 PLCP frame provides the transmission of 10 ATM cells every 3 ms. The PLCP frame is octet aligned to the framing bit in the DS1 frame; there is no relationship between the start of the PLCP frame, and the start of the DS1 frame. A trailer is inserted at the end of each PLCP frame. The number of octets inserted is always six, and cannot be varied.

Figure 7 - G.751 E3 PLCP Frame Format

A1	A2	P8	Z3	ATM Cell	PLCP Frame Rate 125 µsec
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	
A1	A2	P5	F1	ATM Cell	
A1	A2	P4	B1	ATM Cell	
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	Trailer
Framing (3 octets)			POH	53 octets	17,18,19,20, or 21 octets

The G.751 E3 PLCP frame provides the transmission of 9 ATM cells every 125 µs. The PLCP frame is octet aligned to the 16 overhead bits in the ITU-T Recommendation G.751 E3 frame; there is no relationship between the start of the PLCP frame, and the start of the E3 frame. A trailer is inserted at the end of each PLCP frame. The number of octets inserted is nominally 18, 19, or 20, and is based

on the number of E3 overhead octets (4, 5, or 6) that have been inserted during the PLCP frame period. The nominal octet stuffing can be varied by ±1 octet to allow the E3 PLCP frame to be locked to an external 8 kHz reference. Thus the trailer can be 17, 18, 19, 20, or 21 octets in length.

Figure 8 - E1 PLCP Frame Format

A1	A2	P9	Z4	ATM Cell	
A1	A2	P8	Z3	ATM Cell	
A1	A2	P7	Z2	ATM Cell	
A1	A2	P6	Z1	ATM Cell	PLCP
A1	A2	P5	F1	ATM Cell	Frame Rate
A1	A2	P4	B1	ATM Cell	2.375 ms
A1	A2	P3	G1	ATM Cell	
A1	A2	P2	M2	ATM Cell	
A1	A2	P1	M1	ATM Cell	
A1	A2	P0	C1	ATM Cell	
Framing (3 octets)			POH	53 octets	

The E1 PLCP frame provides the transmission of 10 ATM cells every 2.375 ms. Thirty of the thirty-two available E1 channels are used for transporting the PLCP frame. The remaining two channels are reserved for E1 framing and signalling functions. The PLCP frame is octet aligned to the channel boundaries in the E1 frame. The PLCP frame is aligned to the 125 µs E1 frame (the A1 octet of the first row of the PLCP frame is inserted in timeslot 1 of the E1 frame).

12.2 PLCP Path Overhead Octet Processing

- **A1,A2 : Frame Alignment Pattern**

  Transmit: The S/UNI-PDH inserts the PLCP frame alignment pattern (F628H).

  Receive: The S/UNI-PDH searches the receive stream for the PLCP frame alignment pattern. When the pattern has been detected for two consecutive rows, along with two valid, and sequential path overhead identifier octets, the S/UNI-PDH declares in-frame. Note that the ATM cell boundaries are implicitly known when the PLCP frame is located, thus cell delineation is accomplished by locating the PLCP frame. When errors are detected in both octets in a single row, or when errors are detected in two consecutive path overhead identifier octets, the S/UNI-PDH declares an out-of-frame

defect. The loss-of-frame defect is an integrated version of the out-of-frame defect state.

- **P0-P11 : Path Overhead Identifier**

  Transmit: The S/UNI-PDH inserts the path overhead identifier codes in accordance with the PLCP frame alignment. The twelve unique code values are:

POI	POI Code (Hex)
P11	2C
P10	29
P9	25
P8	20
P7	1C
P6	19
P5	15
P4	10
P3	0D
P2	08
P1	04
P0	01

  Receive: The S/UNI-PDH identifies the PLCP path overhead bytes by monitoring the sequence of the POI bytes.

- **Z1-Z6 : Growth**

  Transmit: These octets are unused in the S/UNI-PDH and are nominally programmed with all zeros. Access to these octets is provided by the PLCP transmit overhead access port (TPOH).

  Receive: These octets are ignored by the S/UNI-PDH, and are extracted on the PLCP receive overhead access port (RPOH).

- **F1 : User Channel**

  Transmit: This octet is unused in the S/UNI-PDH. The value inserted in this octet is controlled by the SPLT F1 Octet Register, or by the PLCP transmit overhead access port (TPOH).

  Receive: This octet is ignored by the S/UNI-PDH, and is extracted on the PLCP receive overhead access port (RPOH).

- **B1 : Bit Interleaved Parity**

  Transmit: This octet contains an 8-bit interleaved parity (BIP) calculated across the entire PLCP frame (excluding the A1, A2, and Pn octets and the trailer). The B1 value is calculated based on even parity,

and the value inserted in the current frame is the BIP result calculated for the previous frame.

Receive: The bit interleaved parity is calculated for the current frame and stored. The B1 octet contained in the subsequent frame is extracted, and compared to the calculated value. Differences between the two values provide an indication of the end-to-end bit error rate. These differences are accumulated in the CPPM B1 Error Count Registers.

- **G1 : Path Status**

Transmit: The first four bit positions provide a PLCP far end block error function, and indicate the number of B1 errors detected at the near end. The FEBE field has nine legal values (0000 - 1000) indicating between zero and eight B1 errors.

The fifth bit position is used to transmit PLCP yellow alarm. The last three bit positions provide the link status signal used in IEEE-802.6 DQDB implementations. Yellow alarm and link status signal insertion is controlled by the SPLT Diagnostics and G1 Octet Register, or by the PLCP transmit overhead access port (TPOH).

Receive: The G1 byte provides the PLCP FEBE function as described above. The FEBE value is accumulated in the CPPM FEBE Count Registers. PLCP yellow alarm is detected/removed when the yellow bit is set to logic 1/zero for ten consecutive frames. The yellow alarm state, and the link status signal state are contained in the SPLR Status Register.

- **M1, M2 : Control Information**

Transmit: These octets carry the DQDB layer management information. The M1 and M2 bytes can be ignored as they are defined as "Unassigned - Receiver required to ignore" in the ATM Forum DS3 UNI 3.0 specification. The value inserted in these octets is determined by:

  - The M1TYPE and M2TYPE bits in the SPLT Configuration Register (Register 2CH).
  - The SRCM1 and SRCM2 bits in the SPLT Control Register (Register 2DH).
  - The TPOH, TPOHFP, and TPOHINS input pins.

Receive: These octets are ignored by the S/UNI-PDH, and are extracted on the PLCP receive overhead access port (RPOH).

- **C1 : Cycle/Stuff Counter**

  Transmit: The coding of this octet depends on the PLCP frame format. For DS1 and E1 PLCP formats, this octet is programmed with all zeros.

  For the DS3 PLCP format, this octet indicates the number of stuff nibbles (13 or 14) at the end of each PLCP frame. The C1 value is varied in a three frame cycle where the first frame always contains 13 stuff nibbles, the second frame always contains 14 nibbles, and the third frame contains 13 or 14 nibbles as illustrated below.

C1(Hex)	Frame/Trailer Length
FF	1 (13 Nibbles)
00	2 (14 Nibbles)
66	3 (13 Nibbles)
99	3 (14 Nibbles)

  The nibble stuffing in the third frame is varied so that the PLCP frame rate can be locked to an external 8 kHz timing reference. The S/UNI-PDH supports three timing modes: 1) loop timing using the LOOPT bit in the S/UNI-PDH Configuration Register, 2) external timing using the C13/CADD input, and 3) fixed timing using the FIXSTUFF bit in the SPLT Configuration Register.

  For the G.751 E3 PLCP format, this octet indicates the number of stuff octets (17 - 21) at the end of each PLCP frame. Depending on the alignment of the G.751 E3 frame to the E3 PLCP frame, 18, 19, or 20 octets are nominally stuffed. The stuffing may be varied by ±1 octet so that the PLCP frame rate can be locked to an external 8 kHz timing reference. The C1 octet coding is illustrated below:

C1(Hex)	Trailer Length
3B	17 octets
4F	18 octets
75	19 octets
9D	20 octets
A7	21 octets

  The S/UNI-PDH supports two timing modes: 1) external timing

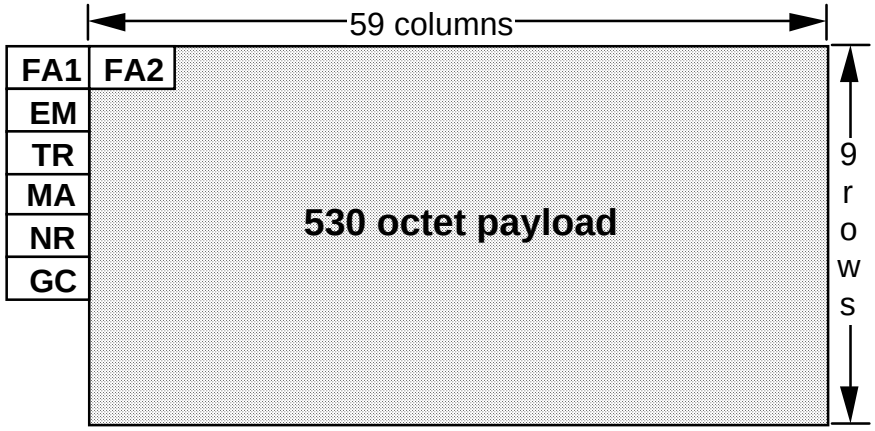
using the C13/CADD input, and 2) fixed timing using the FIXSTUFF bit in the SPLT Configuration Register.

Receive: The S/UNI-PDH interprets the trailer nibble length according to the selected PLCP frame format, and the received C1 code.

12.3 G.832 E3 Frame Format

The S/UNI-PDH provides support for the newly defined G.832 E3 frame format. This format allows direct byte mapping of ATM cells as specified in G.804. The G.832 E3 frame format is shown in figure 9.

Figure 9 - G.832 E3 Frame Structure



12.4 G.832 E3 Path Overhead Octet Processing

- **FA1,FA2 : Frame Alignment Pattern**

  Transmit: The S/UNI-PDH inserts the G.832 E3 frame alignment pattern (F628H).

  Receive: The S/UNI-PDH searches the receive stream for the G.832 E3 frame alignment pattern. When the pattern has been detected for three consecutive frames, the S/UNI-PDH declares in-frame. Note that there is no ATM cell alignment with the G.832 E3 frame, thus cell delineation must be accomplished to locate the ATM cells. When errors are detected in either framing octets for four consecutive frames, the S/UNI-PDH declares an out-of-frame defect.

- **EM : Error Monitoring, BIP-8**

Transmit: The S/UNI-PDH inserts the calculated BIP-8 by computing even parity over all transmit bits, including the overhead bits, of the previous 125µs frame.

Receive: The S/UNI-PDH computes the incoming BIP-8 value over one 125µs frame. The result is held and compared to the value contained in the EM byte of the subsequent frame. Any detected errors are accumulated.

- **TR : Trail Trace**

  Transmit: The S/UNI-PDH inserts the 16-byte trail access point identifier programmed into the TTB registers.

  Receive: The S/UNI-PDH extracts the repetitive trail access point identifier and validates it for consistency (i.e., the same pattern is being received). The S/UNI-PDH also compares the received pattern to an expected pattern programmed into the TTB registers. This allows the S/UNI-PDH to verify its continued connection to the intended transmitter. Note that the S/UNI-PDH does not compute or check the CRC-7 over the 16-byte trace message.

- **MA : Maintenance and Adaptation Byte**

  Transmit: The S/UNI-PDH inserts the FERF, FEBE, Payload Type bits, Tributary Unit Multiframe Indicator bits, and the Timing Marker bit as programmed in the E3 TRAN registers or as indicated by detection of receive OOF or BIP-8 errors.

  Receive: The S/UNI-PDH extracts and reports the FERF bit value when it has been the same for 3 or 5 consecutive frames. S/UNI-PDH also extracts and accumulates FEBE occurrences, and extracts the Payload Type, Tributary Unit Multiframe, and Timing Marker indicator bits and reports them through microprocessor accessible registers. The Maintenance and Adaptation byte is also extracted and output on the ROH.

- **NR : Network Operator Byte**

  Transmit: The S/UNI-PDH inserts the Network Operator byte from the TOH overhead stream or, optionally, from the XFDL or the TDLSIG input. When not configured for Tandem Connection Maintenance, all 8 bits of the Network Operator byte are inserted from TOH or from XFDL/TDLSIG input. When configured for Tandem Connection, zeros are inserted into the first four bits of the byte and the last four bits of the byte are inserted from TOH or from XFDL/ TDLSIG input.

  Receive: The S/UNI-PDH extracts the Network Operator byte and outputs it on ROH or, optionally, terminates it in RFDL or outputs it on

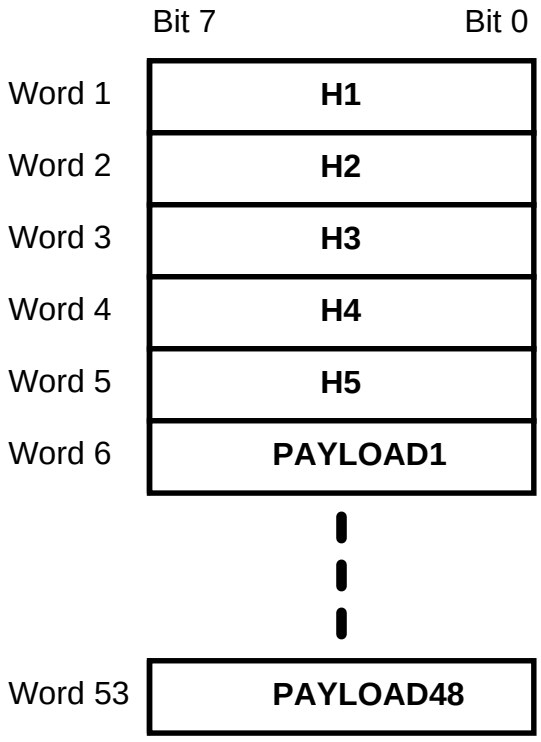
RDLSIG. When not configured for Tandem Connection Maintenance, all 8 bits of the Network Operator byte are extracted and presented on ROH, RDLSIG, or to RFDL. When configured for Tandem Connection, the first four bits of the byte are accumulated by S/UNI-PDH and the last four bits of the byte are output on ROH, RDLSIG, or terminated by RFDL.

- **GC : General Purpose Communication Channel**
  Transmit: The S/UNI-PDH inserts the GC byte from the TOH overhead stream or, optionally, from the XFDL or the TDLSIG input.
  Receive: The S/UNI-PDH extracts the GC byte and outputs it on ROH or, optionally, terminates it in RFDL or outputs it on RDLSIG.

12.5 S/UNI-PDH Cell Data Structure

ATM cells are passed to/from the S/UNI-PDH transmit and receive FIFOs using a 53 word data structure. The data structure is shown in figure 10.

Figure 10 - Cell Data Structure



Fifty-three 8-bit words are contained in this data structure. Bit 7 of each word is the most significant bit and corresponds to the first bit transmitted or received. The start

of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first cell header octet). Word 5 of this structure contains the HCS octet.

A FIFO data path integrity check is provided using Word 5 (HCS octet). The HCK bit in the RXCP Control Register enables the overwriting of the receive HCS octet position in the cell data structure with an alternating AAH/55H pattern (or, optionally, with a fixed 55H pattern). The receive data path between the S/UNI-PDH and the external ATM layer processing device is monitored by checking the HCS octet position for the AAH/55H (or fixed 55H) pattern. Any discrepancy indicates a failure in this datapath. In the transmit direction, the S/UNI-PDH monitors the HCS octet position, and verifies the presence of the alternating AAH/55H (or fixed 55H) pattern. Any discrepancy in this pattern indicates a failure in the transmit data path, and is reported by the HCKI bit in the TXCP Interrupt Enable/Status Register.

In the receive direction, idle/unassigned cells or cell matching the user-programmed header are dropped when the BLOCK bit in the RXCP Control Register is set to a logic 1. Cells containing HCS errors are also dropped while the HCSPASS bit in the RXCP Control Register is set to logic 0. No header status information is passed within this data structure. Error free headers, and headers containing detectable errors are passed while HCSPASS is a logic 1. No cells are passed when the S/UNI-PDH is in the PLCP loss of frame defect state (for PLCP based transmission), or when the S/UNI-PDH is in the out of cell delineation defect state (for non-PLCP based transmission).

In the transmit direction, the HCSINS bit in the TXCP Control Register determines whether the HCS is calculated internally, or is inserted directly from Word 5.

12.6 Using the Performance Monitoring Features

The PMON and CPPM blocks are provided for performance monitoring purposes. The PMON block is used to monitor DS3 performance primitives while the CPPM is used to monitor PLCP and cell-based primitives. The counters in the PMON block have been sized as not to saturate if polled every second. The counters in the CPPM blocks have been sized as not to saturate if polled every 1/2 second at line rates up to 45 MHz.

The DS3 and E3 primitives can be accumulated independently of the PLCP and cell-based primitives. An accumulation interval is initiated by writing to one of the PMON register addresses. After writing to a PMON count register, three RTOHCLK clock periods (<5.7 μs) must be allowed to elapse to permit the PMON counter values to be transferred. The PMON registers may then be read.

PLCP and cell-based primitives are accumulated together with DS3 and E3 primitives. An accumulation interval is initiated by writing to one of the CPPM register addresses. This write transfers both the PMON and CPPM counter values after a maximum of 3 RTOHCLK clock periods (<5.7 µs). The CPPM and PMON registers may then be read.

12.7 Using the Internal Data Link Transmitter

Upon reset of the S/UNI-PDH, the XFDL should be disabled by setting the EN bit in the XFDL Configuration Register to logic 0. If data is not ready to be transmitted, the INTB output should also be masked by setting the INTE bit to logic 0.

When a frame (or frames) of data are ready to be transmitted, the XFDL Configuration Register should be initialized for transmission: if the FCS is desired, the CRC bit should be set to logic 1; if the block is to be used in interrupt driven mode, interrupts should be enabled by setting the INTE bit in the XFDL Configuration Register and the XFDLE bit in the S/UNI-PDH Interrupt Enable Register to logic 1. Finally, the XFDL can be enabled by setting the EN bit to logic 1.

The XFDL can be used in a polled or interrupt driven mode for the transfer of frame data. In the polled mode, the processor controlling the XFDL must periodically read the XFDL Interrupt Status Register to determine when to write to the XFDL Transmit Data Register. In the interrupt driven mode, the processor controlling the XFDL uses the INTB output, and the interrupt source registers, to determine when to write to the XFDL Transmit Data Register.

If the XFDL data transfer is operating in the polled mode, then a timer periodically starts up a service routine, which should process data as follows:

1) Read the XFDL Interrupt Status Register and check the UDR and INTR bits.

2) If UDR=1, then clear the XFDL Interrupt Status Register, set the UDR bit in the XFDL Configuration Register to logic 0, and restart the current frame.

3) If INTR=1, then:

   a) If there is still data to send, then write the next data byte to the XFDL Transmit Data Register;
   b) If all bytes in the frame have been sent, then set the EOM bit in the XFDL Configuration Register to logic 1, and set the INTE bit to logic 0.

4) Read the XFDL Interrupt Status Register and check the UDR bit.

5) If UDR=1, then clear the XFDL Interrupt Status Register, clear the UDR bit in the XFDL Configuration Register to logic 0. Restart the current frame.

In the case of interrupt driven data transfer, the INTB output of the S/UNI-PDH is connected to the interrupt input of the processor, and the interrupt service routine should process the data exactly as described above for the polled mode.

12.8 Using the Internal Data Link Receiver

On power up of the S/UNI-PDH, the RFDL should be disabled by setting the EN bit in the RFDL Configuration Register to logic 0. The RFDL Enable/Status Register should then be initialized to select the FIFO buffer fill level at which an interrupt will be generated. In addition, the RFDLE bit in the S/UNI-PDH Interrupt Enable Register should be set to logic 1.

After the RFDL Enable/Status Register has been written, the RFDL can be enabled at any time by setting the EN bit in the RFDL Configuration Register to logic 1. When the RFDL is enabled, it will assume that the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated (if enabled), and the byte received before the first flag was detected will be written into the FIFO buffer. Because the FLG and EOM bits are passed through the buffer, this dummy write allows the RFDL Status Register to accurately reflect the current state of the data link. An RFDL Status Register read after a RFDL Data Register read of the dummy byte will return EOM as logic 1 and FLG as logic 1. The first interrupt and data byte read after the RFDL is enabled (or TR bit set to logic 1) is an indication of the link status, and the data byte should therefore be discarded. It is up to the controlling processor to keep track of the link state as idle (all ones) or active (flags received).

The RFDL can be used in a polled or interrupt driven mode for the transfer of frame data. In the polled mode, the processor controlling the RFDL must periodically read the RFDL Status Register to determine when to read the RFDL Data Register. In the interrupt driven mode, the processor controlling the RFDL uses either the INTB output, or the main processor INTB output and the interrupt source registers, to determine when to read the RFDL Data Register.

In the case of interrupt driven data transfer from the RFDL to the processor, the INTB output of the S/UNI-PDH is connected to the interrupt input of the processor. The processor interrupt service routine should process the data in the following order:

1) Read the RFDL Data Register.

2) Read the RFDL Status Register to check for, in order, underrun, OVR, FLG, EOM, and FE.

3) If the FIFO has underrun (i.e. the Status Register returns 00H), then discard the last data byte and wait for the next interrupt.

4) If OVR=1, then discard the last frame and wait for the next interrupt.

5) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the last frame, and wait for the next interrupt.

6) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and wait for the next interrupt.

7) Otherwise, save the last data byte read.

8) If EOM=1, then check the CRC, NVB and process the frame.

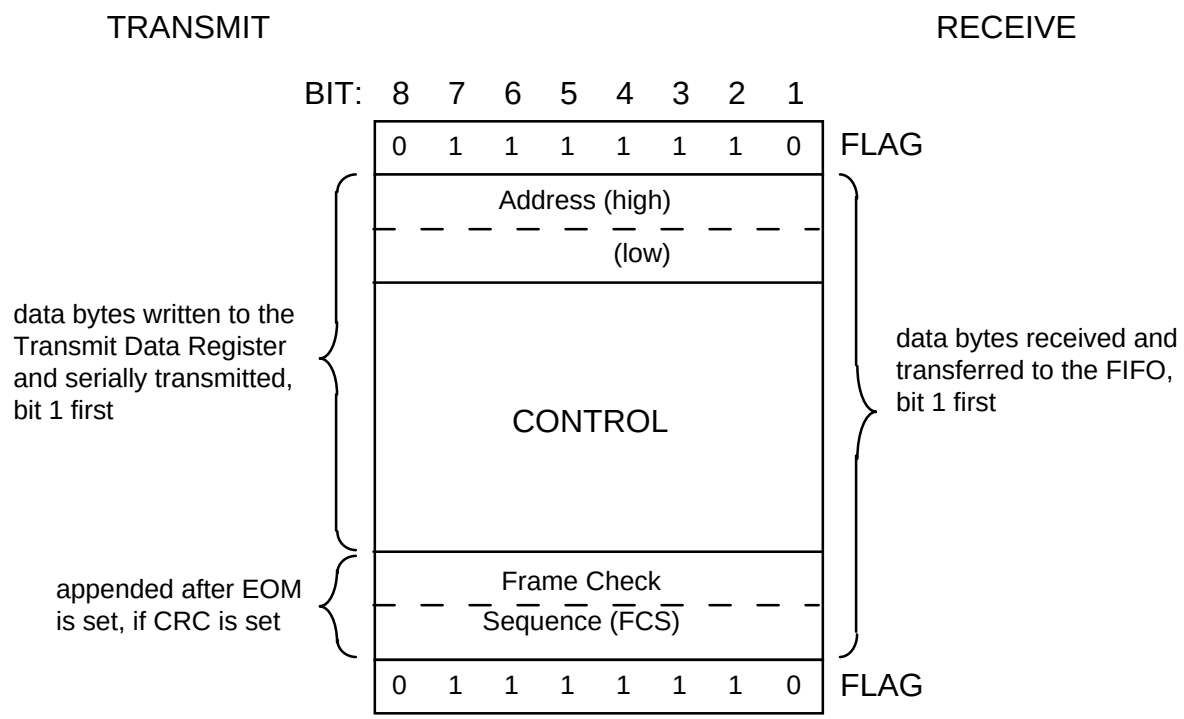
9) If FE=0, then go to step 1, else wait for the next interrupt.

The interrupt service routine can optionally read the RFDL Status Register first to check for an overrun condition, and then for available data, before advancing to step one above.

The link state is typically a local software variable. The link state is inactive if the RFDL is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RFDL is receiving flags or data.

If the RFDL data transfer is operating in the polled mode, then processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt. In the polled mode, the option of reading the RFDL Status Register first should be used to avoid unnecessary reads of the RFDL Data Register.

Figure 11 - Typical Data Frame

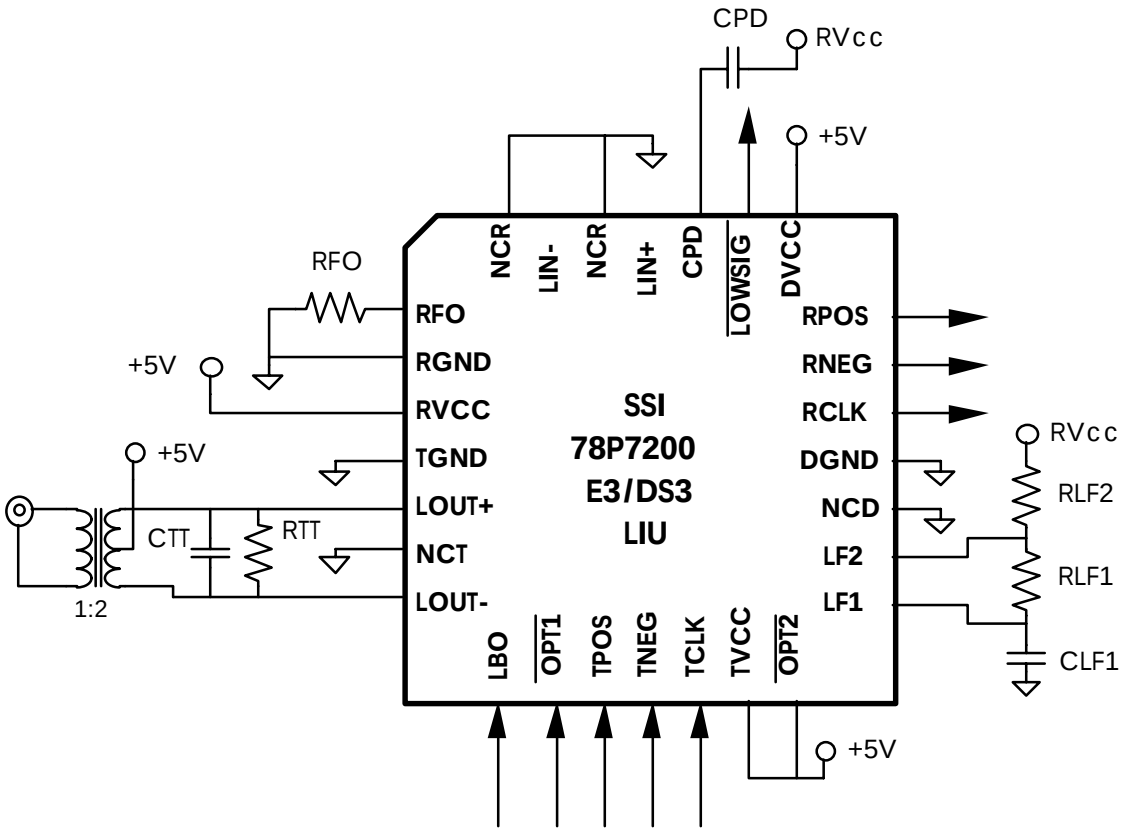


12.9 Silicon Systems 78P7200 Implementation

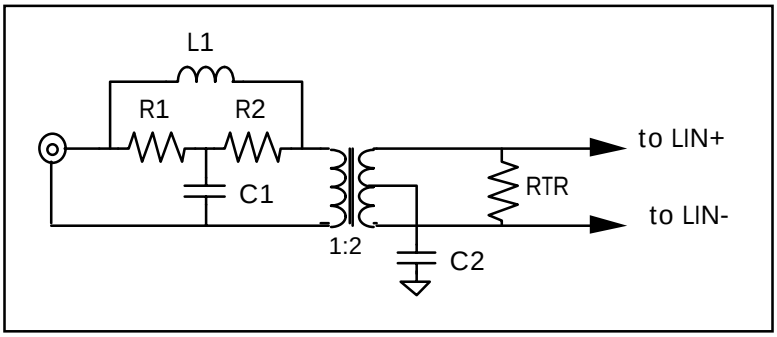
The following diagram and tables show the configuration of the SSI 78P7200 used by PMC-Sierra.[2]

[2] Please contact Silicon Systems at (714) 573-6200 for detailed application information concerning the 78P7200 E3/DS3 LIU.

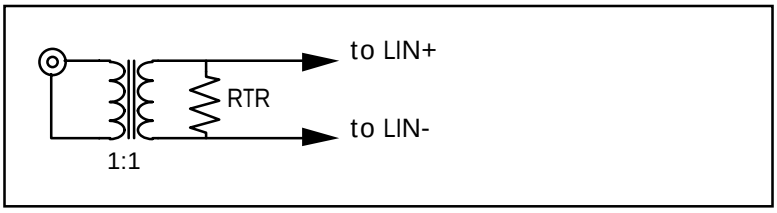
Figure 12 - SSI 78P7200 Configuration



E3 Suggested Input Circuit



DS3 Input Circuit



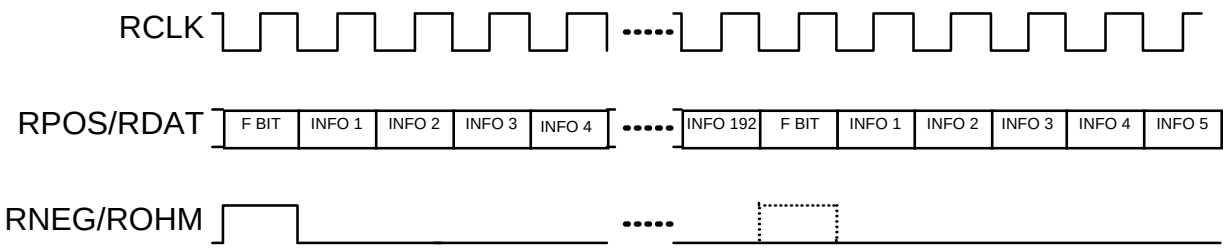
Component	Name	Tolerance	DS3	E3	Unit
Inductor 1	L1	-		0.47	µH
Resistor 1	R1	1%		75	•
Resistor 2	R2	1%		75	•
Capacitor 1	C1	5%		22	pF
Capacitor 2	C2	5%		0.01	µF
Loop filter resistor 1	RLF1	1%	6.04	6.04	k•
Loop filter resistor 2	RLF2	1%	100	100	k•
Loop filter capacitor	CLF1	5%	0.22	0.22	µF
Peak detector capacitor	CPD	10%	0.022	0.022	µF
Loop center frequency resistor	RFO	1%	5.23	6.81	k•
Transmit termination capacitor	CTT	5%	10	3	pF
Transmit termination resistor	RTT	1%	301	604	•
Receive termination resistor	RTR	1%	75	422	•
Receive transformer turns ratio	T1	3%	1:1	1:2	

Condition	LBO	OPT1
E3 all cables	low	low
DS3 cable < 225'	high	high
DS3 cable > 225'	low	high

13 FUNCTIONAL TIMING

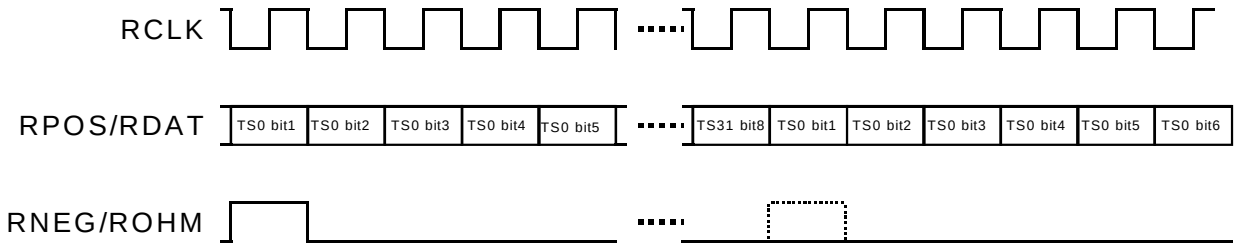
All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the S/UNI-PDH registers are set to their default states).

Figure 13 - Receive DS1 Stream



The Receive DS1 Stream diagram (figure 13) shows the expected DS1 overhead indicators on RNEG/ROHM when the S/UNI-PDH is configured for DS1 PLCP or DS1 non-PLCP frame formats. Once internally synchronized by a pulse on RNEG/ROHM, the S/UNI-PDH can use its internal timeslot counter for DS1 overhead bit identification. Subsequent frame pulses on RNEG/ROHM are not required unless new frame alignment is required. The ATM cell stream is contained in RPOS/RDAT, along with a framing bit placeholder every 193 bit periods. An upstream DS1 framer (such as the PM4341A T1XC) must be used to identify the DS1 framing bit position.

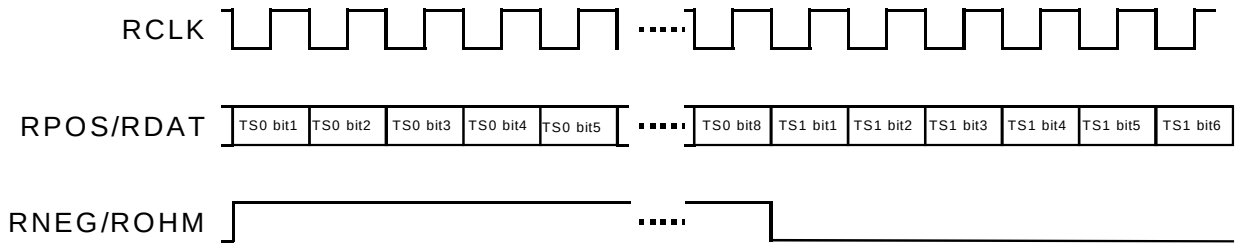
Figure 14 - Receive E1 PLCP Stream



The Receive E1 PLCP Stream diagram (figure 14) shows the expected E1 overhead indicators on RNEG/ROHM when the S/UNI-PDH is configured for E1 PLCP frame format. Once internally synchronized by a pulse on RNEG/ROHM, the S/UNI-PDH can use its internal timeslot counter for E1 overhead bit identification. Subsequent frame pulses on RNEG/ROHM are not required unless new frame alignment is required. The PLCP frame and transmission overhead and ATM cell stream are

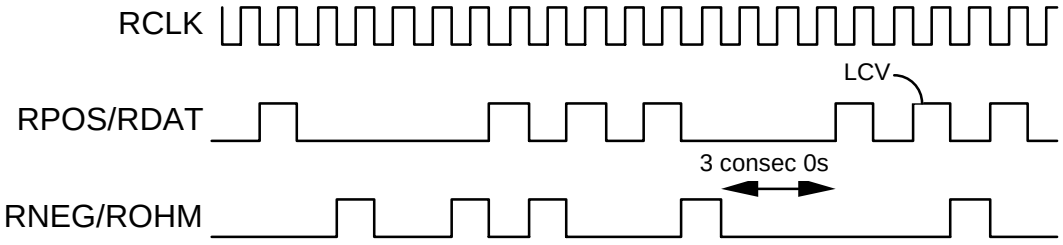
contained in RPOS/RDAT. An upstream E1 framer (such as the PM6341A E1XC) must be used to identify the E1 framing bit position.

Figure 15 - Receive E1 ATM Direct-Mapped Stream



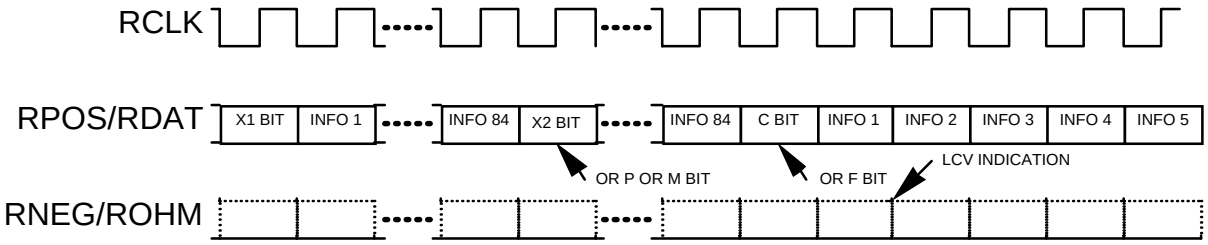
The Receive E1 ATM Direct-Mapped Stream diagram (figure 15) shows the expected E1 overhead indicators on RNEG/ROHM when the S/UNI-PDH is configured for E1 ATM direct-mapped operation. All overhead on timeslots 0 and 16 must be identified on every frame on the RNEG/ROHM input. The ATM cell stream and E1 framing and transmission overhead bits are contained in RPOS/RDAT. An upstream E1 framer (such as the PM6341A E1XC) must be used to identify all E1 overhead bit positions.

Figure 16 - Receive Bipolar DS3 Stream



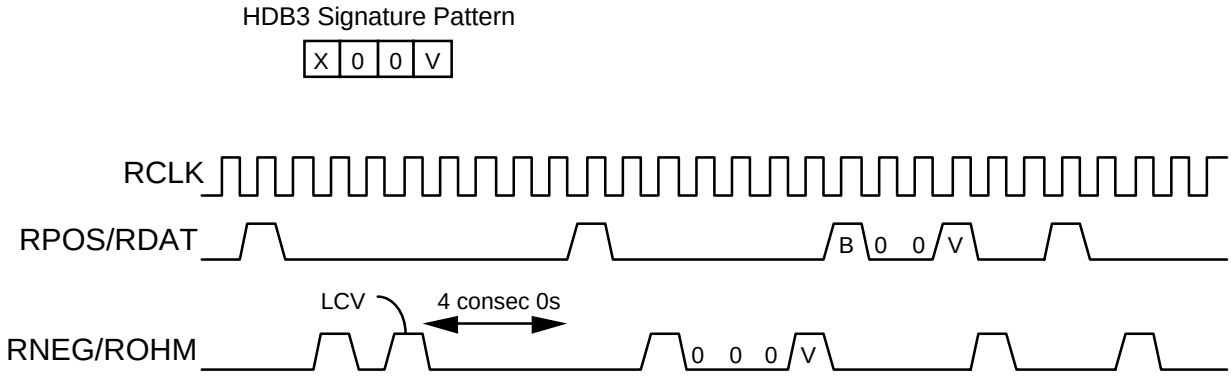
The Receive Bipolar DS3 Stream diagram (figure 16) shows the operation of the S/UNI-PDH while processing a B3ZS encoded DS3 stream on inputs RPOS/RDAT and RNEG/ROHM. It is assumed that the first bipolar violation (on RNEG/ROHM) illustrated corresponds to a valid B3ZS signature. A line code violation is declared upon detection of three consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid B3ZS signature.

Figure 17 - Receive Unipolar DS3 Stream



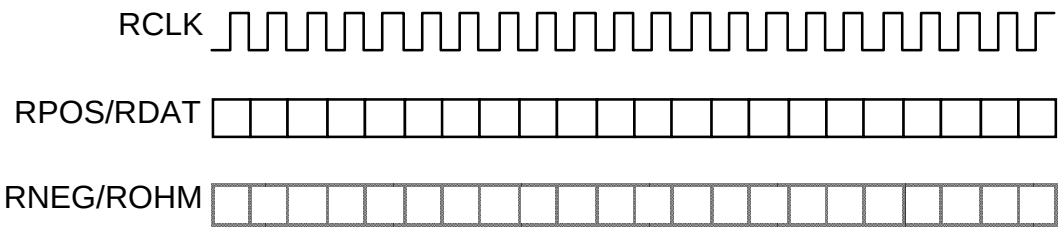
The Receive Unipolar DS3 Stream diagram (figure 17) shows the complete DS3 receive signal on the RPOS/RDAT input. Line code violation indications, detected by an upstream B3ZS decoder, are indicated on input RNEG/ROHM. RNEG/RLCV is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RNEG/ROHM.

Figure 18 - Receive Bipolar E3 Stream



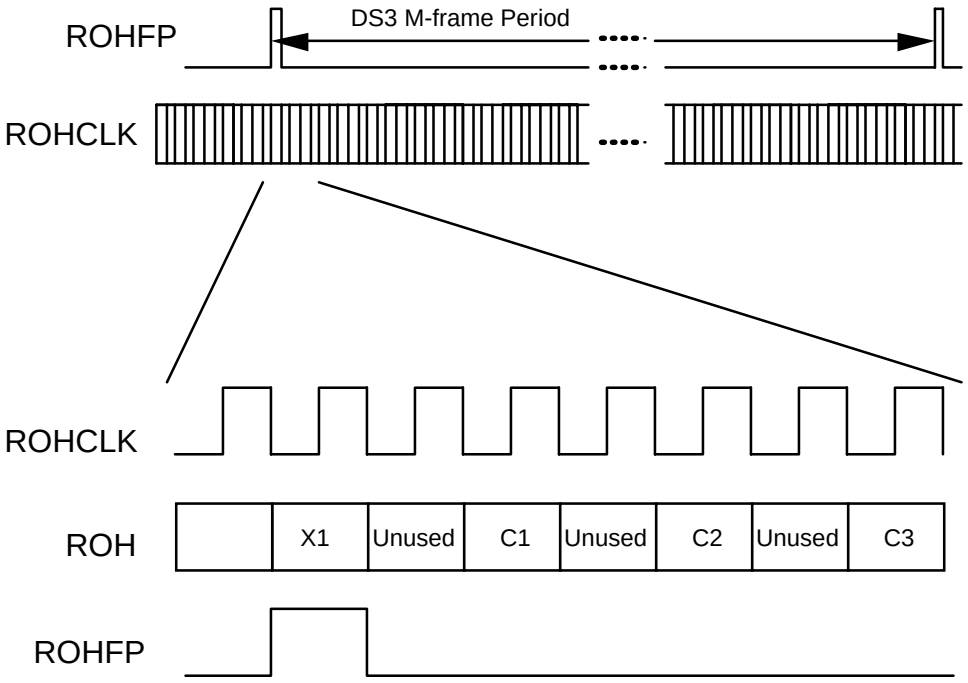
The Receive Bipolar E3 Stream diagram (figure 18) shows the operation of the S/UNI-PDH while processing an HDB3-encoded E3 stream on inputs RPOS/RDAT and RNEG/ROHM. It is assumed that the first bipolar violation (on RNEG/ROHM) illustrated corresponds to a valid HDB3 signature. A line code violation is declared upon detection of four consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid HDB3 signature.

Figure 19 - Receive Unipolar E3 Stream



The Receive Unipolar E3 Stream diagram (figure 19) shows the unipolar E3 receive signal on the RPOS/RDAT input. Line code violation indications, detected by an upstream HDB3 decoder, are indicated on input RNEG/ROHM. RNEG/ROHM is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RNEG/ROHM.

Figure 20 - Receive DS3 Overhead

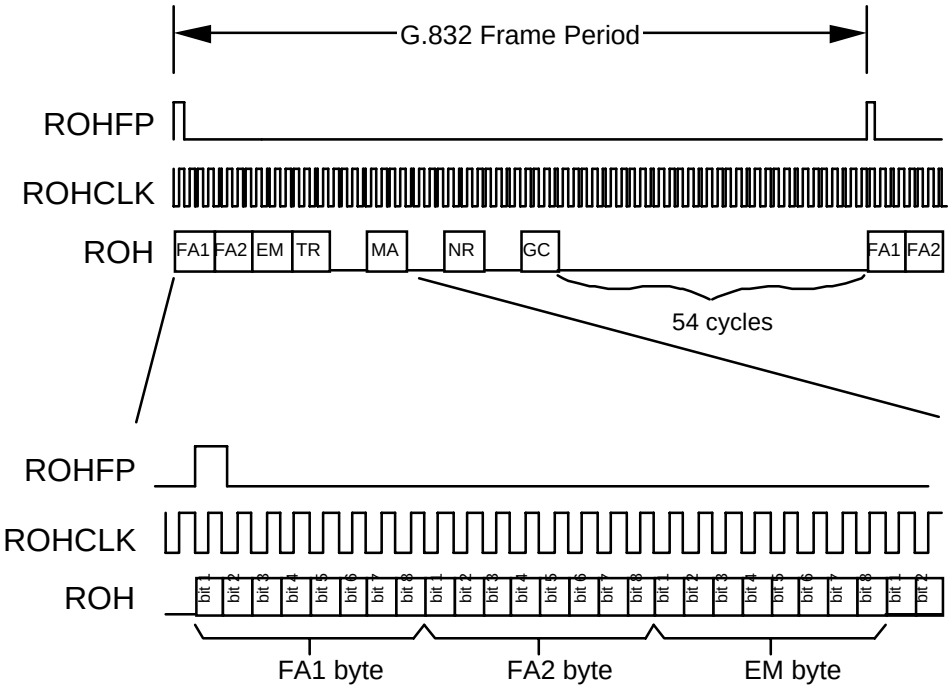


The Receive DS3 Overhead diagram (figure 20) shows the extraction of the DS3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and M-frame position indicator (ROHFP). The DS3 M-frame can be divided into seven M-subframes, with each subframe containing eight overhead bits. The table below illustrates the overhead bit order on ROH:

	DS3 Overhead Bits							
M-subframe	1	2	3	4	5	6	7	8
1	X_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
2	X_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
3	P_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
4	P_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
5	M_1	N/U	C_1	N/U	C_2	N/U	C_3	N/U
6	M_2	N/U	C_1	N/U	C_2	N/U	C_3	N/U
7	M_3	N/U	C_1	N/U	C_2	N/U	C_3	N/U

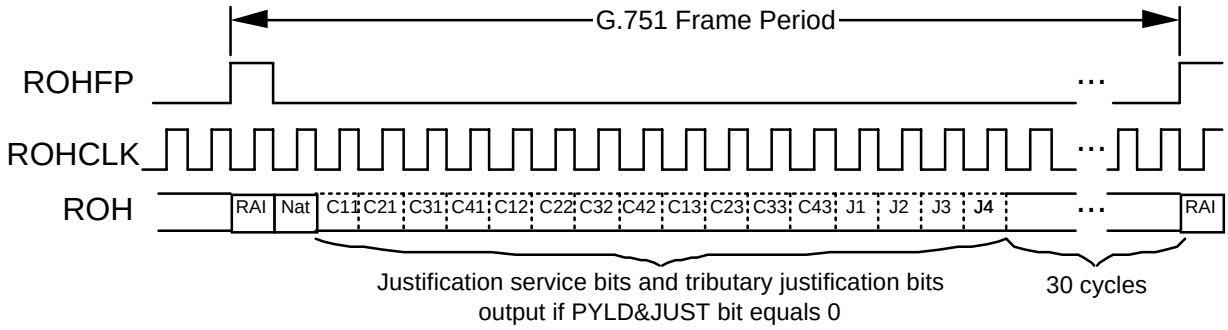
The DS3 framing bits (F-bits) are not extracted on the overhead port. The bit positions corresponding to the F-bits in the extracted stream are marked N/U in the above table. The ROH stream is invalid when the DS3 frame alignment is lost.

Figure 21 - Receive G.832 E3 Overhead



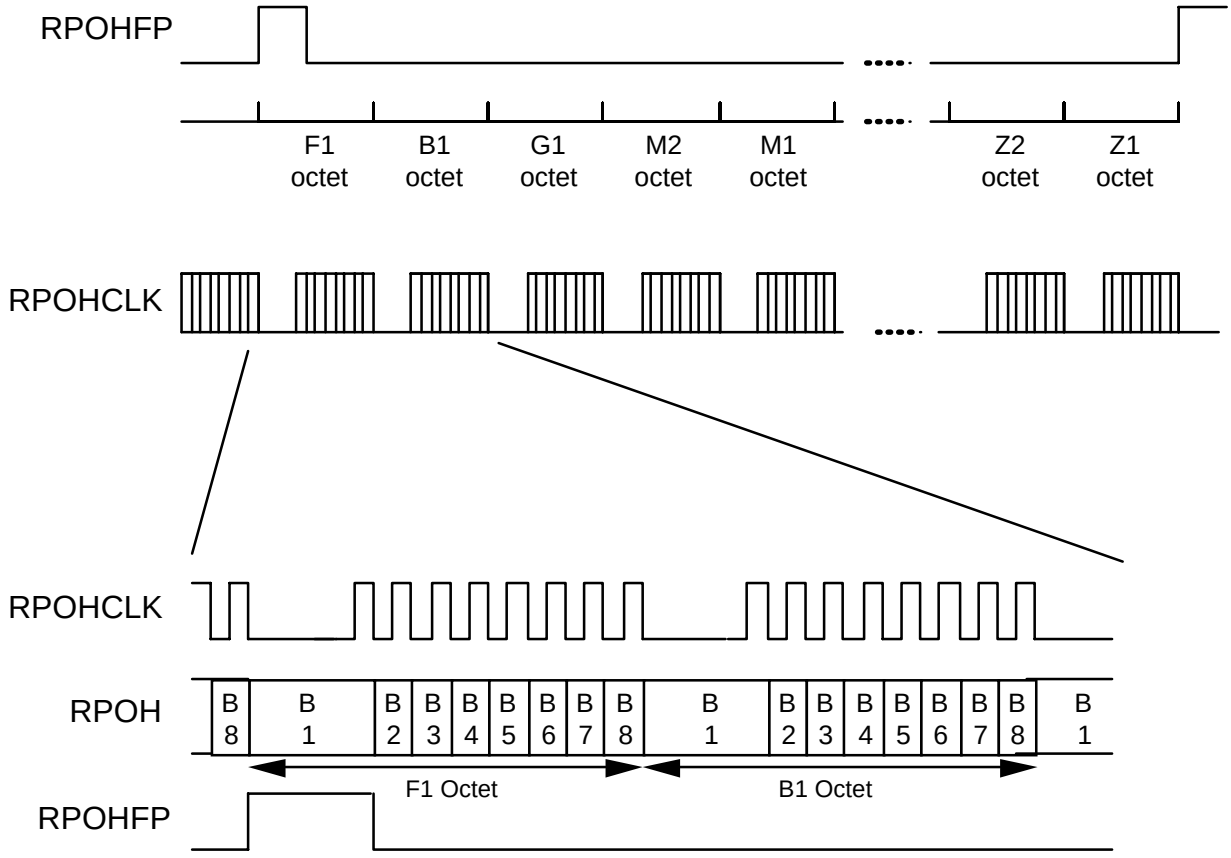
The Receive G.832 E3 Overhead diagram (figure 21) shows the extraction of the G.832 E3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP).

Figure 22 - Receive G.751 E3 Overhead



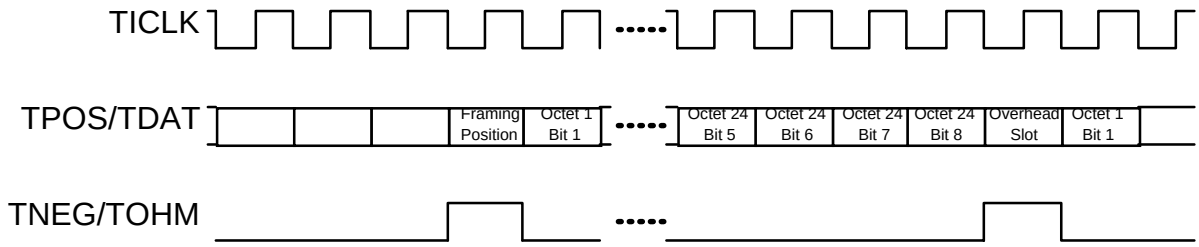
The Receive G.751 E3 Overhead diagram (figure 22) shows the extraction of the G.751 E3 overhead bits on the ROH output, along with overhead clock (ROHCLK), and frame position indicator (ROHFP). The justification indication bits (C_{jk}) along with the justification opportunity bits (J1-J4) are extracted when they are treated as overhead (PYLD&JUST bit in the E3 FRMR Maintenance Options register set to logic 0).

Figure 23 - Receive PLCP Overhead



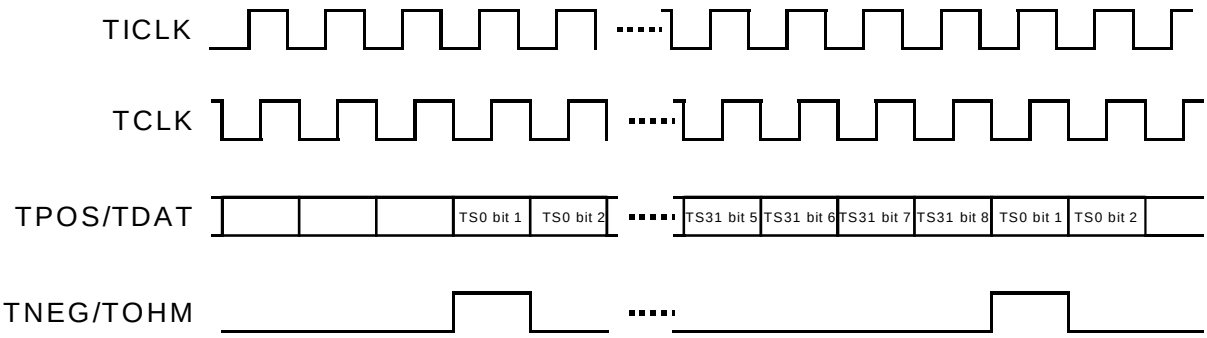
The Receive PLCP Overhead diagram (figure 23) shows the extraction of the PLCP path overhead bits on the RPOH output, along with overhead clock (RPOHCLK), and PLCP frame position indicator (RPOHFP). The path overhead octets are shifted out in order with the most significant bit (bit 1) of each octet first. The number of growth octets (Zn) in the PLCP frame varies according to the selected PLCP frame format (DS3, DS1, G.751 E3, or E1). The PLCP frame position indicator (RPOHFP) is set high once per PLCP frame period, during bit 1 of the F1 octet, and indicates the 8 kHz receive PLCP frame timing.

Figure 24 - Transmit DS1 Stream



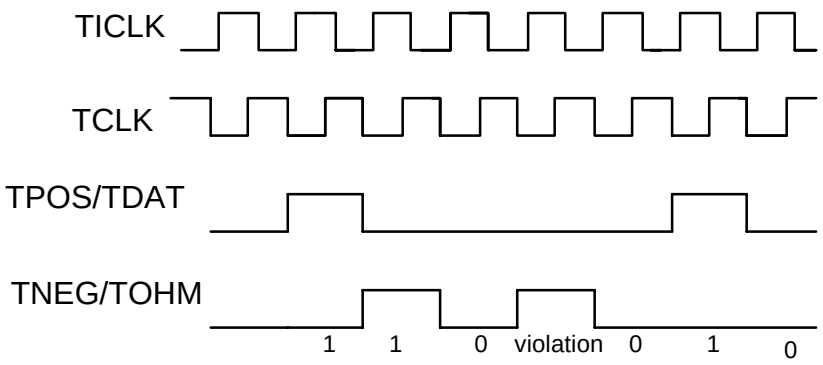
The Transmit DS1 Stream diagram (figure 24) illustrates the generation of DS1 overhead indicators on TNEG/TOHM when the S/UNI-PDH is configured for DS1 PLCP or non-PLCP frame formats. The S/UNI-PDH flywheels using its internal timeslot counter to generate TNEG/TOHM. The ATM cell stream is inserted in TPOS/TDAT, along with a framing bit placeholder every 193 bit periods. An upstream DS1 framer (such as the PM4341A T1XC) must be used to insert the appropriate DS1 framing pattern.

Figure 25 - Transmit E1 Stream



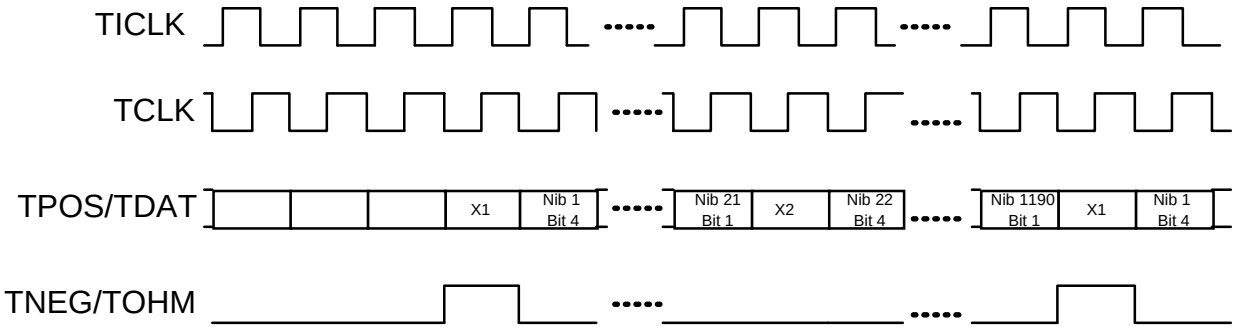
The Transmit E1 Stream diagram (figure 25) illustrates the generation of E1 overhead indicators on TNEG/TOHM when the S/UNI-PDH is configured for E1 PLCP or non-PLCP frame formats. The S/UNI-PDH flywheels using its internal timeslot counter to generate TNEG/TOHM. The ATM cell stream is inserted in TPOS/TDAT, along with a frame alignment indicator bit every 256 bit periods. An upstream E1 framer (such as the PM6341A E1XC) must be used to insert the appropriate E1 framing pattern.

Figure 26 - Transmit Bipolar DS3 Stream



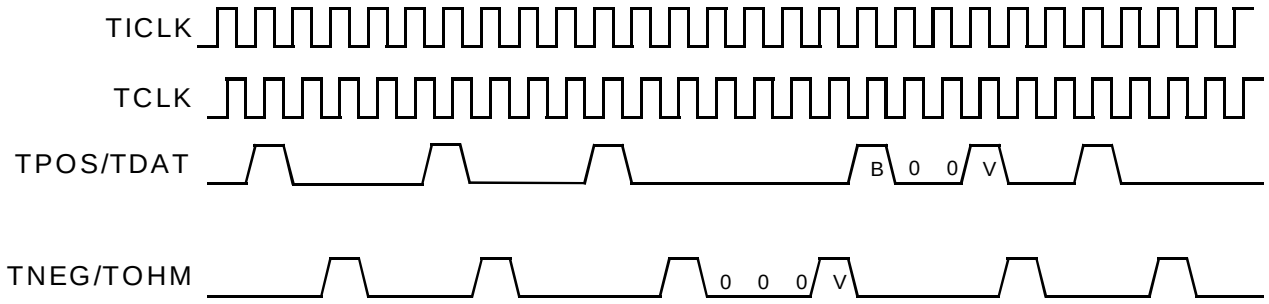
The Transmit Bipolar DS3 Stream diagram (figure 26) illustrates the generation of a bipolar DS3 stream. The B3ZS encoded DS3 stream is present on TPOS/TDAT and TNEG/TOHM. These outputs, along with the transmit clock, TCLK, are directly connected to a DS3 line interface unit. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 27 - Transmit Unipolar DS3 Stream



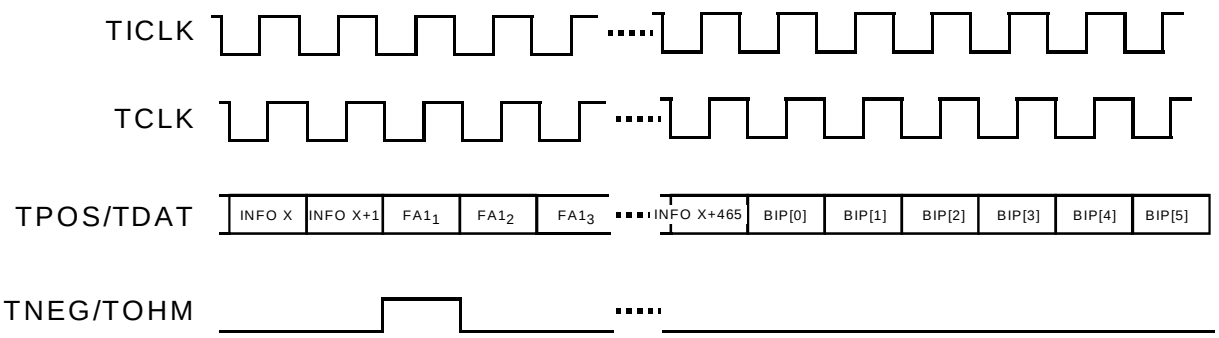
The Transmit Unipolar DS3 Stream diagram (figure 27) illustrates the unipolar DS3 stream generation. The ATM cell stream, along with valid DS3 overhead bits is contained in TPOS/TDAT. The TNEG/TOHM output marks the M-frame boundary (the X1 bit) in the transmit stream. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 28 - Transmit Bipolar E3 Stream



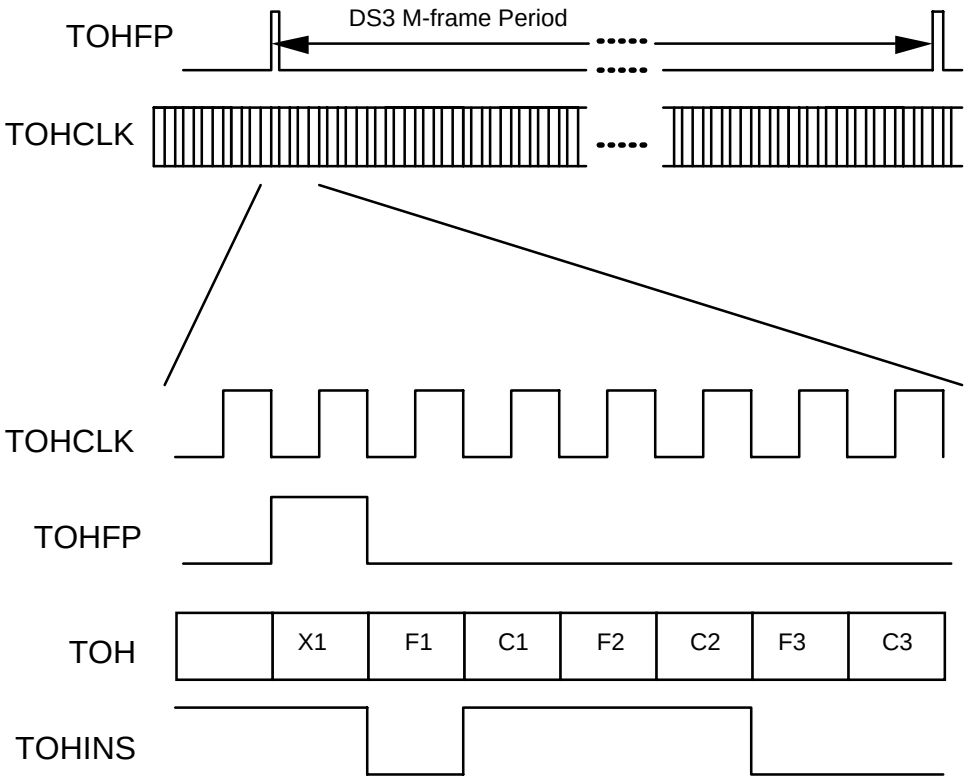
The Transmit Bipolar E3 Stream diagram (figure 28) illustrates the generation of a bipolar E3 stream. The HDB3 encoded E3 stream is present on TPOS/TDAT and TNEG/TOHM. These outputs, along with the transmit clock, TCLK, are directly connected to a E3 line interface unit. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 29 - Transmit Unipolar E3 Stream



The Transmit Unipolar E3 Stream diagram (figure 29) illustrates the unipolar E3 G.832 stream generation. The ATM cell stream, along with valid E3 overhead bits is contained in TPOS/TDAT. The TNEG/TOHM output marks the frame in the transmit stream. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals. The E3 G.751 stream operates in a similar fashion.

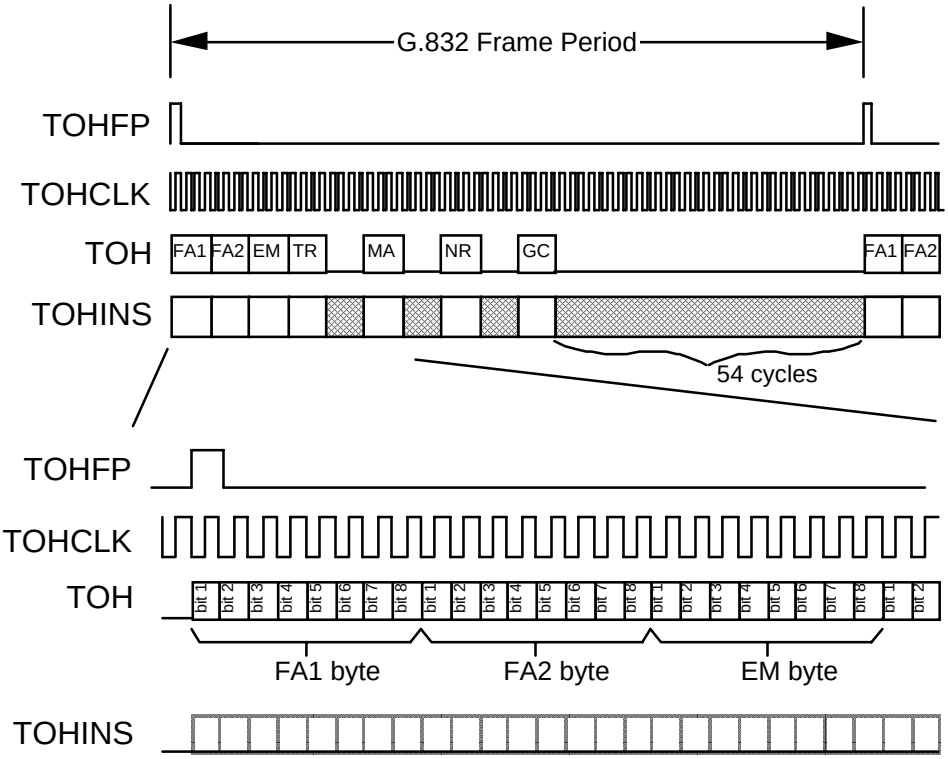
Figure 30 - Transmit DS3 Overhead



The Transmit DS3 Overhead diagram (figure 30) shows the insertion of DS3 overhead bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic 1 once per DS3 M-frame period (during the X1 bit position). In figure 30, the data sampled on TOH during the X1, C1, F2, and C2 bit positions is inserted into the DS3 overhead bits in the transmit stream. The F1, F3, and C3 overhead bits are internally generated by the S/UNI-PDH. The table below illustrates the overhead bit order on TOH:

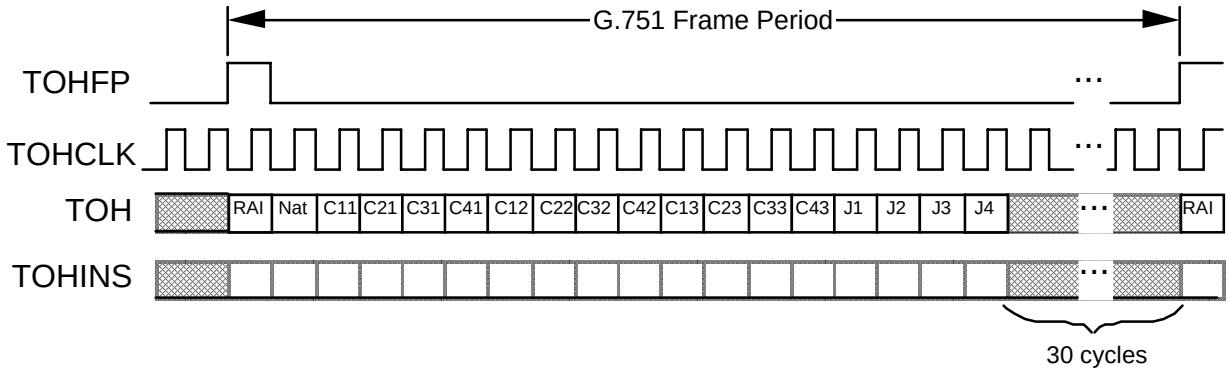
	DS3 Overhead Bits							
M-subframe	1	2	3	4	5	6	7	8
1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	F_4

Figure 31 - Transmit G.832 E3 Overhead



The Transmit G.832 E3 Overhead diagram (figure 31) shows the insertion of G.832 E3 overhead bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic 1 once per G.832 frame period (during the first bit position of the FA1 byte). In figure 31, the bit data sampled on TOH during each byte position while TOHINS is logic 1 is inserted into the G.832 E3 overhead bits in the transmit stream. Note that if an entire byte is to be replaced with data from the TOH stream, TOHINS must be held logic 1 for the duration of that byte position. Also note that the EM byte behaves as an error mask, that is the binary value sampled on TOH in the EM byte location is not inserted directly into the transmit overhead but, rather, the value is XORed with the calculated BIP-8 and inserted in the transmit overhead. Asserting TOHINS during the “gaps” in the TOH stream has no effect.

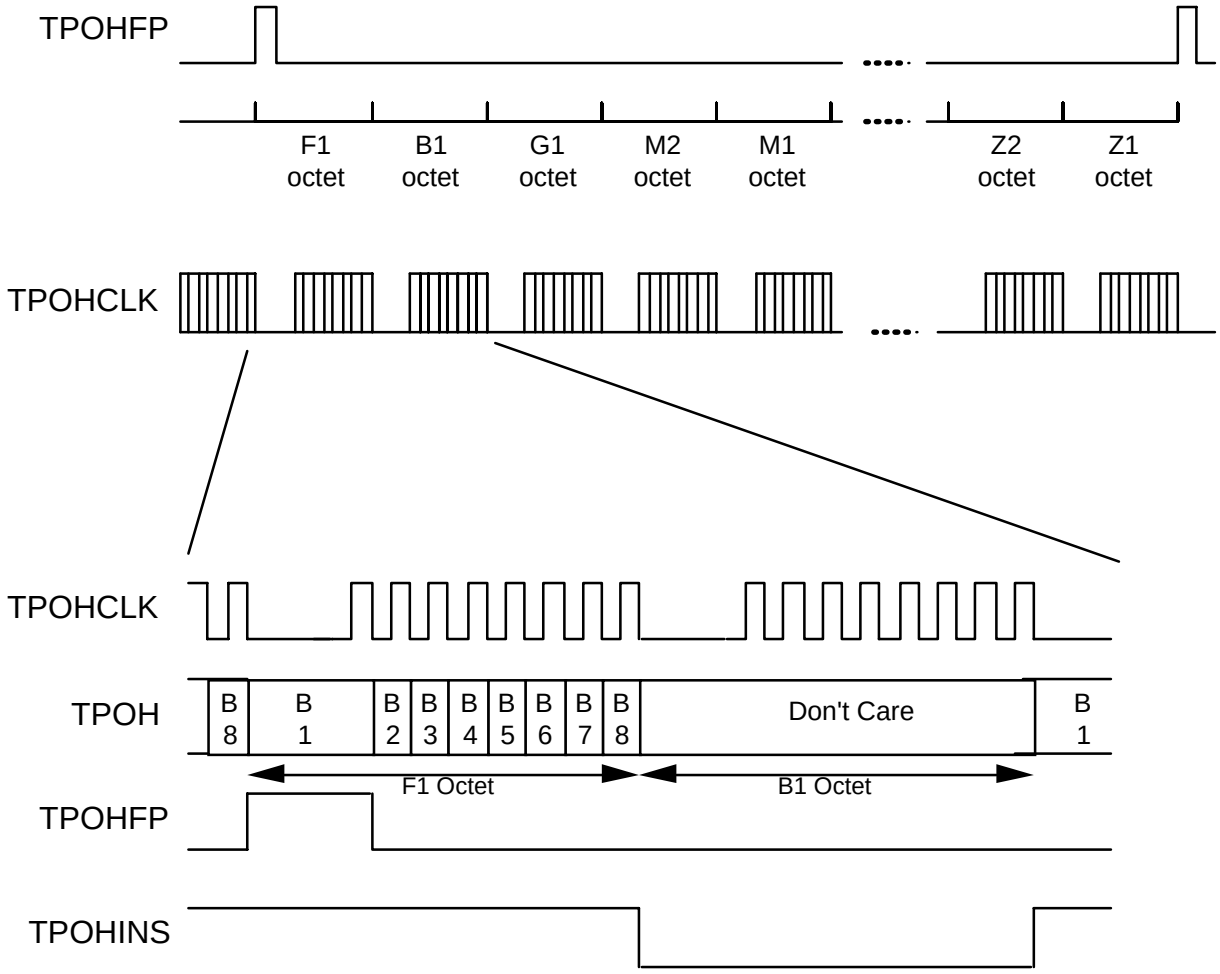
Figure 32 - Transmit G.751 E3 Overhead



The Transmit G.751 E3 Overhead diagram (figure 32) shows the insertion of G.751 overhead bits RAI,the National Use Bit, and the stuff indication and opportunity bits using the TOH input, along with the overhead insertion enable input, TOHINS. The TOHFP output is set to logic 1 once per G.751 E3 frame period (during the RAI bit position). In figure 32, the data sampled on TOH during the RAI, National Use, or stuff bit positions while TOHINS is logic 1 is inserted into the G.751 E3 overhead bits in the transmit stream.

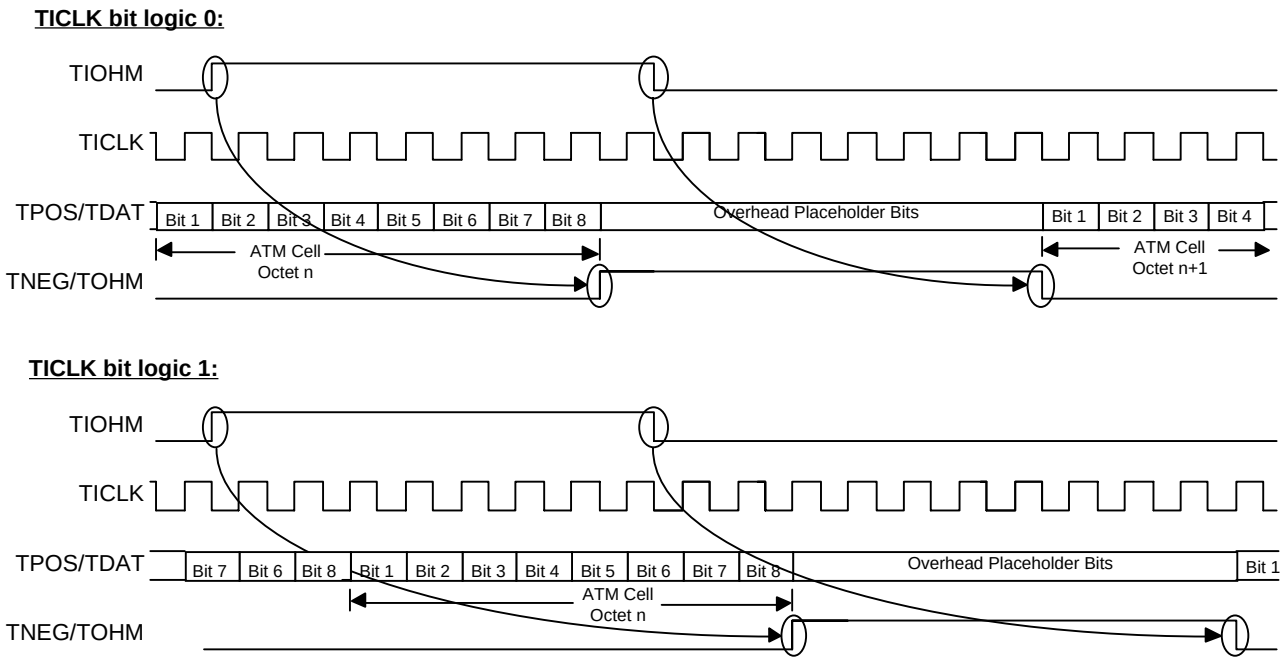
The PYLD&JUST bit in the E3 TRAN Status and Diagnostics Options register has no affect on the insertion of the justification service and the tributary justification bits through the TOH and the TOHINS inputs.

Figure 33 - Transmit PLCP Overhead



The Transmit PLCP Overhead diagram (figure 33) shows the insertion of the PLCP path overhead bits using the TPOH input, along with overhead clock (TPOHCLK), and PLCP frame position indicator (TPOHFP). The path overhead octets are shifted in order with the most significant bit (bit 1) of each octet first. The number of growth octets (Zn) in the PLCP frame varies according to the selected PLCP frame format (DS3, DS1, G.751 E3, or E1). The PLCP frame position indicator (TPOHFP) is set high once per PLCP frame period, during bit 1 of the F1 octet, and indicates the transmit PLCP frame timing. TPOH and TPOHINS are sampled using the rising edge of TPOHCLK. The bit presented on TPOH is only inserted into the path overhead if TPOHINS is asserted during the bit in question, or if the appropriate bit is set in the SPLT Control Register. The timing diagram above assumes that the SRCB1 bit in the SPLT Control Register is programmed to logic 0, thereby selecting internal insertion of that octet.

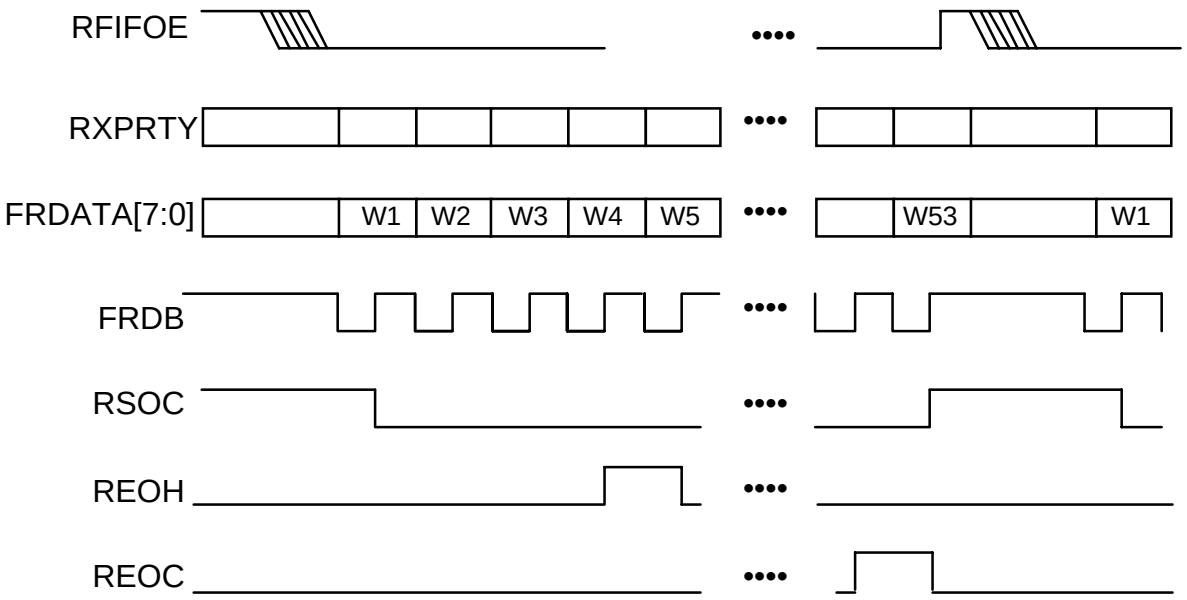
Figure 34 - Generic Transmit Stream



The Generic Transmit Stream diagram (figure 34) illustrates overhead indication positions when interfacing to a non-PLCP based transmission system not supported by the SUNI-PDH. The overhead bit placeholder positions are indicated using the TIOHM input. The ATM cells presented in the TPOS/TDAT transmit stream are held off to include the overhead placeholders. The location of these placeholder positions is indicated by TNEG/TOHM. A downstream framer inserts the correct overhead information in the placeholder positions.

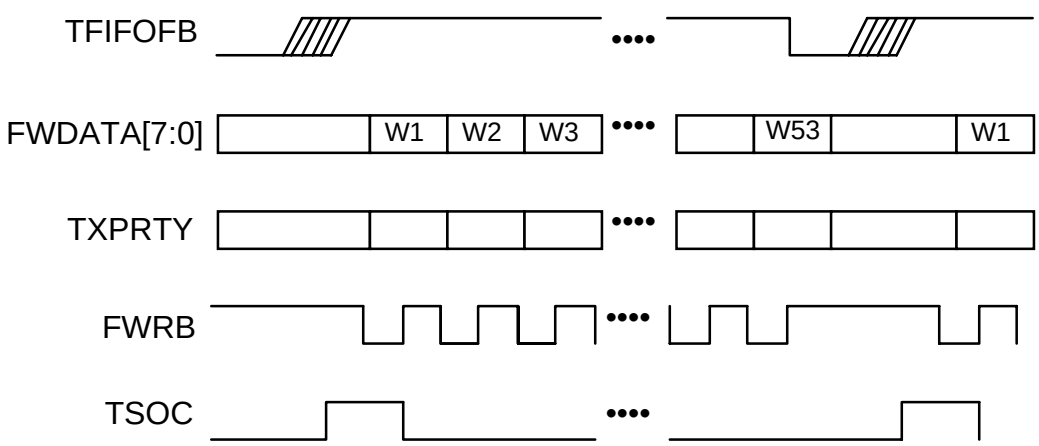
The delay between TIOHM and TNEG/TOHM is dependent on the state of the TICLK bit of the S/UNI-PDH Control register (0x03). If the TICLK bit is a logic zero, TNEG/TOHM is presented on the seventh falling edge of TICLK after the rising edge which samples TIOHM. If the TICLK bit is a logic one, TNEG/TOHM is presented on the tenth rising edge of TICLK after the rising edge which samples TIOHM.

Figure 35 - Receive FIFO Interface (84-pin PLCC and 100-pin PQFP with SYFIFOB=1)



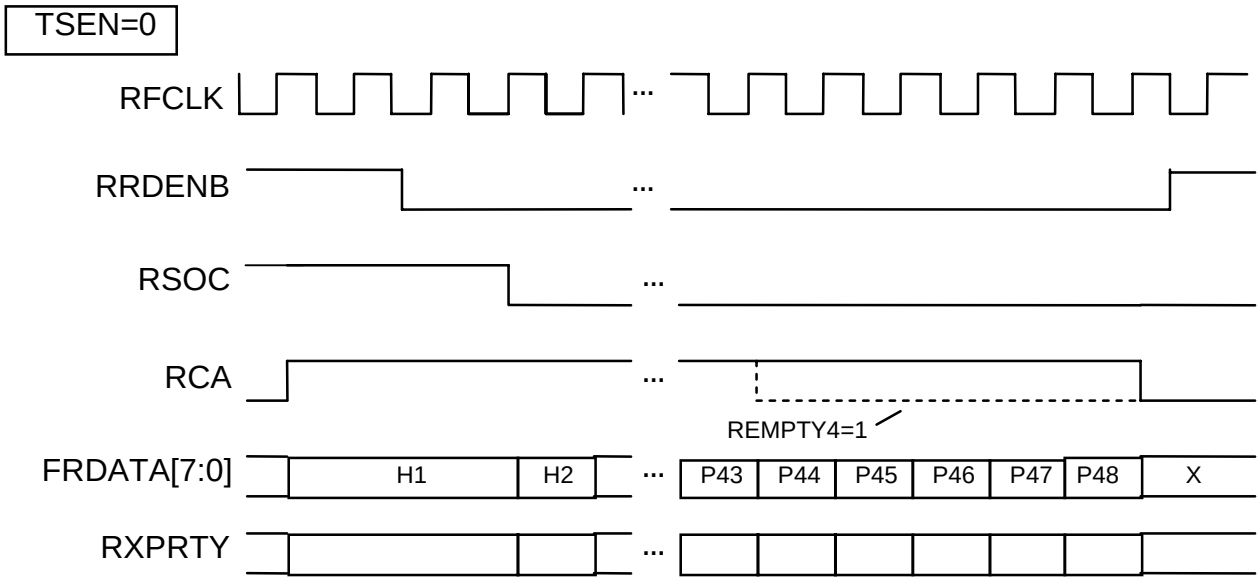
The Receive FIFO Interface diagram (figure 35) illustrates the FIFO based cell interface. The RFIFOE output transitions from a logic 1 to a logic 0 (with timing aligned to the receive line clock, RCLK) when a cell is available in the FIFO. FRDB should be held high until the cell is available. Transitions on FRDB while RFIFOE is logic 1 cause the FIFO to underrun. RFIFOE is updated at the end of each cell read from the FIFO. In figure 35, it is assumed that the FIFO is emptied before the next cell has been completely written, and RFIFOE transitions to a logic 0 when the cell write is complete. If a second cell had been completely written to the FIFO before the first cell was read, RFIFOE would have remained at logic 0 in the figure. An arbitrarily narrow pulse can be generated on RFIFOE, it is recommended that RFIFOE be externally synchronized to avoid metastability problems in downstream logic. RXPRTY is available only on the 100-pin PQFP package. The parity value is driven on RXPRTY while FRDB is low. RXPRTY is forced tristate when FRDB is high.

Figure 36 - Transmit FIFO Interface (84-pin PLCC and 100-pin PQFP with SYFIFOB=1)



The Transmit FIFO Interface diagram (figure 36) illustrates the FIFO based cell interface. The TFIFOFB output transitions from a logic 0 to a logic 1 (with timing aligned to the transmit line clock, TICLK) when the transmit FIFO is not full (one or more cell buffers are empty). FWRB should be held high while the FIFO is full. Transitions on FWRB while TFIFOFB is logic 0 cause the FIFO to overrun. TFIFOFB is updated at the end of each cell written to the FIFO. In figure 36, it is assumed that the FIFO is full at the end of the cell write, and TFIFOFB transitions to a logic 1 when a cell is not full. If a second cell buffer had been emptied before the first cell was written, TFIFOFB would have remained at logic 1 in the figure. An arbitrarily narrow pulse can be generated on TFIFOFB, it is recommended that TFIFOFB be externally synchronized to avoid metastability problems in downstream logic. TXPRTY is available only on the 100-pin PQFP package. If parity use is not desired, TXPRTY can be left unconnected (it has an integral pull-up resistor) and TPERRE should be set to logic 0 to disable transmit parity error interrupts.

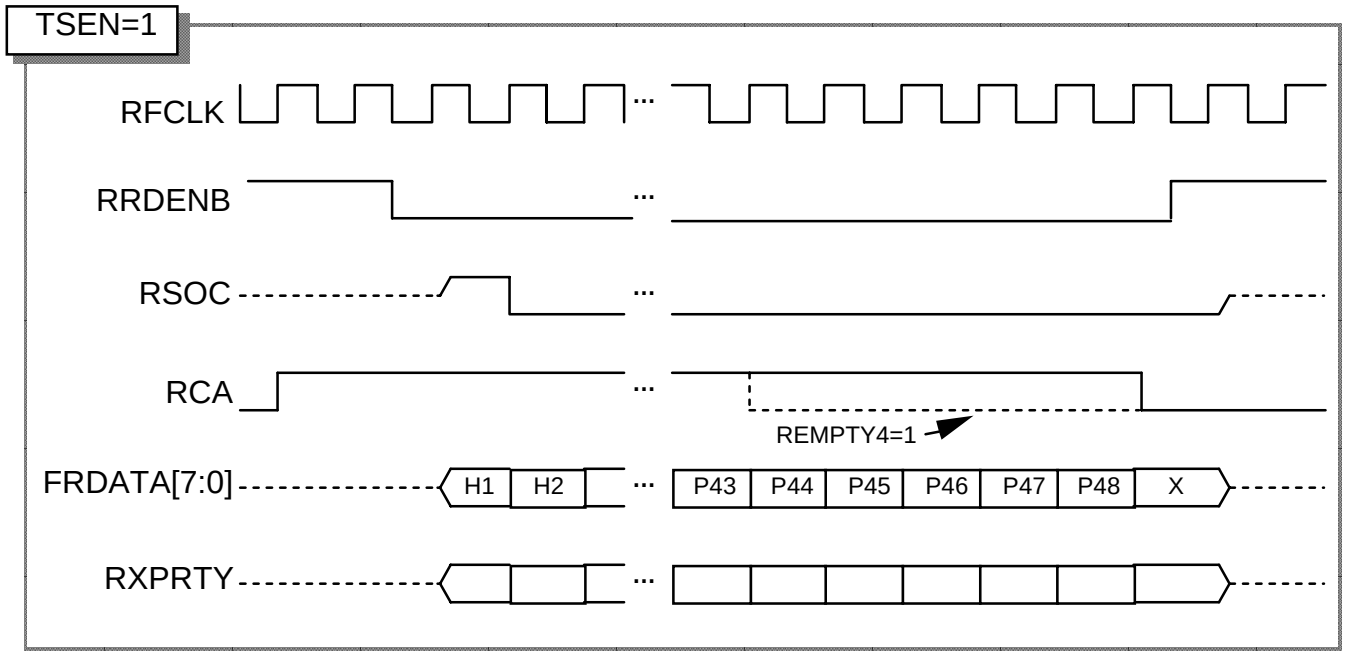
Figure 37 - Receive Synchronous FIFO (100-pin PQFP with SYFIFOB=0, TSEN=0)



The Receive Synchronous FIFO Timing, TSEN=0 Diagram (figure 37) illustrates the operation of the receive interface with tristating disabled. The S/UNI-PDH indicates a cell is available by asserting high the receive cell available output, RCA. RCA remains high until the receive FIFO is near-empty (four bytes remain in the FIFO), is empty, or if an error condition is detected. Selection of empty or near-empty indication is made with the REMPTY4 register bit in the RXCP Framing Control register. In the diagram, the near-empty option is illustrated. RCA transitions low four bytes before the last byte of the last cell is read from the FIFO. RCA remains low for a minimum of one RFCLK clock cycle and then can transition high to indicate that there are additional cells available in the FIFO. At anytime, the downstream can throttle back the reception of words by deasserting FRDENB.

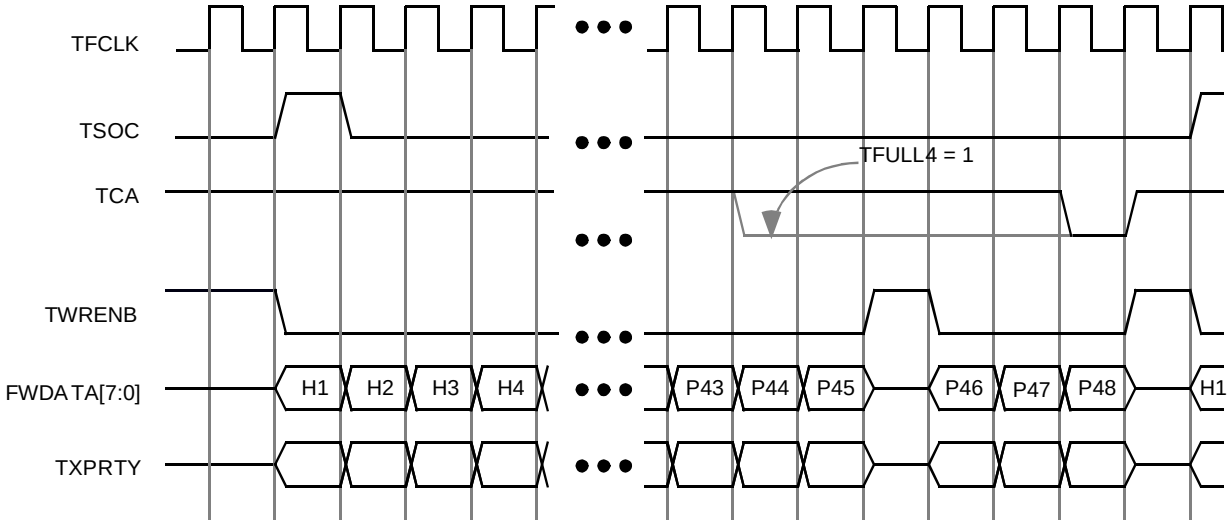
When TSEN=0, the RSOC control signal will "idle" or default to logic 1. Thus RSOC defaults high when FRDATA is undefined. RSOC will remain at logic 1 until RCA is asserted, RRDENB is asserted AND the first byte (H1) is read from the receive FIFO. RSOC is thus deasserted on the rising edge of RFCLK following the H1 being read (as shown in figure 37).

Figure 38 - Receive Synchronous FIFO (100-pin PQFP with SYFIFOB=0, TSEN=1)



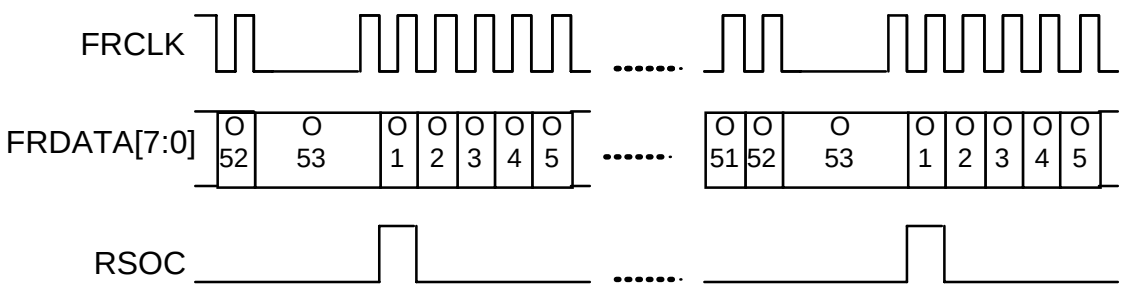
The Receive Synchronous FIFO Timing, TSEN=1 Diagram (figure 38) illustrates the operation of the receive interface with tristating enabled. If tristating is enabled (TSEN=1), the rising edge of RFCLK is used to sample RRDENB and control the tristating of the outputs.

Figure 39 - Transmit Synchronous FIFO (100-pin PQFP with SYFIFOB=0)



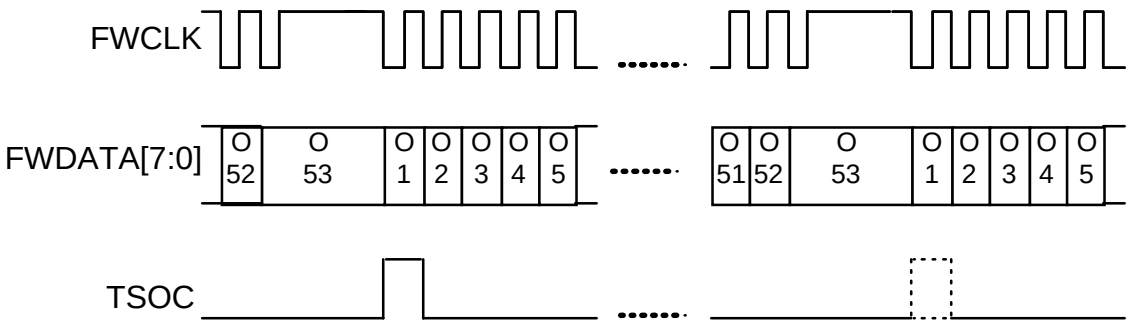
The Transmit Synchronous FIFO Timing Diagram (figure 39) illustrates the operation of the transmit interface. The S/UNI-PDH indicates that there is space available for at least one cell in the transmit FIFO by asserting high the transmit cell available output, TCA. TCA remains high until the transmit FIFO is almost full, full, or if an error condition is detected. Almost full implies that the transmit FIFO can accept at most an additional four writes. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells by the FIFODP[1:0] bits of TXCP Control register. If the programmed depth is less than four, more than one cell may be written after TCA is asserted. Selection between almost full and full is made using the TFULL4 bit in the TXCP Interrupt Enable/Status and Control register. If TCA is asserted high and the downstream is ready to write a word, the downstream device should assert TWRENB low. At anytime, if the downstream does not have a word to write, it can deassert TWRENB.

Figure 40 - Receive FIFO Bypass Interface



The Receive FIFO Bypass Interface diagram (figure 40) shows S/UNI-PDH operation when the FIFO is bypassed (using the FIFOBP bit in the S/UNI-PDH Configuration Register). The FIFO can only be bypassed when a PLCP formatted stream is processed. The read clock output, FRCLK is used to update the cell stream, FRDATA[7:0] and the cell stream status signals, RSOC, OOF and LOF.

Figure 41 - Transmit FIFO Bypass Interface



The Transmit FIFO Bypass Interface diagram (figure 41) shows S/UNI-PDH operation when the FIFO is bypassed (using the FIFOBP bit in the S/UNI-PDH Configuration Register). The FIFO can only be bypassed when a PLCP formatted stream is processed. The write clock output, FWCLK is used to sample the cell stream, FWDATA[7:0] and the cell stream status signal, TSOC.

14 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.5V to +6.0V
Voltage on Any Pin	-0.5V to V_{DD}+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+300°C
Absolute Maximum Junction Temperature	+150°C
Power Dissipation	500 mW

15 D.C. CHARACTERISTICS

T_C = -40°C to +85°C, V_{DD} = 5 V ±10%
(Typical Conditions: T_C = 25°C, V_{DD} = 5 V)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	4.5	5	5.5	Volts	
V_{IL} (TTL)	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage for TTL Inputs
V_{IH} (TTL)	Input High Voltage	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage for TTL inputs
V_{IL} (CMOS)	Input Low Voltage	-0.5		0.3* V_{DD}	Volts	Guaranteed Input LOW Voltage for CMOS Inputs
V_{IH} (CMOS)	Input High Voltage	0.7* V_{DD}		V_{DD}	Volts	Guaranteed Input HIGH Voltage for CMOS inputs
V_{OL}	Output or Bidirectional Low Voltage		0.1	0.4	Volts	V_{DD} = min, I_{OL} = 4 mA for Data Bus Pins and high speed transmit outputs and 2 mA for all others, Note 3
V_{OH}	Output or Bidirectional High Voltage	2.4	4.7		Volts	V_{DD} = min, I_{OH} = 4 mA for Data Bus Pins and high speed transmit outputs and 2 mA for all others, Note 3
V_{T+}	Reset Input High Voltage	3.5			Volts	RSTB pin only
V_{T-}	Reset Input Low Voltage			1.0	Volts	RSTB pin only
V_{TH}	Reset Input Hysteresis Voltage		1.0		Volts	RSTB pin only

I_{ILPU}	Input Low Current	+20	+83	+200	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 1, 3
I_{ILPD}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 3, 4
I_{IHPD}	Input High Current	-200	-83	-20	µA	$V_{IH} = V_{DD}$, Notes 3, 4
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 2, 3
C_{IN}	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{OUT}	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
C_{IO}	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
I_{DDOP1}	Operating Current		40	60	mA	V_{DD} = 5.5 V; Outputs Unloaded; TICLK, RCLK = 44.736 MHz; DS3 PLCP enabled, synchronous FIFO
I_{DDOP2}	Operating Current		36	55	mA	V_{DD} = 5.5 V; Outputs Unloaded; TICLK, RCLK = 44.736 MHz; DS3 PLCP enabled, asynchronous FIFO
I_{DDOP3}	Operating Current		38	55	mA	V_{DD} = 5.5 V; Outputs Unloaded; TICLK, RCLK = 44.736 MHz; DS3 PLCP disabled, asynchronous FIFO
I_{DDOP4}	Operating Current		37	55	mA	V_{DD} = 5.5 V; Outputs Unloaded; TICLK, RCLK = 34.368 MHz; E3 PLCP enabled, asynchronous FIFO

I_{DDOP5}	Operating Current		38	55	mA	V_{DD} = 5.5 V; Outputs Unloaded; TICLK, RCLK = 34.368 MHz; E3 PLCP disabled, asynchronous FIFO
I_{DDSB}	Standby Current		1		mA	V_{DD} = 5.5 V, Outputs Unloaded, No Clocks

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistor.
2. Input pin or bidirectional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Input pin or bidirectional pin with internal pull-down resistor.

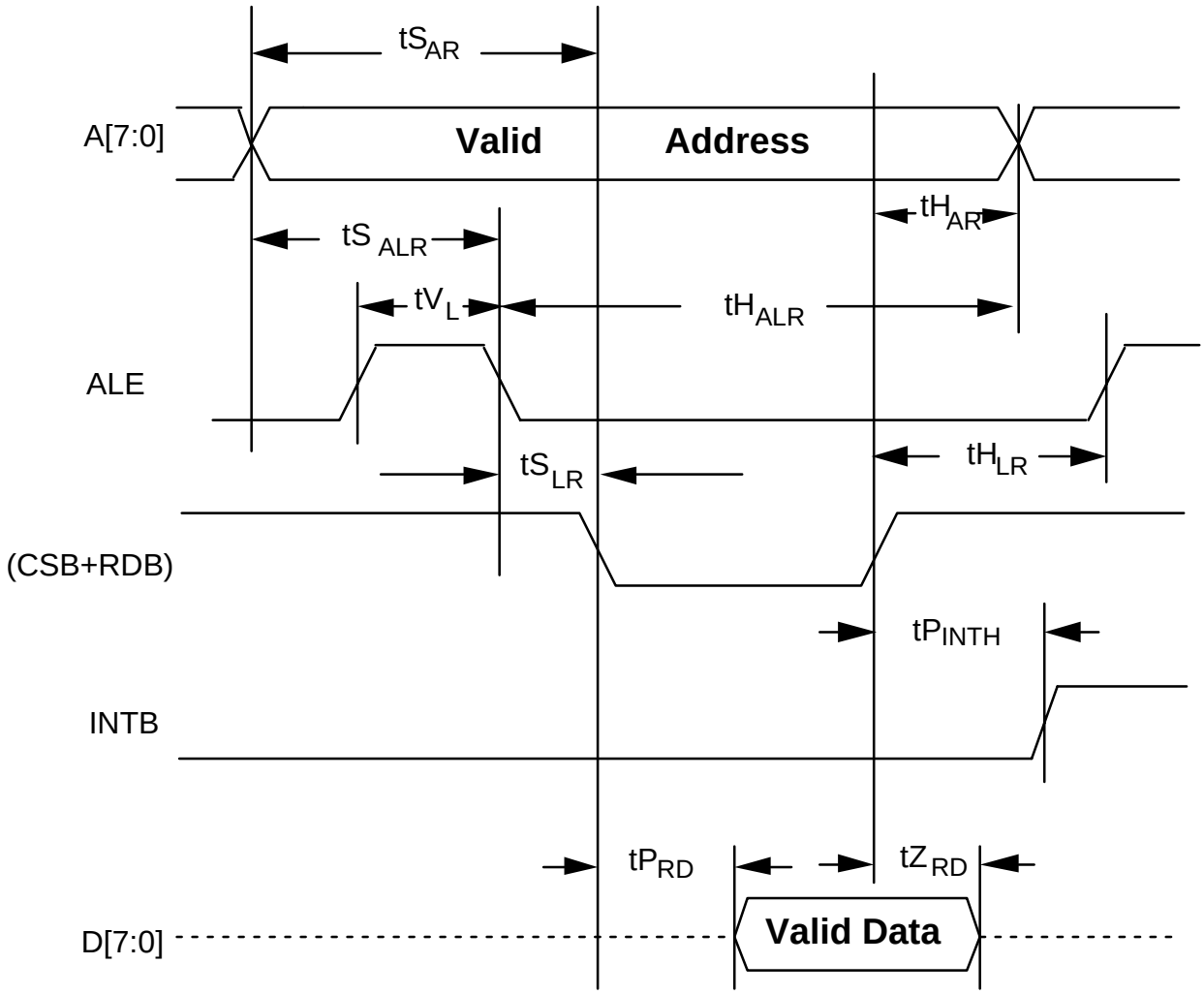
16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Microprocessor Read Access (Fig. 42)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	25		ns
tH_{AR}	Address to Valid Read Hold Time	10		ns
tS_{ALR}	Address to Latch Set-up Time	20		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	10		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Deasserted to Output Tristate		20	ns
tP_{INTH}	Valid Read Deasserted to INTB High		50	ns

Figure 42 - Microprocessor Read Access Timing



Notes on Microprocessor Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. In non-multiplexed address/data bus applications, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.

6. Parameter tH_{AR} is not applicable if address latching is used.

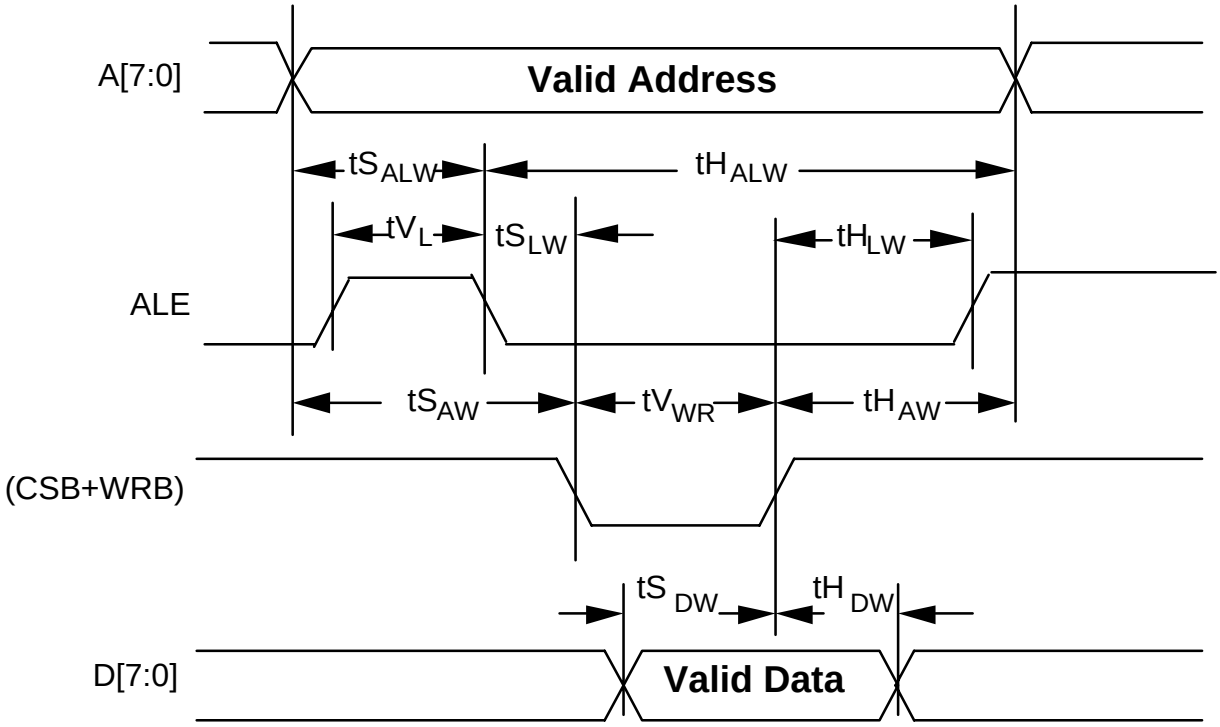
7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Microprocessor Write Access (Fig. 43)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	25		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	20		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	10		ns
tH_{DW}	Data to Valid Write Hold Time	10		ns
tH_{AW}	Address to Valid Write Hold Time	10		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 43 - Microprocessor Write Access Timing



Notes on Microprocessor Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW}, and tH_{LW} are not applicable.

4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

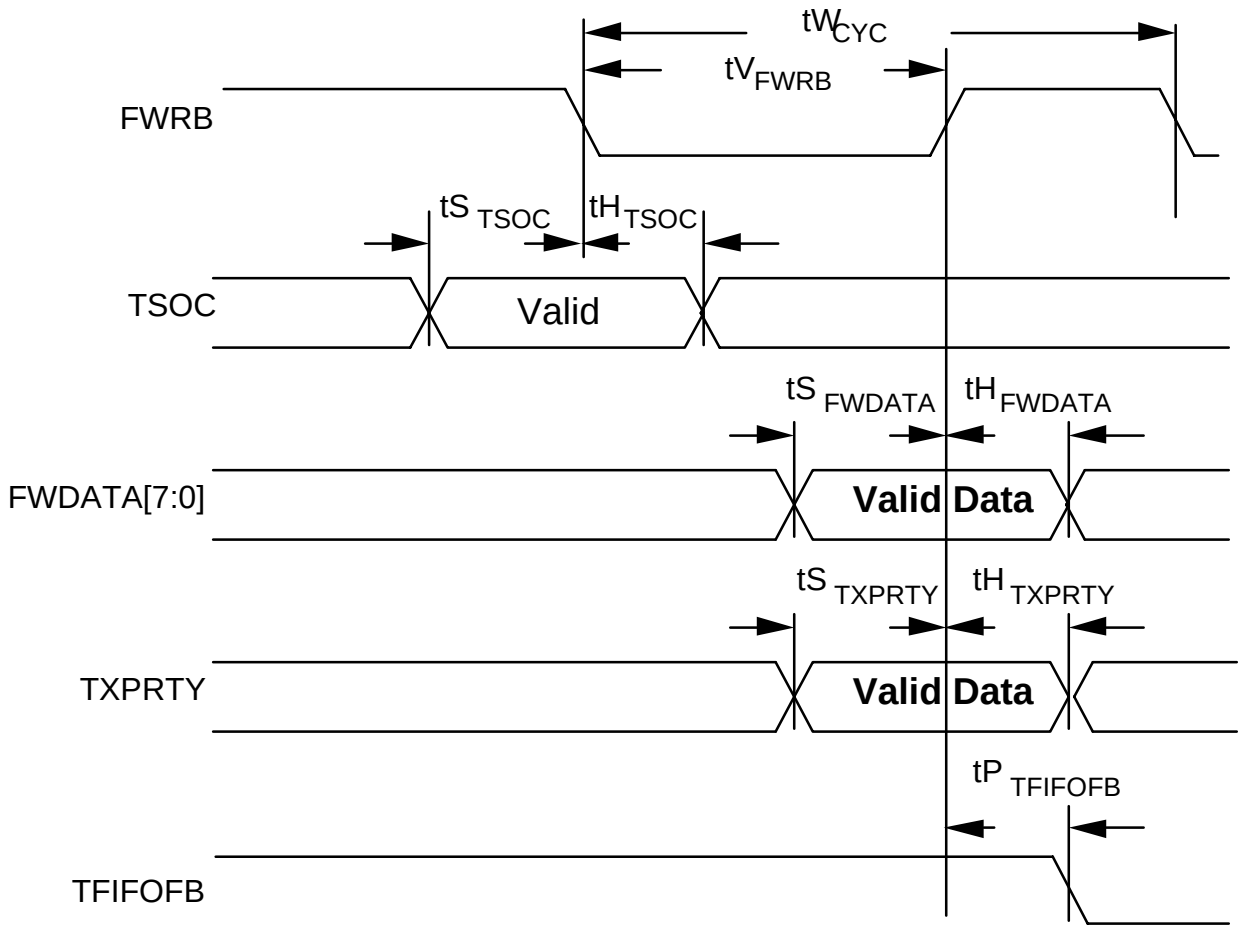
17 S/UNI-PDH TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±10%)

Asynchronous Transmit FIFO (Fig. 44)
(84-pin PLCC and 100-pin PQFP, SYFIFOB=1)

Symbol	Description	Min	Max	Units
tW_{CYC}	FIFO Write Cycle Time	70		ns
tV_{FWRB}	Valid FIFO Write Pulse Width	40		ns
tS_{TSOC}	TSOC Set-up Time	10		ns
tH_{TSOC}	TSOC Hold Time	10		ns
tS_{FWDATA}	FWDATA[7:0] Set-Up Time	20		ns
tH_{FWDATA}	FWDATA[7:0] Hold Time	10		ns
tS_{TXPRTY}	TXPRTY Set-up Time	10		ns
tH_{TXPRTY}	TXPRTY Hold Time	1		ns
$tP_{TFIFOFB}$	FWRB High to TFIFOFB Low Delay	5	50	ns

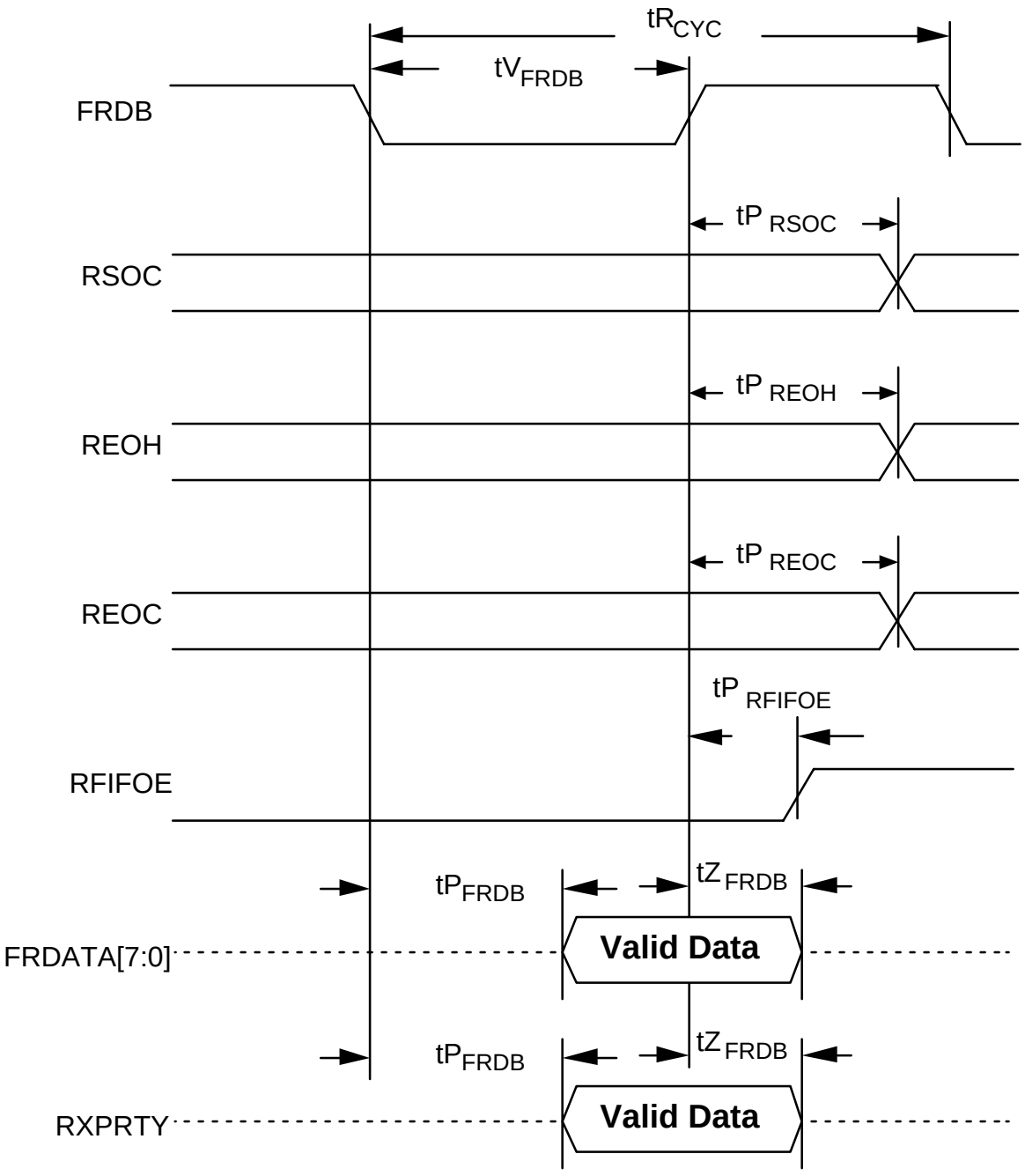
Figure 44 - Transmit FIFO Timing



Asynchronous Receive FIFO (Fig. 45) (84-pin PLCC and 100-pin PQFP, SYFIFOB=1)

Symbol	Description	Min	Max	Units
tR_{CYC}	FIFO Read Cycle Time	70		ns
tV_{FRDB}	Valid FIFO Read Pulse Width	40		ns
tP_{RSOC}	FRDB High to RSOC Valid Delay	3	20	ns
tP_{REOH}	FRDB High to REOH Valid Delay	3	20	ns
tP_{REOC}	FRDB High to REOC Valid Delay	3	20	ns
tP_{FRDB}	Valid FIFO Read to Valid Output Prop Delay	3	40	ns
tZ_{FRDB}	Valid FIFO Read Deasserted to Output Tristate	3	20	ns
tP_{RFIFOE}	FRDB High to RFIFOE High Delay	3	20	ns

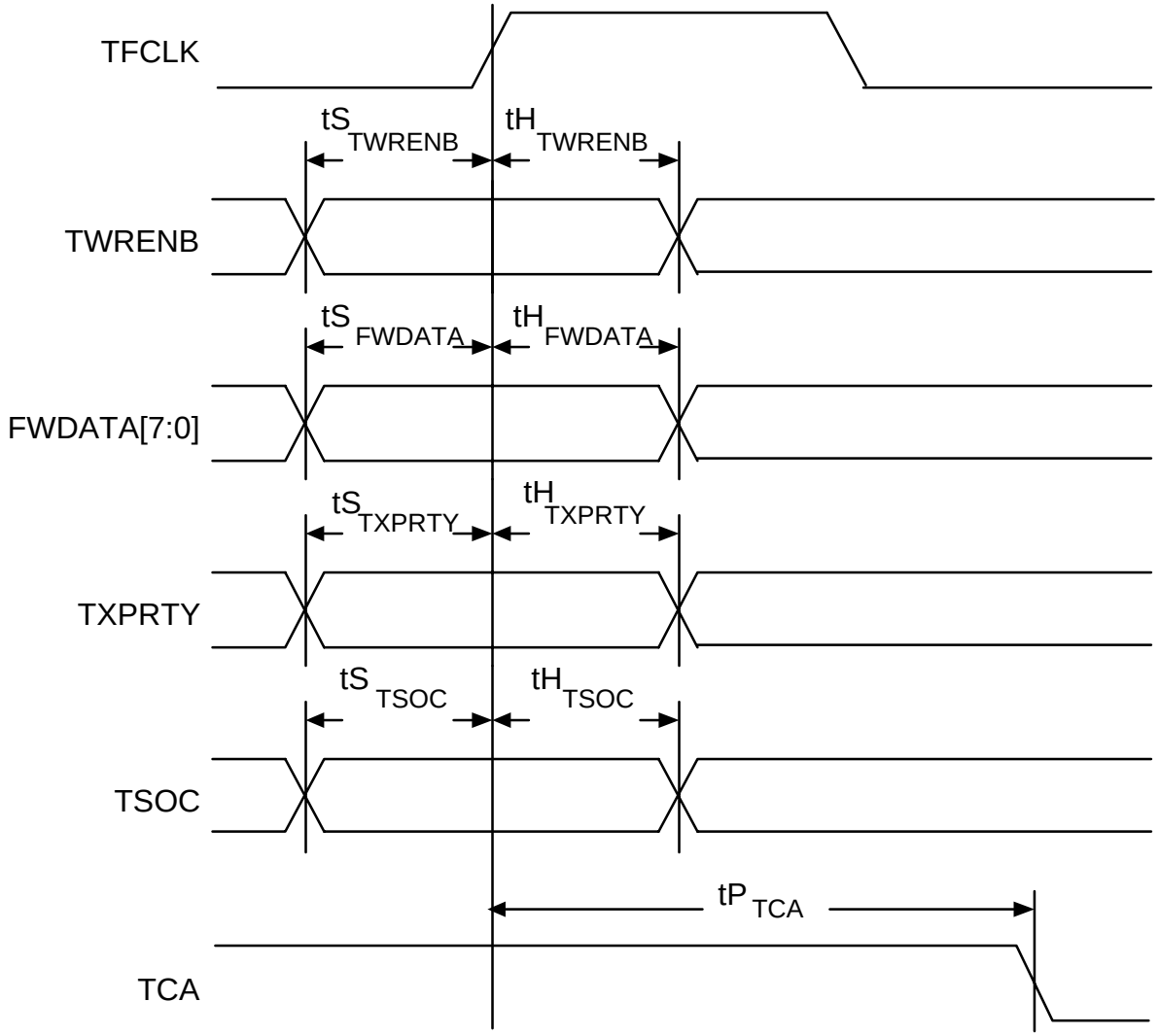
Figure 45 - Receive FIFO Timing



Synchronous Transmit FIFO (Fig. 46) (100-pin PQFP,SYFIFOB=0)

Symbol	Description	Min	Max	Units
	TFCLK Frequency		25	MHz
	TFCLK Duty Cycle	40	60	%
tS_{TWRENB}	TWRENB Set-up time to TFCLK	10		ns
tH_{TWRENB}	TWRENB Hold time to TFCLK	1		ns
tS_{FWDATA}	FWDATA[7:0] Set-up time to TFCLK	10		ns
tH_{FWDATA}	FWDATA[7:0] Hold time to TFCLK	1		ns
tS_{TXPRTY}	TXPRTY Set-up time to TFCLK	10		ns
tH_{TXPRTY}	TXPRTY Hold time to TFCLK	1		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	10		ns
tH_{TSOC}	TSOC Hold time to TFCLK	1		ns
tP_{TCA}	TFCLK High to TCA Valid	4	25	ns

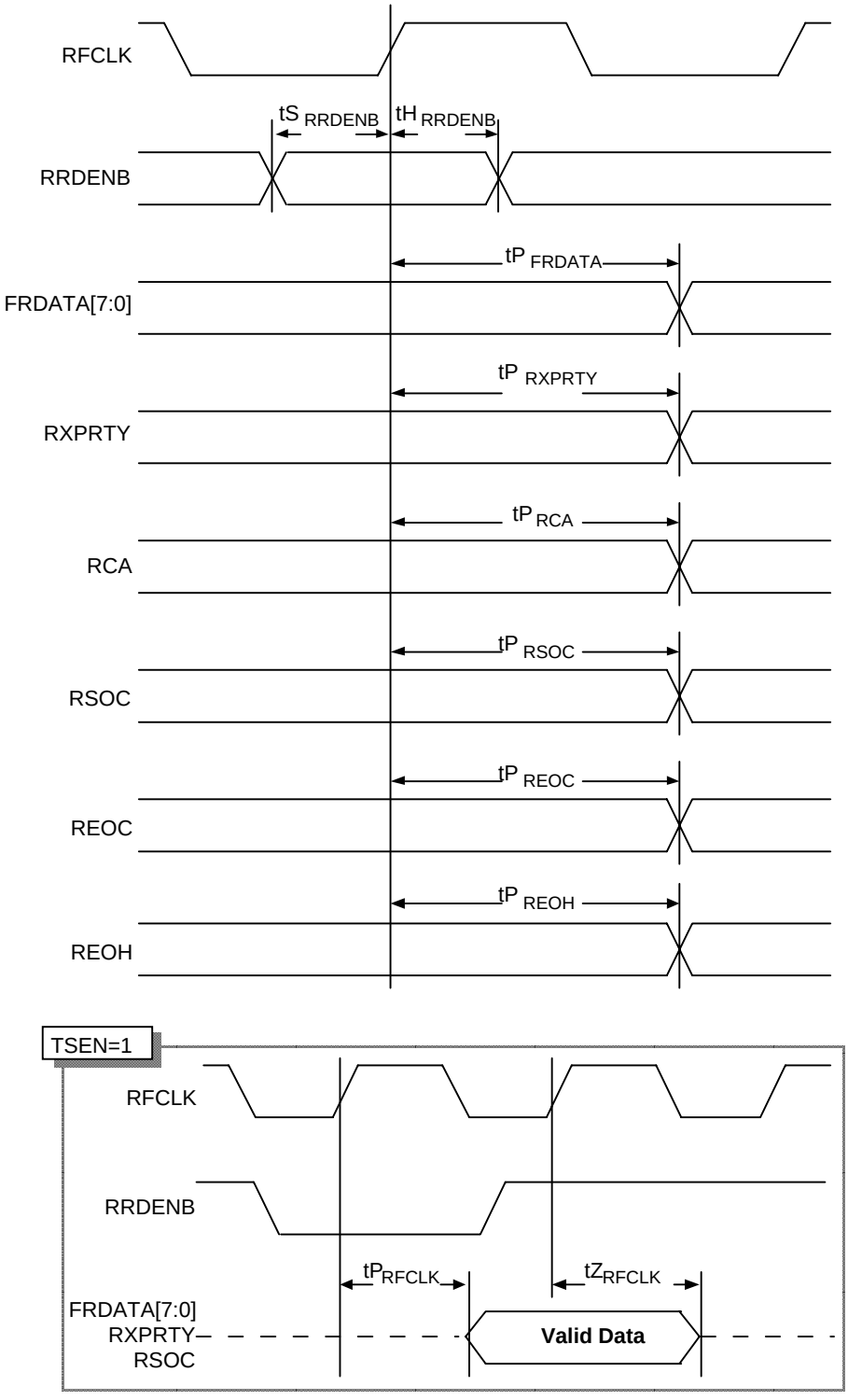
Figure 46 - Transmit FIFO Timing



Synchronous Receive FIFO (Fig. 47) (100-pin PQFP,SYFIFOB=0)

Symbol	Description	Min	Max	Units
	RFCLK Frequency		25	MHz
	RFCLK Duty Cycle	40	60	%
tS_{RRDENB}	RRDENB Set-up time to RFCLK	10		ns
tH_{RRDENB}	RRDENB Hold time to RFCLK	1		ns
tP_{RCA}	RFCLK High to RCA Valid	4	20	ns
tP_{RSOC}	RFCLK High to RSOC Valid	4	20	ns
tP_{REOC}	RFCLK High to REOC Valid	4	20	ns
tP_{REOH}	RFCLK High to REOH Valid	4	20	ns
tP_{FRDATA}	RFCLK High to FRDATA[7:0] Valid	4	20	ns
tP_{RXPRTY}	RFCLK High to RXPRTY Valid	4	20	ns
tP_{RFCLK}	RFCLK High to Output Enable	4	20	ns
tZ_{RFCLK}	RFCLK High to Output Tristate	4	20	ns

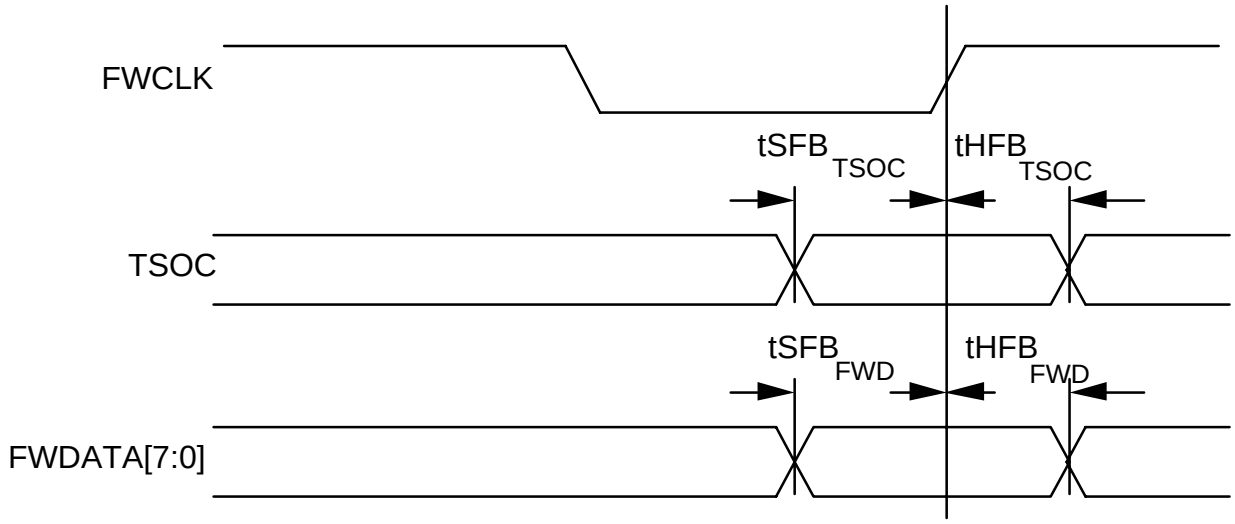
Figure 47 - Receive FIFO Timing



Transmit System Side - FIFO Bypass (Fig. 48)

Symbol	Description	Min	Max	Units
	FWCLK Frequency (TICLK / 8)		6.5	MHz
$tSFB_{TSOC}$	TSOC Set-up Time	25		ns
$tHFB_{TSOC}$	TSOC Hold Time	10		ns
$tSFB_{FWD}$	FWDATA[7:0] Set-Up Time	25		ns
$tHFB_{FWD}$	FWDATA[7:0] Hold Time	10		ns

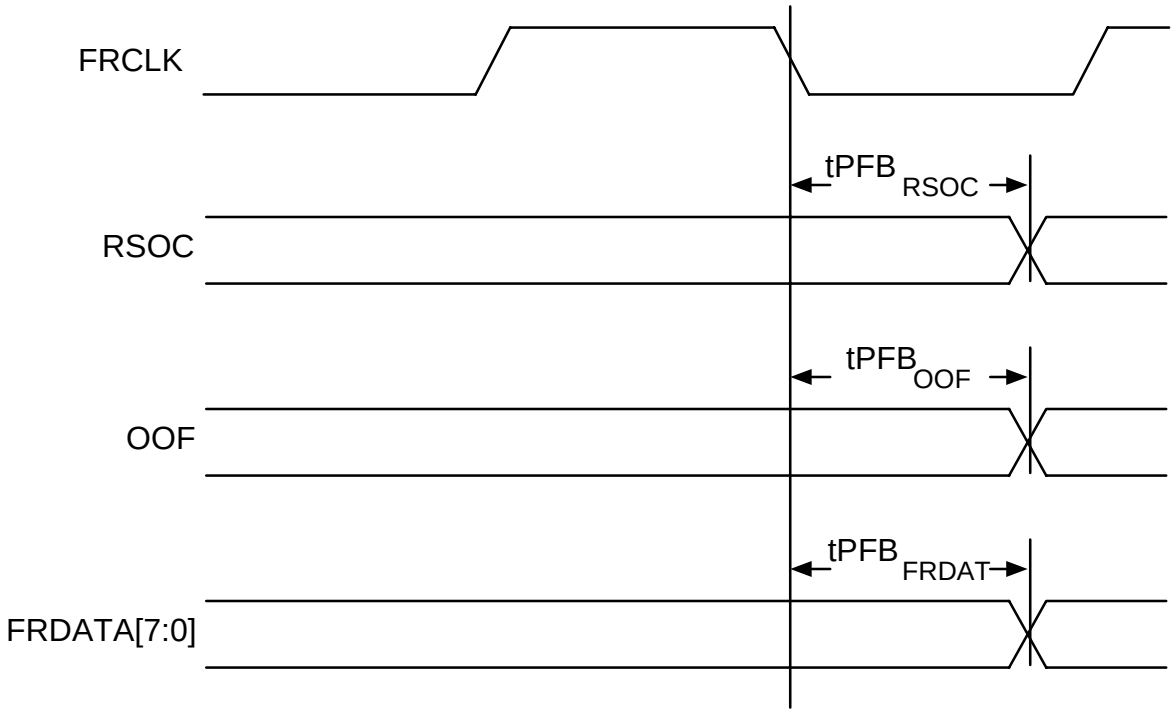
Figure 48 - Transmit System Side - FIFO Bypass



Receive System Side - FIFO Bypass (Fig. 49)

Symbol	Description	Min	Max	Units
	FRCLK Frequency (RCLK / 8)		6.5	MHz
$tPFB_{RSOC}$	FRCLK Low to RSOC Valid Delay	-10	10	ns
$tPFB_{OOF}$	FRCLK Low to OOF Valid Delay	-10	10	ns
$tPFB_{FRDAT}$	FRCLK Low to FRDATA[7:0] Valid Delay	-10	10	ns

Figure 49 - Receive System Side - FIFO Bypass



S/UNI-PDH Input (Fig. 50)

Symbol	Description	Min	Max	Units
	TICLK Frequency: framer bypass DS3 Framer E3 Framer		52 45 35	MHz
	TICLK Duty Cycle	40	60	%
tS_{TIOHM}	TIOHM Set-up Time	5		ns
tH_{TIOHM}	TIOHM Hold Time	4		ns
tS_{TOH}	TOH Set-Up Time	20		ns
tH_{TOH}	TOH Hold Time	20		ns
tS_{TOHINS}	TOHINS Set-Up Time	20		ns
tH_{TOHINS}	TOHINS Hold Time	20		ns
tS_{TPOH}	TPOH Set-Up Time	20		ns
tH_{TPOH}	TPOH Hold Time	20		ns
tS_{TPOHIN}	TPOHINS Set-Up Time	20		ns
tH_{TPOHIN}	TPOHINS Hold Time	20		ns
	RCLK Frequency: framer bypass DS3 Framer E3 Framer		52 45 35	MHz
	RCLK Duty Cycle	40	60	%
tS_{RPOS}	RPOS/RDAT Set-up Time	5		ns
tH_{RPOS}	RPOS/RDAT Hold Time	4		ns
tS_{RNEG}	RNEG/ROHM Set-Up Time	5		ns
tH_{RNEG}	RNEG/ROHM Hold Time	4		ns
tS_{DIN}	TDLCLK to TDLSIG Input Set-up Time	80		ns
tH_{DIN}	TDLCLK to TDLSIG Input Hold Time	20		ns

Figure 50 - Input Timing

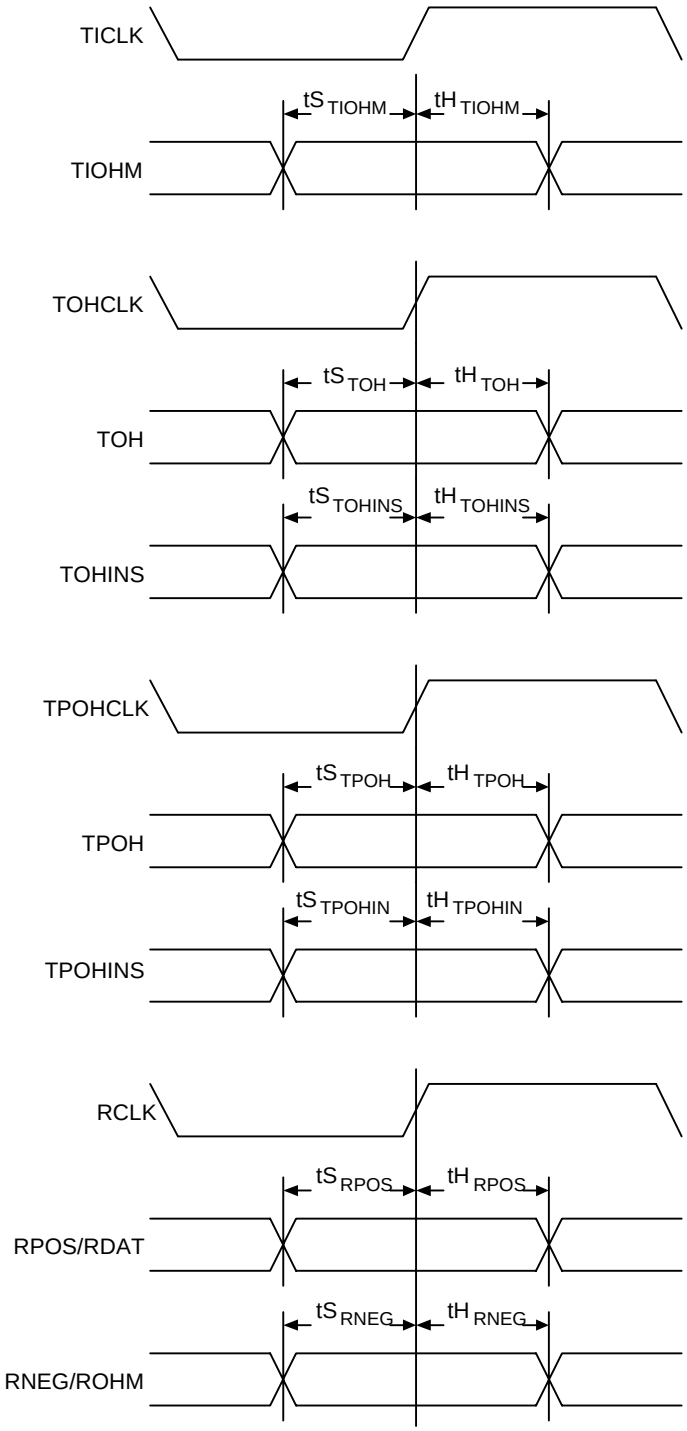
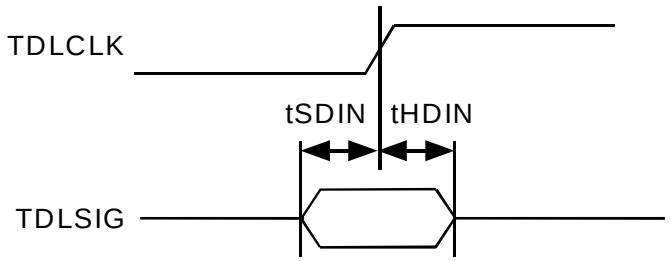


Figure 51 - Input Timing – cont'd



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 50% point of the input to the 50% point of the clock for CMOS inputs.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 50% point of the clock to the 50% point of the input for CMOS inputs.

3. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock for TTL inputs.

4. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input for TTL inputs.

S/UNI-PDH Output (Fig. 51 and 52)

Symbol	Description	Min	Max	Units
tP_{TCLK}	TICLK Edge to TCLK EDGE Prop Delay	2	15	ns
tP_{TPOS}	TCLK Low to TPOS/TDAT Valid Prop Delay	-1	5	ns
tP_{TNEG}	TCLK Low to TNEG/TOHM Valid Prop Delay	-1	5	ns
tP_{TPOS2}	TICLK High to TPOS/TDAT Valid Prop Delay	2	15	ns
tP_{TNEG2}	TICLK High to TNEG/TOHM Valid Prop Delay	2	15	ns
tP_{TOHFP}	TOHCLK Low to TOHFP Valid Prop Delay	-15	20	ns
tP_{TPOHFP}	TPOHCLK Low to TPOHFP Valid Prop Delay	-15	20	ns
tP_{ROH}	ROHCLK Low to ROH Valid Prop Delay	-15	20	ns
tP_{ROHFP}	ROHCLK Low to ROHFP Valid Prop Delay	-15	20	ns
tP_{RPOH}	RPOHCLK Low to RPOH Valid Prop Delay	-15	20	ns
tP_{RPOHFP}	RPOHCLK Low to RPOHFP Valid Prop Delay	-15	20	ns
tP_{RDLCLK}	RDLCLK to RDLSIG Propagation Delay		50	ns

Figure 52 - Output Timing

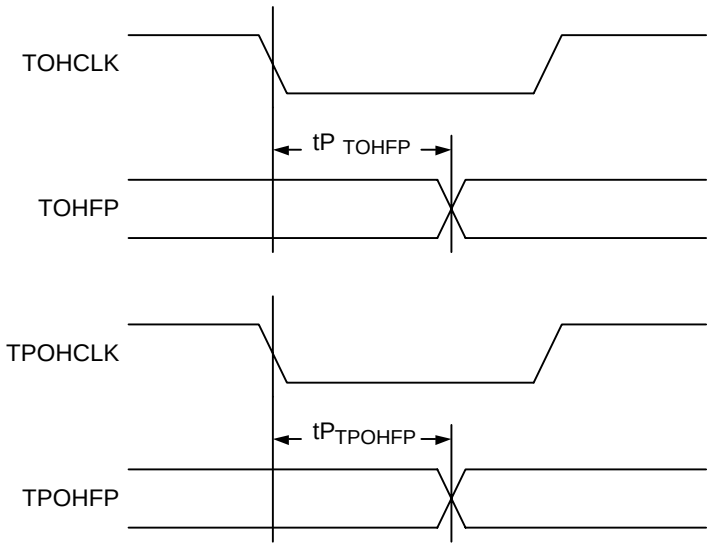
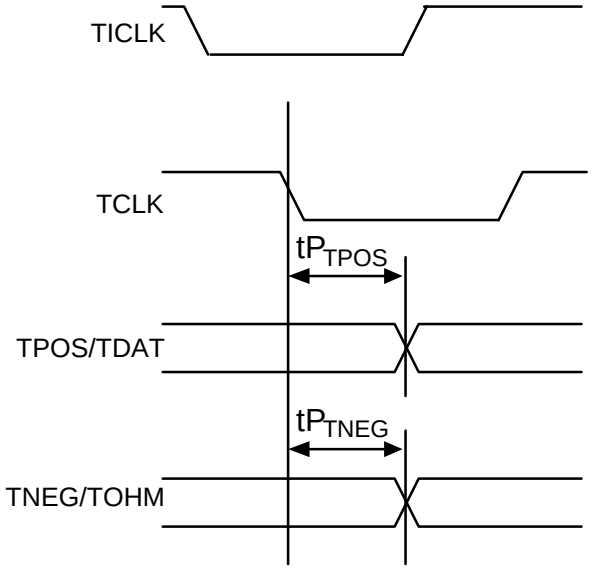
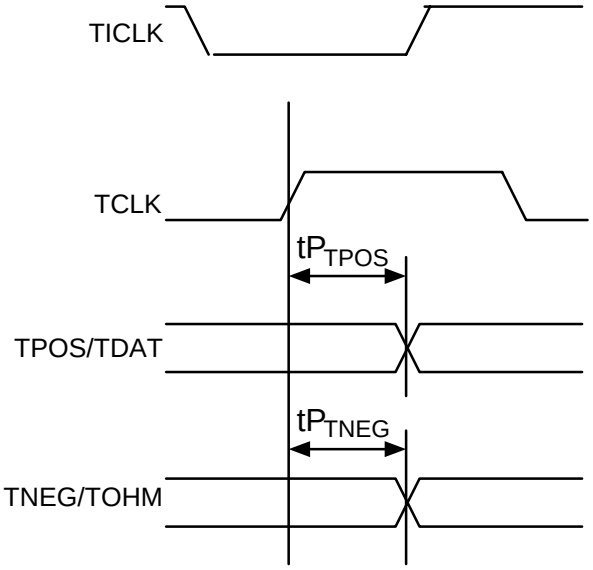


Figure 53 - Output Timing - cont'd

TICLK=0, TCLKINV=0



TICLK=0, TCLKINV=1



TICLK=1, TCLKINV=X

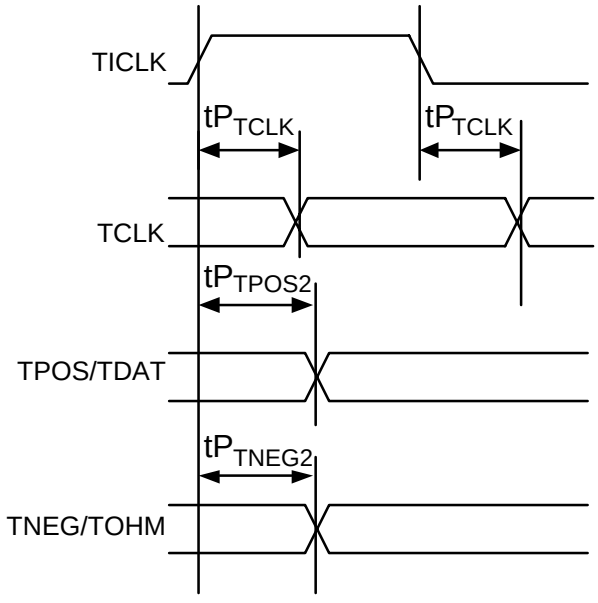
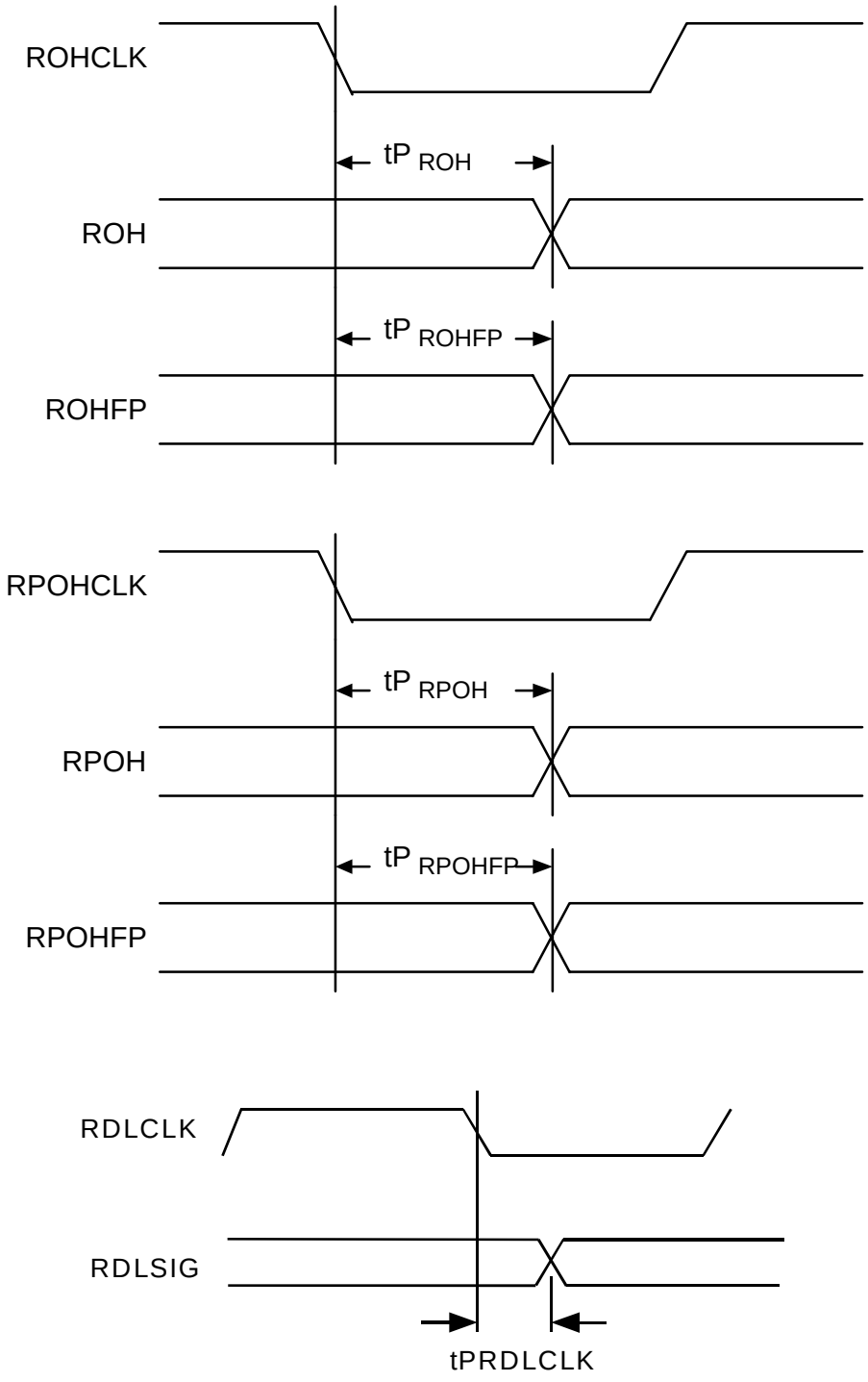


Figure 54 - Overhead Output Timing



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 50% point of the output for CMOS inputs

2. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output for TTL inputs

3. Minimum and maximum output propagation delays are measured with a 22 pF load on the TCLK, TPOS, and TNEG outputs.

4. Minimum and maximum output propagation delays are measured with a 50 pF load on all other outputs.

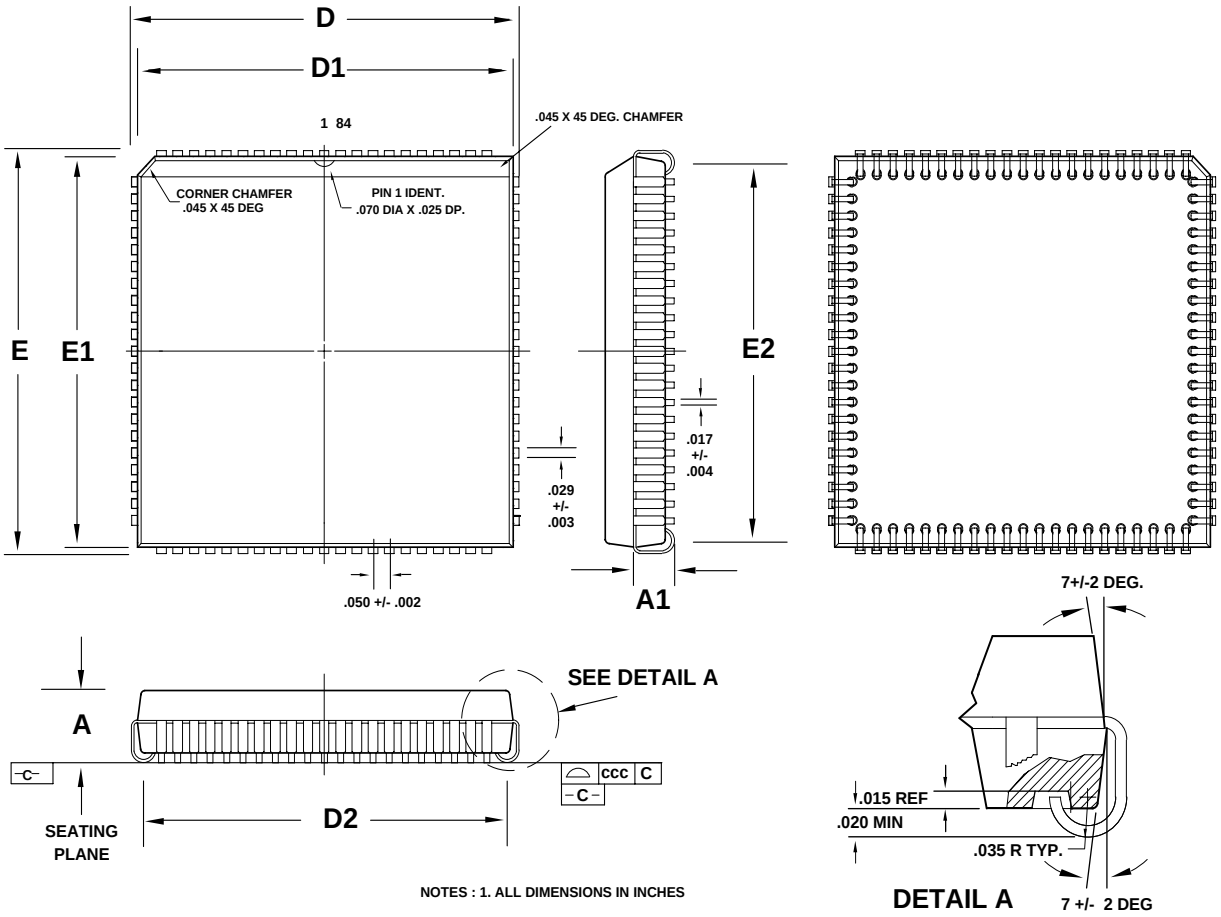
18 ORDERING AND THERMAL INFORMATION

PART NO.	DESCRIPTION
PM7345-QI	84 Plastic Leaded Chip Carrier (PLCC)
PM7345-RI	100 Plastic Quad Flat Pack (PQFP)

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM7345-QI	-40°C to 85°C	36 °C/W	10 °C/W
PM7345-RI	-40°C to 85°C	62 °C/W	16 °C/W

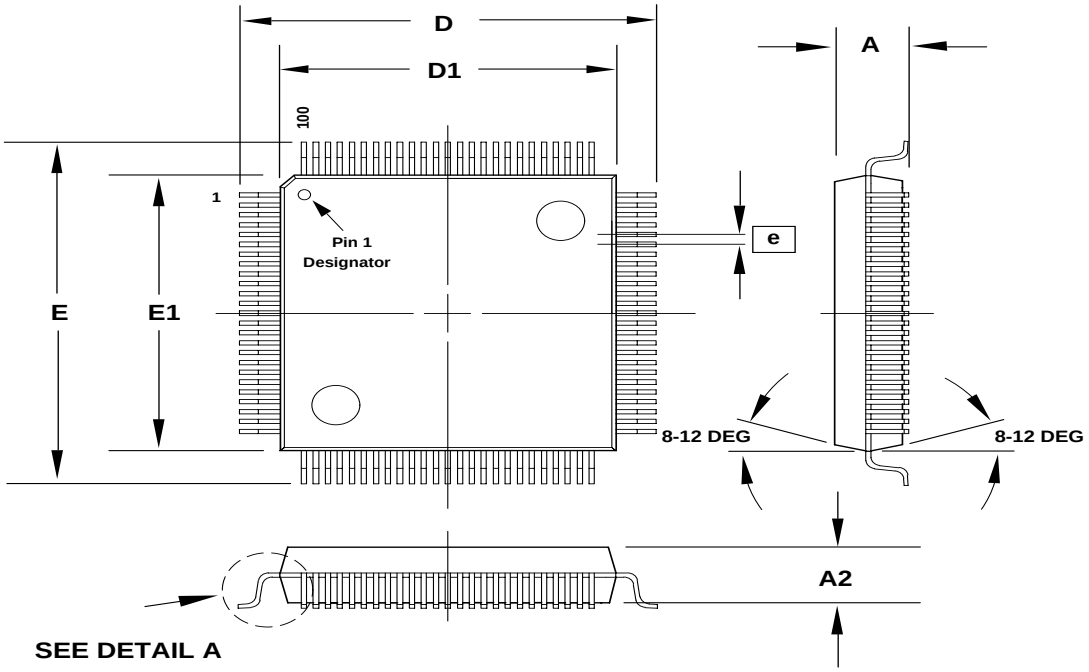
19 MECHANICAL INFORMATION

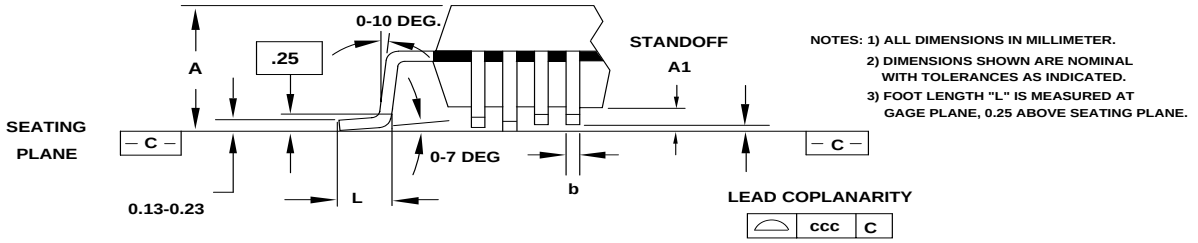
19.1 84 Pin Plastic Leaded Chip Carrier (Q Suffix):



PACKAGE TYPE: 84 PIN PLASTIC LEADED CHIP CARRIER-PLCC									
Dim.	A	A1	D	D1	D2	E	E1	E2	ccc
Min.	0.165	0.090	1.185	1.150	1.090	1.185	1.150	1.090	
Nom.	0.175		1.190	1.154	1.120	1.190	1.154	1.120	
Max.	0.200	0.130	1.195	1.158	1.130	1.195	1.158	1.130	0.004

19.2 100 Pin Plastic Quad Flat Pack (R Suffix):





DETAIL A

PACKAGE TYPE: 100 PIN METRIC PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 14 x 14 x 2.0 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	2.05	0.10	1.95	16.95	13.90	16.95	13.90	0.73		0.17	
Nom.	2.17	0.17	2.00	17.20	14.00	17.20	14.00	0.88	0.50	0.22	
Max.	2.35	0.25	2.10	17.45	14.10	17.45	14.10	1.03		0.27	0.10

NOTES

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PMC-931011 (R6) ref PMC-930818 (R9) Issue date: June 1998