PM7344

S/UNI-MPH™

S/UNI-MPH

SATURN QUAD T1/E1 MULTI-PHY USER NETWORK INTERFACE DEVICE

DATA SHEET

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1 FEATURES

- Single chip quad ATM User Network Interface operating at 1.544 Mbit/s or 2.048 Mbit/s.
- Implements the ATM Forum User Network Interface Specification V3.1 for DS1 and E1 transmission rates.
- Implements the ATM physical layer for Broadband ISDN according to ITU-T Recommendation I.432.
- Implements the direct cell mapping into DS1 or E1 transmission systems according to ITU-T Recommendation G.804.
- Implements (with an external framer device) the direct cell mapping into J2 (6.312 Mbit/s) transmission systems according to ITU-T Recommendation G.804.
- Integrates a quad full-featured T1/E1 framer/transmitter for terminating four duplex 1.544 Mbit/s DS-1 signals or four duplex 2.048 Mbit/s E1 signals.
- Integrates a quad ATM cell processor for mapping ATM cells into T1, E1 and other arbitrary rate streams using HEC (Header Check Sequence Error Correction) cell delineation.
- Provides Saturn Compatible Interface (SCI-PHY™) FIFO buffers in both transmit and receive paths with parity support and Utopia Level 2 compatible multi-PHY control signals.
- Software compatible with the PM4341A T1XC, PM6341 E1XC, and PM7345 S/UNI-PDH.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power, +5V, CMOS technology
- 128 pin rectangular (14mm x 20mm) PQFP package.

The T1 framer section:

- Recovers clock and data using a digital phase locked loop for high jitter tolerance. A direct clock input is provided to allow clock recovery to be bypassed.
- Accepts dual rail or single rail digital PCM inputs.
- Supports B8ZS or AMI line code.
- Accepts gapped data streams to support higher rate demultiplexing.
- Frames to SF or ESF format DS1 signals. Provides loss of signal detection, and red, yellow, and AIS alarm detection. Red, yellow, and AIS alarms are integrated as per industry specifications.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192 bit window.
- Provides programmable framed or unframed in-band loopback code detection.
- Supports line and path performance monitoring according to ANSI specifications. Accumulators are provided for counting:
    - ESF CRC-6 errors to 333 per second;
    - Framing bit errors to 31 per second;
    - Line code violations to 4095 per second; and
    - Loss of frame or change of frame alignment events to 7 per second.
- Provides ESF bit-oriented code detection, and an HDLC interface for terminating the ESF data link.
- Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Extracts the data link in ESF mode.

The T1 transmitter section:

- Formats data to SF or ESF format DS1 signals.

- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192 bit window or optionally stuffs ones to maintain minimum ones density.
- Allows insertion of framed or unframed in-band loopback code sequences.
- Allows insertion of the data link in ESF mode.
- Supports transmission of the alarm indication signal (AIS) or the yellow alarm signal in all formats.
- Provides ESF bit-oriented code generation and an HDLC interface for generating the ESF data link.
- Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Supports B8ZS or AMI line code.
- Provides dual rail or single rail digital PCM output signals.

The E1 receiver section:

- Recovers clock and data using a digital phase locked loop for high jitter tolerance. A direct clock input is provided to allow clock recovery to be bypassed.
- Accepts dual rail or single rail digital PCM inputs.
- Supports HDB3 or AMI line code.
- Accepts gapped data streams to support higher rate demultiplexing.
- Frames to a G.704 2048 kbit/s signal within 1 ms.
- Frames to the CRC multiframe alignment when enabled.
- Frames to the signalling multiframe alignment when enabled.
- Provides loss of signal detection, and indicates loss of frame alignment (OOF), loss of signalling multiframe alignment and loss of CRC multiframe alignment.
- Supports line and path performance monitoring according to ITU-T recommendations. Accumulators are provided for counting:
    - CRC-4 errors to 1000 per second;

- Far end block errors to 1000 per second;
- Frame sync errors to 127 per second; and
- Line code violations to 8191 per second;

- Indicates the reception of remote alarm.
- Indicates the reception of alarm indication signal (AIS).
- Declares RED and AIS alarms using Q.516 recommended integration periods.
- Provides an HDLC interface for terminating a data link. Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Optionally extracts the data link from timeslot 16 (64 kbit/s), which may be used to receive common channel signalling, or from any combination of the national bits in timeslot 1 of non-frame alignment signal frames (4 kbit/s - 20 kbit/s).

The E1 transmitter section:

- Formats data to create a G.704 2048 kbit/s signal. Optionally inserts signalling multiframe alignment signal. Optionally inserts CRC multiframe structure including optional transmission of far end block errors.
- Supports transmission of the alarm indication signal (AIS), timeslot 16 AIS, remote alarm signal or remote multiframe alarm signal.
- Provides an HDLC interface for generating a data link. Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Optionally inserts the data link into timeslot 16 (64 kbit/s), which may be used to transmit common channel signalling, or into any combination of the national bits in timeslot 0 of non-frame alignment signal frames (4 kbit/s - 20 kbit/s).
- Supports HDB3 or AMI line code.
- Provides dual rail or single rail digital PCM output signals.

The receive ATM cell processor section:

- Provides ATM framing using cell delineation.
- Provides cell descrambling, header check sequence (HCS) error detection, idle/unassigned cell filtering, and accumulates the number of received idle/unassigned cells, the number of received cells written to the FIFO, and the number of HCS errors.
- Provides a four cell FIFO for rate decoupling between the line, and a higher layer processing entity.
- Provides a synchronous 8-bit wide FIFO with receive byte parity generation and timing compatible with the Saturn Compatible Interface Specification (SCI-PHY™) for multi-PHY interfaces.
- All four receive ATM cell processors are serviced via a single 8-bit wide multi-PHY interface.

The transmit ATM cell processor section:

- Provides optional ATM cell scrambling, HCS generation/insertion, programmable idle/unassigned cell insertion, diagnostics features and accumulates transmitted cells read from the FIFO.
- Provides a four cell FIFO for rate decoupling between the line, and a higher layer processing entity.
- Provides a synchronous 8-bit wide FIFO with transmit byte parity checking and timing compatible with the Saturn Compatible Interface Specification (SCI-PHY™) for multi-PHY interfaces.
- All four transmit ATM cell processors are serviced via a single 8-bit wide multi-PHY interface.

Loopback features:

- Provides for DS1 or E1 line loopback, payload loopback, or diagnostic loopback.

2 APPLICATIONS

- ATM Switches Supporting DS1 or E1 UNI Ports
- ATM Switches Supporting DS3 Ports Carrying Multiplexed DS1 or E1 UNI Signals
- ATM Switches Supporting STS-3/STM-1 Or Other SONET/SDH Ports Carrying Tributary Mapped DS1 or E1 UNI Signals
- ATM Customer Premise Equipment Supporting Multiple DS1 or E1 UNI Ports

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16. ITU-T Recommendation G.738, - "Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s and Offering Synchronous Digital Access at 320 kbit/s and/or 64 kbit/s", Blue Book Fasc. III.4, 1988.

17. ITU-T Recommendation G.739, - "Characteristics of an External Access Equipment Operating at 2048 kbit/s Offering Synchronous Digital Access at 320 kbit/s and/or 64 kbit/s", Blue Book Fasc. III.4, 1988.

18. ITU-T Recommendation G.742, - "Second Order Digital Multiplex Equipment Operating at 8448 kbit/s and Using Positive Justification", Blue Book Fasc. III.4, 1988.

19. ITU-T Recommendation G.821, - "Error Performance of an International Digital Connection Forming Part of an Integrated Services Digital Network", Blue Book Fasc. III.5, 1988.

20. ITU-T Recommendation G.823, - "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy", 1993.

21. ITU-T Recommendation O.151, - "Error Performance Measuring Equipment Operating at the Primary Rate and Above", Rev. 1, Oct. 1992.

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23. ITU-T, Recommendation I.432 - “B-ISDN User-Network Interface - Physical Layer Specification”, August 1992.

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25. ITU-T, Draft Recommendation G.832 - “Transport of SDH Elements on PDH Networks: Frame and Multiplexing Structures”, January 1993.

26. ETSI DE/TM-1015 - "Transmission and Multiplexing (TM); Generic Functional Requirements for SDH Transmission Equipment, Part 1: Generic Processes and Performance", Version 1.0, November, 1993.

27. ATM Forum, V3.1, August, 1994 - “ATM User-Network Interface Specification”

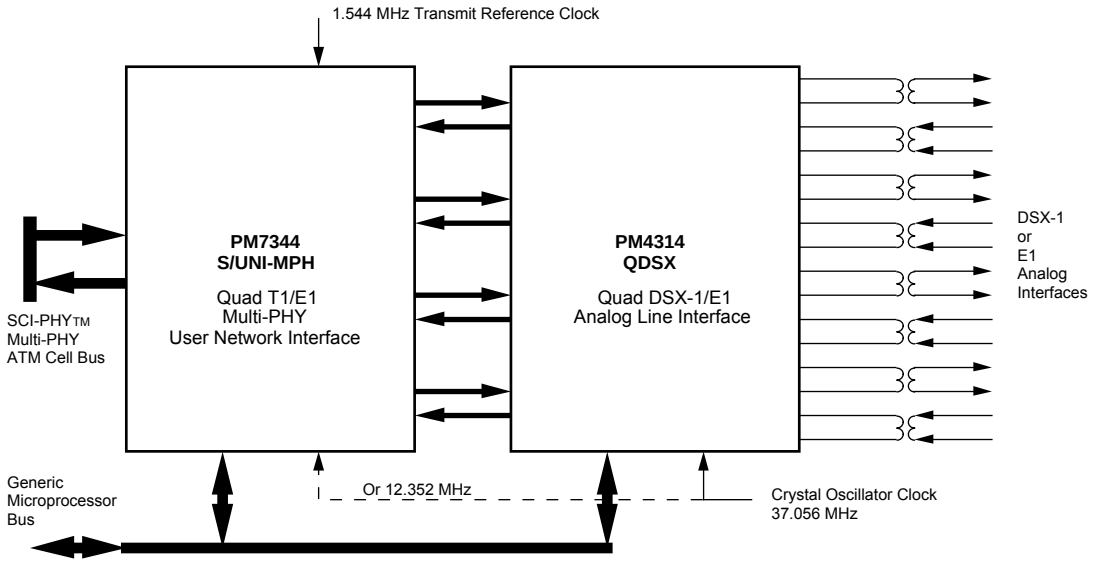
28. ATM Forum, Level 1, V2.00 - “An ATM PHY Data Path Interface”, February 1994.

29. ATM Forum, Level 2, V0.8 - “UTOPIA, An ATM-PHY Interface Specification”, April 1995.

30. PMC-Sierra, Inc., “(SCI-PHY™) SATURN Compliant Interface For ATM PHY Devices”, Issue 2, July 1994.

4 APPLICATION EXAMPLES

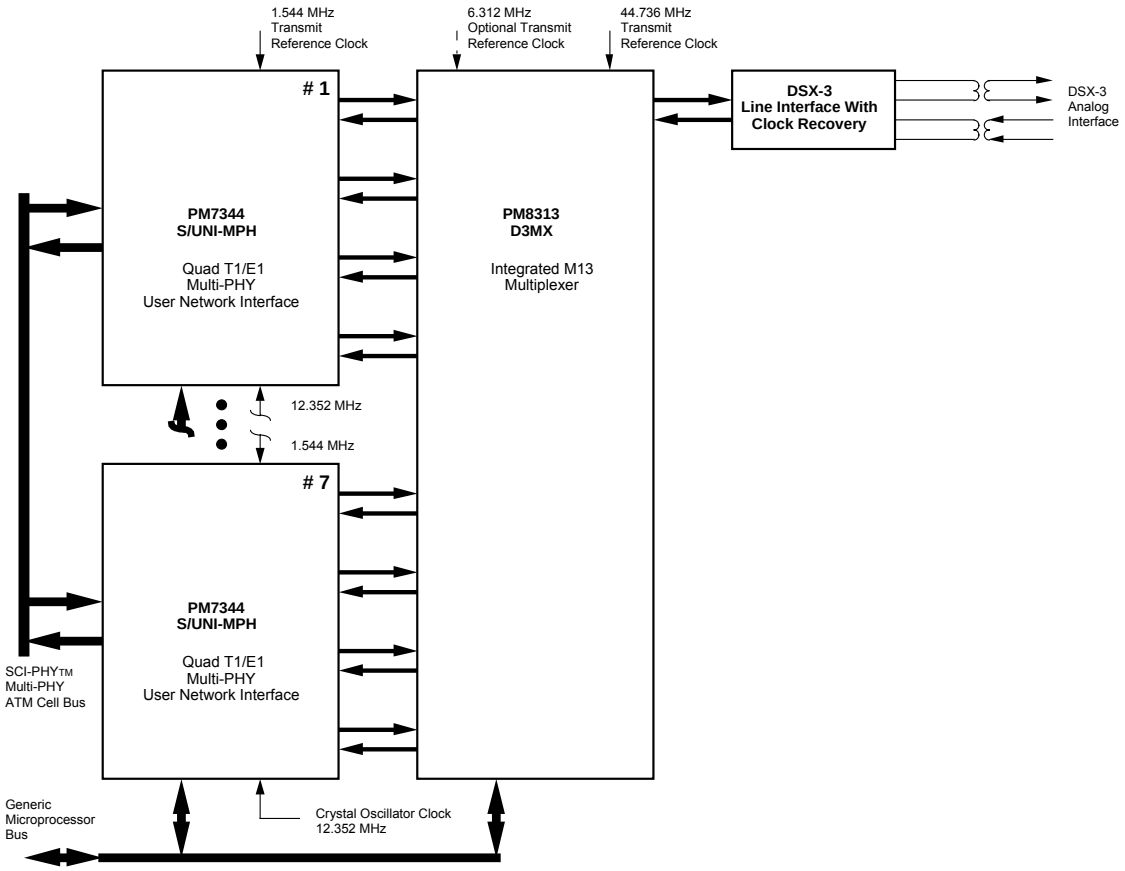
Figure 1 - Example 1. T1 or E1 Multi-PHY ATM UNI



Example 1 shows the PM7344 S/UNI-MPH used with the PM4314 QDSX to implement a quad T1/E1 UNI where the DS1 or E1 signals are presented on DSX-1 or E1 electrical interfaces.

In this example, the DSX-1 or E1 line interface functions are provided by the QDSX and the DS1 or E1 framing functions are provided by the S/UNI-MPH. Note that many other standard DSX-1 or E1 line interface devices are also compatible with the S/UNI-MPH. The S/UNI-MPH also provides the ATM cell processing functions associated with the PHY layer, including the implementation of a SCI-PHY multi-PHY interface to the ATM layer device(s). The combination of the QDSX device with the S/UNI-MPH allows both ANSI/ITU compliant DSX-1/E1 analog signals and ATM Forum UNI 3.1 and ITU G.804 compliant DS1/E1 digital signals to be processed. The UNI 3.1 and G.804 specifications define ATM cell mappings for a variety of transmission formats, including the 1.544 Mbit/s DS1 and the 2.048 Mbit/s E1 formats.

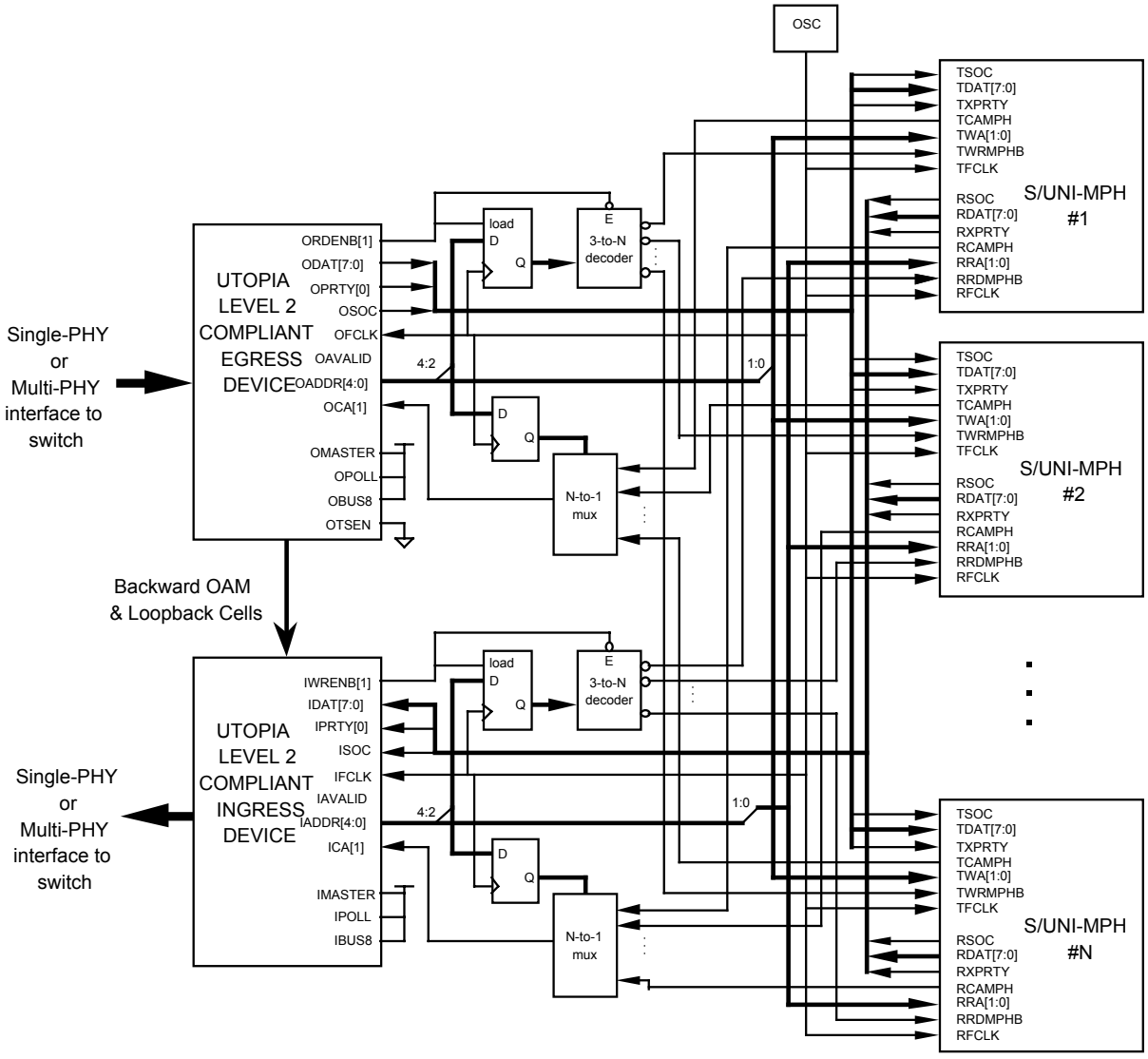
Figure 2 - Example 2. DS3 Port Carrying Multiplexed T1 or E1 ATM UNI Signals



Example 2 shows seven PM7344 S/UNI-MPH devices used with a PM8313 D3MX device and a generic DSX-3 LIU device being used to implement a DS3 port where the DS3 carries a multiplex of DS1 (or E1) UNI signals.

In this example, each S/UNI-MPH provides four duplex DS1 signals to the D3MX device which, in turn, performs the asynchronous multiplex and demultiplex function required to map these into a DS3 signal. The D3MX may use the traditional M23 format or may use the C-bit parity format when performing this multiplex. Note that the D3MX may also be configured for G.747 multiplexing of three E1 signals into each of the seven DS2 signals within the overall DS3 signal. Many generic DSX-3 line interface unit devices may be used with the D3MX to implement a DSX-3 electrical interface on the high speed line side of such a system. Each S/UNI-MPH device implements the T1 or E1 UNI function for four T1 or E1 streams. The seven S/UNI-MPH devices may be serviced by a common ATM layer device through a shared (SCI-PHY™) multi-PHY bus.

Figure 3 - Example 3. Multi-PHY Addressing Application



Example 3 shows N (where N is a number from 1 to 8) PM7344 S/UNI-MPH devices used with UTOPIA Level 2 compliant ingress and egress devices.

The S/UNI-MPH supports PHY address polling by sampling the two least significant address bits (RRA[1:0] and TWA[1:0]) and generating the cell available status for the selected PHY entity. It also holds the last state of RRA[1:0] and TWA[1:0] before the assertion of RRDMPHB and TWRMPHB, respectively, thus latching the PHY address resolved by the polling process. The only support logic is that required to select between the S/UNI-MPH devices.

Note that the oscillator can be at any frequency less than or equal to 25 MHz. For the DS-1 case the data rate is 1.536 Mbits/s (1.544 Mbits/s * 192 payload bits per frame / 193 bits per frame) for each DS-1 port. Thus, the aggregate throughput is less than 6.144 Mbyte/s with 32 DS-1 ports; therefore, the clock oscillator frequency can be as low as 6.5 MHz.

5 BLOCK DIAGRAM

Figure 4 - Normal Operating Mode

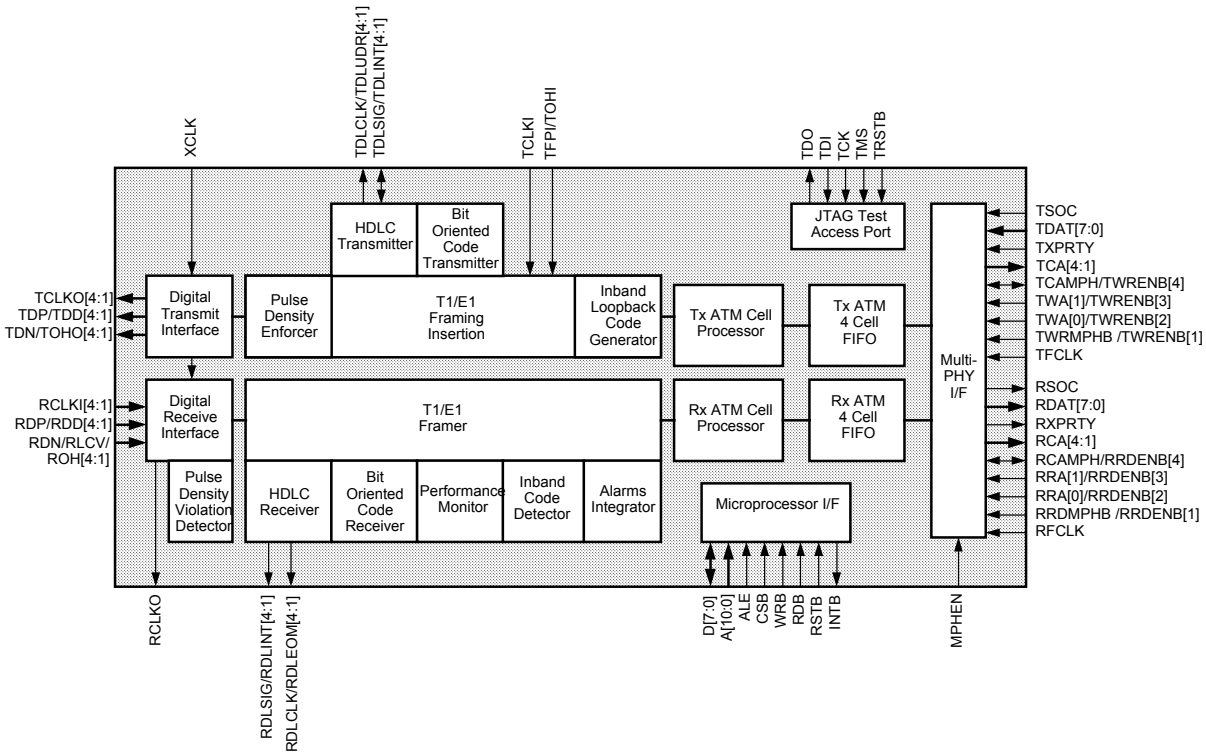
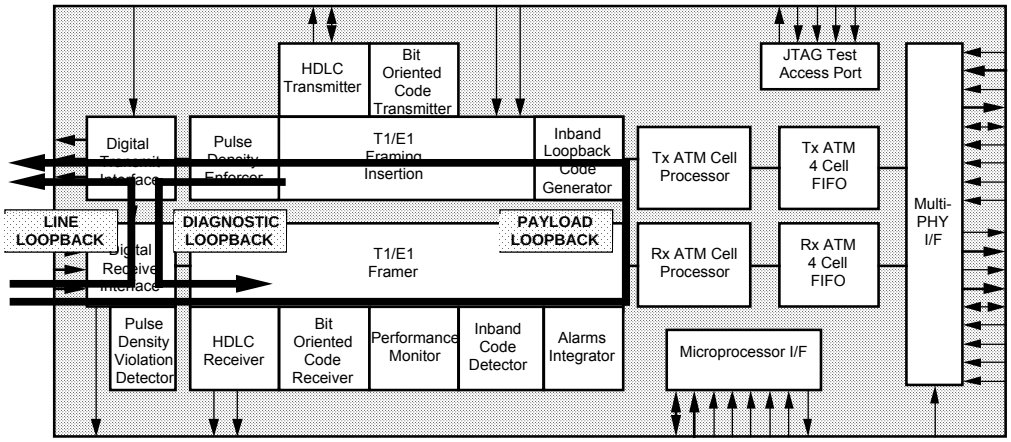


Figure 5 - Loopback Modes



6 DESCRIPTION

The PM7344 SATURN Quad T1/E1 Multi-PHY User Network Interface (S/UNI-MPH) is a monolithic integrated circuit that implements the T1/E1 processing and ATM mapping functions for four 1.544 Mbit/s or 2.048 Mbit/s ATM User Network Interfaces. It can also be used in conjunction with external framing devices, to implement ATM user network interfaces for other bit rates. For example, a quad J2 (6.312 Mbit/s) interface can be realized with four external J2 framers and a single S/UNI-MPH. It is fully compliant with both ANSI and ITU requirements and ATM Forum UNI specifications. The S/UNI-MPH is software configurable, allowing feature selection without changes to external wiring.

On the receive side, when configured for T1 processing, the S/UNI-MPH recovers clock and data and can be configured to frame to either of the common DS-1 signal formats; SF or ESF. Clock recovery may also be bypassed. The S/UNI-MPH also supports detection of various alarm conditions such as loss of signal, pulse density violation, red alarm, yellow alarm, and AIS alarm. The S/UNI-MPH detects and indicates the presence of yellow and AIS patterns and also integrates yellow, red, and AIS alarms as per industry specifications.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, line code violations, and loss of frame events is provided. The S/UNI-MPH also detects the presence of in-band loopback codes, ESF bit oriented codes, and detects and terminates HDLC messages on the ESF data link.

On the receive side, when configured for E1 processing, the S/UNI-MPH recovers clock and data and can be configured to frame to a basic G.704 2048 kbit/s signal or also frame to the signalling multiframe alignment signal and the CRC multiframe alignment signal. Clock recovery may also be bypassed.

The S/UNI-MPH also supports detection of various alarm conditions such as loss of signal, loss of frame, loss of signalling multiframe, loss of CRC multiframe, and reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and timeslot 16 alarm indication signal. The S/UNI-MPH detects and indicates the presence of remote alarm and AIS patterns and also integrates red and AIS alarms as per industry specifications.

Performance monitoring with accumulation of CRC-4 errors, far end block errors, framing bit errors, and line code violation is provided. The S/UNI-MPH also detects and terminates HDLC messages on a data link. The data link may be extracted from timeslot 16 or may be extracted from the national bits.

For both T1 and E1 configurations, the S/UNI-MPH interprets the received frame alignment and extracts the transmission format payload which carries the received ATM cell payload.

The S/UNI-MPH frames to the ATM payload using cell delineation. HCS error correction is optionally provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled.

Valid, assigned cells are written to a four cell FIFO buffer. These cells are read from the FIFO using a synchronous 8 bit wide datapath interface with a cell-based handshake. Counts of received ATM cell headers that are errored and uncorrectable, those that are errored and correctable and all passed cells are accumulated independently for performance monitoring purposes. A multi-PHY interface allows the four receive FIFOs (one for each T1 or E1 port) to be serviced via a single 8 bit wide bus.

On the transmit side, when configured for T1 processing, the S/UNI-MPH generates framing for SF and ESF DS1 formats. The S/UNI-MPH can also generate in-band loopback codes, ESF bit oriented codes, and transmit HDLC messages on the ESF data link.

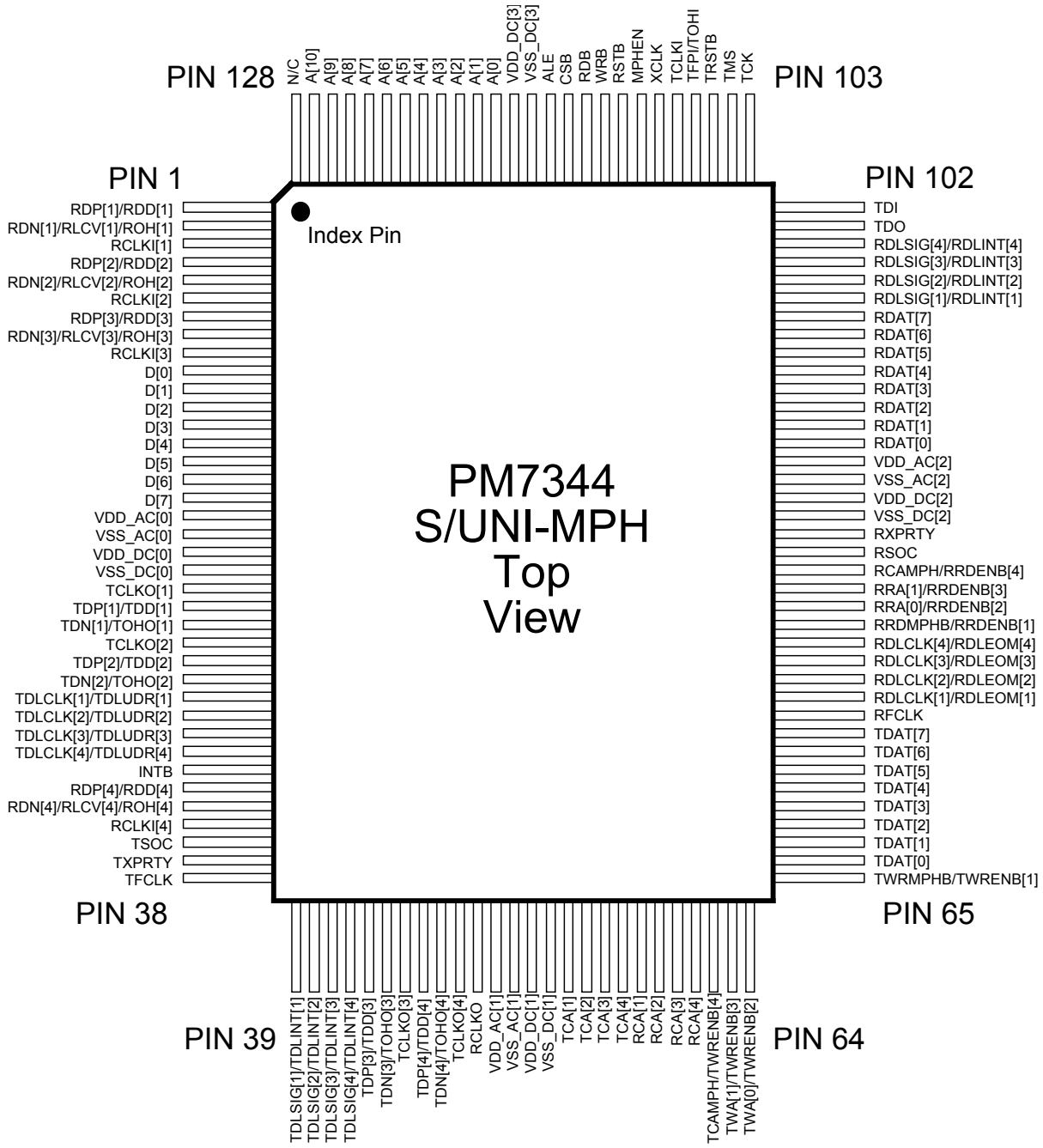
On the transmit side, when configured for E1 processing, the S/UNI-MPH generates framing for a basic G.704 2048 kbit/s signal. The signalling multiframe alignment signal may be optionally inserted and the CRC multiframe structure may be optionally inserted. HDLC messages on a data link can be transmitted. The data link may be inserted into timeslot 16 or may be inserted into the national bits.

For both T1 and E1 configurations, the S/UNI-MPH generates the transmitted frame and inserts the transmit ATM cell payload into the transmission format payload appropriately.

ATM cells are written to an internal programmable-length 4-cell FIFO using a synchronous 8 bit wide datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell. The S/UNI-MPH generates of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed. A multi-PHY interface allows the four transmit FIFOs (one for each T1 or E1 port) to be serviced via a single 8 bit wide bus.

The S/UNI-MPH is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. The S/UNI-MPH also provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.

7 PIN DIAGRAM



8 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
RDP[4] RDP[3] RDP[2] RDP[1]/	Input		Receive Digital Positive Line Pulse (RDP). This signal is available when the S/UNI-MPH is configured to receive dual-rail formatted data. The RDP input can be enabled for either RZ or NRZ waveforms. When enabled for NRZ, RDP may be enabled to be sampled on the rising or falling edge of RCLKI. When enabled for RZ, clock is recovered from the RDP and RDN inputs.
RDD[4] RDD[3] RDD[2] RDD[1]		33 7 4 1	Receive Digital Data (RDD). When the S/UNI-MPH is configured to receive single-rail data or when the T1/E1 framers are bypassed, this signal contains the receive data stream. RDD may be enabled to be sampled on the rising or falling edge of RCLKI.

Pin Name	Type	Pin No.	Function
RDN[4] RDN[3] RDN[2] RDN[1]/	Input		Receive Digital Negative Line Pulse (RDN). This signal is available when the S/UNI-MPH is configured to receive dual-rail formatted data. The RDN input can be enabled for either RZ or NRZ waveforms. When enabled for NRZ, RDN may be enabled to be sampled on the rising or falling edge of RCLKI. When enabled for RZ, clock is recovered from the RDP and RDN inputs.
RLCV[4] RLCV[3] RLCV[2] RLCV[1]/		34 8 5 2	Receive Line Code Violation Indication (RLCV). When the S/UNI-MPH is configured to receive single-rail data, this signal contains line code violation indications that are detected by the upstream line interface unit (LIU). RLCV may be enabled to be sampled on the rising or falling edge of RCLKI.
ROH[4] ROH[3] ROH[2] ROH[1]			Receive Overhead Mask (ROH). When the S/UNI-MPH is configured to bypass the T1/E1 framers, this signal indicates the framing overhead in the receive stream, thus allowing the S/UNI-MPH to provide a user network interface for arbitrary bit rates (such as the 6.312 Mbit/s J2 rate). ROH may be configured to be active high or active low, and may be enabled to be sampled on the rising or falling edge of RCLKI.
RCLKI[4] RCLKI[3] RCLKI[2] RCLKI[1]	Input	35 9 6 3	Receive Line Clock Input (RCLKI). This signal is the externally recovered line clock that may be enabled to sample the RDP and RDN inputs on its rising or falling edge when the input format is enabled for dual-rail NRZ; or to sample the RDD and RLCV/ROH inputs on its rising or falling edge when the input format is enabled for single-rail, or when the T1/E1 framers are bypassed. RCLKI must operate at frequencies less than or equal to 25 MHz.

Pin Name	Type	Pin No.	Function
RCLKO	Output	49	Receive Clock Output (RCLKO). This signal is recovered from the RDP and RDN inputs (if the input format is dual-rail RZ), or from the RCLKI input (if the input format is NRZ or if the T1/E1 framers are bypassed). Any one of the four sets of RDP/RDN or RCLKI signals may be selected as the source of RCLKO using internal registers.
RDLSIG[4] RDLSIG[3] RDLSIG[2] RDLSIG[1]/	Output	100 99 98 97	Receive Data Link Signal (RDLSIG). The RDLSIG signal is available on this pin when the internal HDLC receiver (RFDL) is disabled from use. When the S/UNI-MPH is configured to receive T1-ESF formatted data, RDLSIG contains the data stream extracted from the facility data link; when the S/UNI-MPH is configured to receive T1-SF formatted data, the RDLSIG output is held low; when the S/UNI-MPH is configured to receive E1 formatted data, RDLSIG contains the data stream extracted from timeslot 16 or a data stream made up of any combination of the national bits. RDLSIG is updated on the falling edge of RDLCLK.
RDLINT[4] RDLINT[3] RDLINT[2] RDLINT[1]			Receive Data Link Interrupt (RDLINT). The RDLINT signal is available on this pin when RFDL is enabled. RDLINT goes high when an event occurs which changes the status of the HDLC receiver.

Pin Name	Type	Pin No.	Function
RDLCLK[4] RDLCLK[3] RDLCLK[2] RDLCLK[1]/	Output	78 77 76 75	Receive Data Link Clock (RDLCLK). The RDLCLK signal is available on this pin when the internal HDLC receiver (RFDL) is disabled from use. RDLCLK is used to process the data stream contained on RDLSIG. When the S/UNI-MPH is configured to receive T1-SF formatted data, or when the T1/E1 framers are bypassed, RDLCLK is held low. In all other formats the rising edge of RDLCLK can be used to sample the data on RDLSIG.
RDLEOM[4] RDLEOM[3] RDLEOM[2] RDLEOM[1]			Receive Data Link End of Message (RDLEOM). The RDLEOM signal is available on this pin when RFDL is enabled. RDLEOM goes high when the last byte of a received sequence is read from the RFDL FIFO buffer, or when the FIFO buffer is overrun.
TDLSIG[4] TDLSIG[3] TDLSIG[2] TDLSIG[1]/	I/O	42 41 40 39	Transmit Data Link Signal (TDLSIG). The TDLSIG signal is input on this pin when the internal HDLC transmitter (XFDL) is disabled from use. TDLSIG is the source for the data stream to be inserted into the data link. When the S/UNI-MPH is configured to transmit T1-ESF formatted data, TDLSIG contains the data stream inserted in the facility data link; when the S/UNI-MPH is configured to transmit T1-SF formatted data, TDLSIG is ignored; when the S/UNI-MPH is configured to transmit E1 formatted data, TDLSIG contains the data stream inserted in timeslot 16 or a data stream inserted in any combination of the national bits. TDLSIG is sampled on the rising edge of TDLCLK.
TDLINT[4] TDLINT[3] TDLINT[2] TDLINT[1]			Transmit Data Link Interrupt (TDLINT). The TDLINT signal is output on this pin when XFDL is enabled. TDLINT goes high when the last data byte written to the XFDL has been set up for transmission and processor intervention is required to either write control information to end the message, or to provide more data.

Pin Name	Type	Pin No.	Function
TDLCLK[4] TDLCLK[3] TDLCLK[2] TDLCLK[1]/	Output	31 30 29 28	Transmit Data Link Clock (TDLCLK). The TDLCLK signal is available on this pin when the internal HDLC transmitter (XFDL) is disabled from use. The rising edge of TDLCLK is used to sample the data stream contained on the TDLSIG input. When the S/UNI-MPH is configured to transmit T1-SF formatted data, or when the T1/E1 framers are bypassed, TDLCLK is held low.
TDLUDR[4] TDLUDR[3] TDLUDR[2] TDLUDR[1]			Transmit Data Link Underrun (TDLUDR). The TDLUDR signal is available on this pin when XFDL is enabled. TDLUDR goes high when the processor has failed to service the TDLINT interrupt before the transmit buffer is emptied.
TCLKO[4] TCLKO[3] TCLKO[2] TCLKO[1]	Output	48 45 25 22	Transmit Clock Output (TCLKO). The TDP, TDN, and TDD outputs may be enabled to be updated on the rising or falling edge of TCLKO. TCLKO is the transmit clock that is adequately jitter and wander free in absolute terms to permit an acceptable transmission signal to be generated. Depending on the configuration of the S/UNI-MPH, TCLKO may be derived from TCLKI, RCLKO, or XCLK, with or without jitter attenuation.
TDP[4] TDP[3] TDP[2] TDP[1]/	Output	46 43 26 23	Transmit Digital Positive Line Pulse (TDP). This signal is available on the pin when the S/UNI-MPH is configured to transmit dual-rail data. The TDP signal can be formatted for either RZ or NRZ waveforms, and can be enabled to be updated on the rising or falling edge of TCLKO.
TDD[4] TDD[3] TDD[2] TDD[1]			Transmit Digital Data (TDD). This signal is available on the pin when the S/UNI-MPH is configured to transmit single-rail data, or when the T1/E1 framers are bypassed. The TDD signal may be enabled to be updated on the rising or falling edge of TCLKO.

Pin Name	Type	Pin No.	Function
TDN[4] TDN[3] TDN[2] TDN[1]/	Output	47 44 27 24	Transmit Digital Negative Line Pulse (TDN). This signal is available on the pin when the S/UNI-MPH is configured to transmit dual-rail data. The TDN signal can be formatted for either RZ or NRZ waveforms, and can be enabled to be updated on the rising or falling edge of TCLKO. When configured for single-rail T1 or E1 data, TDN is unused.
TOHO[4] TOHO[3] TOHO[2] TOHO[1]			Transmit Overhead Mask Output (TOHO). When the S/UNI-MPH is configured to bypass the T1/E1 transmit framers, this signal indicates the placeholder bit positions for the framing overhead in the transmit stream. TOHO may be connected to an external framer device to provide a user network interface for arbitrary bit rates or for the J2 rate (for which TOHO is specially conditioned to operate with the Transwitch JT2F framer). The ATM cell stream can be configured to be byte aligned to TOHO (in which case the number of TCLKO periods between active TOHO edges must be divisible by eight). TOHO may be configured to be active high or active low, and may be enabled to be updated on the rising or falling edge of TCLKO.
TCLKI	Input	107	Transmit Clock Input (TCLKI). This signal provides the transmit direction timing (when the S/UNI-MPH is not loop timed). The S/UNI-MPH may be configured to ignore the TCLKI input and utilize XCLK instead. The default requirement is for TCLKI to be a 1.544 MHz clock for T1 or a 2.048 MHz clock for E1. For arbitrary bit rates, TCLKI must be less than or equal to 25 MHz.

Pin Name	Type	Pin No.	Function
TFPI	Input	106	Transmit Frame Position (TFPI). This signal provides the transmit frame position indication for the four T1/E1 framers. TFPI can be used in applications where the transmit frames must be aligned to a common reference. In these applications, TFPI is activated for one clock period every 193 (T1) or 256 (E1) TCLKI periods (or multiple thereof). If such alignment is not required, TFPI may be tied low. TFPI may be configured to be active high or active low, and may be enabled to be sampled on the rising or falling edge of TCLKI.
TOHI			Transmit Overhead Mask Input (TOHI). This signal identifies the placeholder bits in the transmit stream for arbitrary bit rate interfaces. A delayed version of TOHI appears on the four TOHO outputs. Downstream framing insertion devices overwrite the placeholder bit positions with overhead specific to a particular frame format (for example the 6.312 Mbit/s J2 format). TOHI may be configured to be active high or active low, and may be enabled to be sampled on the rising or falling edge of TCLKI.
XCLK/	Input	108	Crystal Clock Input (XCLK). This signal provides timing for the T1 or E1 framer portion of the S/UNI-MPH. Depending on the configuration of the S/UNI-MPH, XCLK must be nominally 24x or 8x the nominal line rate. The 8x clock is used by the clock recovery digital phase locked loop and the T1/E1 framer, while the 24x clock is used by the jitter attenuator in the S/UNI-MPH. This clock may be tied low if the T1/E1 framers are bypassed. The default requirement is for XCLK to be a 37.056 MHz clock for T1 or a 49.152 MHz clock for E1.
VCLK			Vector Clock (VCLK). The VCLK signal is used during S/UNI-MPH production test to verify internal functionality.

Pin Name	Type	Pin No.	Function
MPHEN	Input	109	Multiphy Enable (MPHEN). This input selects the configuration of the receive and transmit cell interfaces. When MPHEN is high, the cell interfaces are configured for multi-phy addressing and signals TWRMPHB, TWA[1:0], TCAMPH, RRDMPHB, RRA[1:0], and RCAMPH are active. When MPHEN is low, the cell interfaces are configured for direct phy selection and signals TWRENB[4:1] and RRDENB[4:1] are active.
RFCLK	Input	74	Receive FIFO Read Clock (RFCLK). This signal is used to read ATM cells from the receive FIFOs. RFCLK must cycle at a 25 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflow.

Pin Name	Type	Pin No.	Function
RRDMPHB	Input	79	Receive Multi-Phy Read Enable (RRDMPHB). The RRDMPHB signal is available on this pin when input MPHEN is high. RRDMPHB is used to initiate reads from the receive FIFOs. When sampled low using the rising edge of RFCLK, a byte is read from the receive FIFO selected by the RRA[1:0] address bus (if one is available) and output on bus RDAT[7:0]. When sampled high using the rising edge of RFCLK, no read is performed and RDAT[7:0] and RSOC are tristated. RRDMPHB must operate in conjunction with RFCLK to access the FIFOs at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert RRDMPHB at anytime it is unable to accept another byte.
RRDENB[1]			Receive Read Enable PHY #1 (RRDENB[1]). The RRDENB[1] signal is available on this pin when input MPHEN is low. RRDENB[1] is used to initiate reads from the receive FIFO of PHY #1. When sampled low using the rising edge of RFCLK (and the remaining three RRDENBs remain high), a byte is read from PHY #1's synchronous FIFO and output on bus RDAT[7:0] if one is available. When sampled high using the rising edge of RFCLK, no read is performed and RDAT[7:0] and RSOC are tristated. RRDENB[1] must operate in conjunction with RFCLK to access the FIFOs at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert RRDENB[1] at anytime it is unable to accept another byte.

Pin Name	Type	Pin No.	Function
RRA[0]	Input	80	Receive Read Address LSB (RRA[0]). The RRA[0] signal is available on this pin when input MPHEN is high. RRA[0] is used (along with RRA[1]) to select the FIFO (and hence port) that is read from using the RRDMPHB signal. RRA[0] is sampled on the rising edge of RFCLK together with RRDMPHB.
RRDENB[2]			Receive Read Enable PHY #2 (RRDENB[2]). The RRDENB[2] signal is available on this pin when input MPHEN is low. RRDENB[2] is used to initiate reads from the receive FIFO of PHY #2. When sampled low using the rising edge of RFCLK (and the remaining three RRDENBs remain high), a byte is read from PHY #2's synchronous FIFO and output on bus RDAT[7:0] if one is available. When sampled high using the rising edge of RFCLK, no read is performed and RDAT[7:0] and RSOC are tristated. RRDENB[2] must operate in conjunction with RFCLK to access the FIFOs at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert RRDENB[2] at anytime it is unable to accept another byte.

Pin Name	Type	Pin No.	Function
RRA[1]	Input	81	Receive Read Address MSB (RRA[1]). The RRA[1] signal is available on this pin when input MPHEN is high. RRA[1] is used (along with RRA[0]) to select the FIFO (and hence port) that is read from using the RRDMPHB signal. RRA[1] is sampled on the rising edge of RFCLK together with RRDMPHB.
RRDENB[3]			Receive Read Enable PHY #3 (RRDENB[3]). The RRDENB[3] signal is available on this pin when input MPHEN is low. RRDENB[3] is used to initiate reads from the receive FIFO of PHY #3. When sampled low using the rising edge of RFCLK (and the remaining three RRDENBs remain high), a byte is read from PHY #3's synchronous FIFO and output on bus RDAT[7:0] if one is available. When sampled high using the rising edge of RFCLK, no read is performed and RDAT[7:0] and RSOC are tristated. RRDENB[3] must operate in conjunction with RFCLK to access the FIFOs at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert RRDENB[3] at anytime it is unable to accept another byte.

Pin Name	Type	Pin No.	Function
RCAMPH	I/O	82	Receive Multi-Phy Cell Available (RCAMPH). The RCAMPH signal is output on this pin when input MPHEN is high. This signal indicates when a cell is available in the receive FIFO for the port selected by RRA[1:0]. RCAMPH can be configured to be deasserted when either zero or four bytes remain in the selected/addressed FIFO. RCAMPH will thus transition low on the rising edge of RFCLK after the 53rd or 48th byte has been output if the PHY being polled is the same as the PHY in use .
RRDENB[4]			Receive Read Enable PHY #4 (RRDENB[4]). The RRDENB[4] signal is input on this pin when input MPHEN is low. RRDENB[4] is used to initiate reads from the receive FIFO of PHY #4. When sampled low using the rising edge of RFCLK (and the remaining three RRDENBs remain high), a byte is read from PHY #4's synchronous FIFO and output on bus RDAT[7:0] if one is available. When sampled high using the rising edge of RFCLK, no read is performed and RDAT[7:0] and RSOC are tristated. RRDENB[4] must operate in conjunction with RFCLK to access the FIFOs at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert RRDENB[4] at anytime it is unable to accept another byte.
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7]	Tristate Output	89 90 91 92 93 94 95 96	Receive Cell Data Bus (RDAT[7:0]). This bus carries the ATM cell octets that are read from the selected receive FIFO. RDAT[7:0] is updated on the rising edge of RFCLK and is tristated when RRDENB[n]/RRDMPHB is high.

Pin Name	Type	Pin No.	Function
RXPRTY	Tristate Output	84	Receive Parity (RXPRTY). This signal indicates the parity of the RDAT[7:0] bus. Odd or even parity selection can be made using a register. RXPRTY is updated on the rising edge of RFCLK and is tristated when RRDENB[4:1]/RRDMPHB is high.
RSOC	Tristate Output	83	Receive Start of Cell (RSOC). This signal marks the start of cell on the RDAT[7:0] bus. When RSOC is high, the first octet of the cell is present on the RDAT[7:0] stream. RSOC is updated on the rising edge of RFCLK and is tristated when RRDENB[4:1]/RRDMPHB is high.
RCA[4] RCA[3] RCA[2] RCA[1]	Output	61 60 59 58	Receive Cell Available (RCA[4:1]). These output signals indicate when a cell is available in the receive FIFO for the corresponding port. RCA[4:1] can be configured to be deasserted when either zero or four bytes remain in the FIFO. RCA[4:1] will thus transition low on the rising edge of RFCLK after the 53rd or 48th byte has been output.
TFCLK	Input	38	Transmit FIFO Write Clock (TFCLK). This signal is used to write ATM cells to the four cell transmit FIFOs. TFCLK cycles at a 25 MHz or lower instantaneous rate. A complete 53 octet cell must be written to the FIFO before being inserted in the transmit stream. Idle/unassigned cells are inserted when a complete cell is not available.
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7]	Input	66 67 68 69 70 71 72 73	Transmit Cell Data Bus (TDAT[7:0]). This bus carries the ATM cell octets that are written to the selected transmit FIFO. TDAT[7:0] is sampled on the rising edge of TFCLK and is considered valid only when TWRENB[n]/TWRMPHB is simultaneously asserted.

Pin Name	Type	Pin No.	Function
TXPRTY	Input	37	Transmit bus parity (TXPRTY). This signal indicates the parity of the TDAT[7:0] bus. Odd or even parity selection can be made using a register. TXPRTY is sampled on the rising edge of TFCLK and is considered valid only when TWRENB[n]/TWRMPHB is simultaneously asserted. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are inserted in the transmit stream, so the TXPRTY input may be unused.
TWRMPHB	Input	65	Transmit Multi-Phy Write Enable (TWRMPHB). The TWRMPHB signal is available on this pin when input MPHEN is high. This active low input is used to initiate writes to the transmit FIFOs. When sampled low using the rising edge of TFCLK, the byte on TDAT[7:0] is written into the transmit FIFO selected by the TWA[1:0] address bus. When sampled high using the rising edge of TFCLK, no write is performed. A complete 53 octet cell must be written to the transmit FIFO before it is inserted into the transmit stream. Idle/unassigned cells are inserted when a complete cell is not available.
TWRENB[1]			Transmit Write Enable PHY #1 (TWRENB[1]). The TWRENB[1] signal is available on this pin when input MPHEN is low. TWRENB[1] is used to initiate writes to the transmit FIFO of PHY #1. When sampled low using the rising edge of TFCLK (and the remaining three TWRENBs remain high), a byte is written to PHY #1's synchronous FIFO. When sampled high using the rising edge of TFCLK, no write is performed. TWRENB[1] must operate in conjunction with TFCLK to access the FIFOs at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert TWRENB[1] at anytime it is unable to provide another byte.

Pin Name	Type	Pin No.	Function
TWA[0]	Input	64	Transmit Write Address LSB (TWA[0]). The TWA[0] signal is available on this pin when input MPHEN is high. TWA[0] is used (along with TWA[1]) to select the FIFO (and hence port) that is written to using the TWRMPHB signal. TWA[0] is sampled on the rising edge of TFCLK together with TWRMPHB.
TWRENB[2]			Transmit Write Enable PHY #2 (TWRENB[2]). The TWRENB[2] signal is available on this pin when input MPHEN is low. TWRENB[2] is used to initiate writes to the transmit FIFO of PHY #2. When sampled low using the rising edge of TFCLK (and the remaining three TWRENBs remain high), a byte is written to PHY #2's synchronous FIFO. When sampled high using the rising edge of TFCLK, no write is performed. TWRENB[2] must operate in conjunction with TFCLK to access the FIFOs at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert TWRENB[2] at anytime it is unable to provide another byte.

Pin Name	Type	Pin No.	Function
TWA[1]	Input	63	Transmit Write Address MSB (TWA[1]). The TWA[1] signal is available on this pin when input MPHEN is high. TWA[1] is used (along with TWA[0]) to select the FIFO (and hence port) that is written to using the TWRMPHB signal. TWA[1] is sampled on the rising edge of TFCLK together with TWRMPHB.
TWRENB[3]			Transmit Write Enable PHY #3 (TWRENB[3]). The TWRENB[3] signal is available on this pin when input MPHEN is low. TWRENB[3] is used to initiate writes to the transmit FIFO of PHY #3. When sampled low using the rising edge of TFCLK (and the remaining three TWRENBs remain high), a byte is written to PHY #3's synchronous FIFO. When sampled high using the rising edge of TFCLK, no write is performed. TWRENB[3] must operate in conjunction with TFCLK to access the FIFOs at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert TWRENB[3] at anytime it is unable to provide another byte.

Pin Name	Type	Pin No.	Function
TCAMPH	I/O	62	Transmit Multi-Phy Cell Available (TCAMPH). The TCAMPH signal is output on this pin when input MPHEN is high. This signal indicates when a cell is available in the transmit FIFO for the port selected by TWA[1:0]. When high, TCAMPH indicates that the corresponding transmit FIFO is not full and a complete cell may be written. When TCAMPH goes low, it can be configured to indicate either that the corresponding transmit FIFO is near full and can accept no more than four writes or that the corresponding transmit FIFO is full. TCAMPH will thus transition low on the rising edge of TFCLK on which the 52nd or 48th byte is sampled if the PHY being polled is the same as the PHY in use. To reduce FIFO latency, the FIFO depth at which TCAMPH indicates "full" can be set to one, two, three or four cells.
TWRENB[4]			Transmit Write Enable PHY #4 (TWRENB[4]). The TWRENB[4] signal is input on this pin when input MPHEN is low. TWRENB[4] is used to initiate writes to the transmit FIFO of PHY #4. When sampled low using the rising edge of TFCLK (and the remaining three TWRENBs remain high), a byte is written to PHY #4's synchronous FIFO. When sampled high using the rising edge of TFCLK, no write is performed. TWRENB[4] must operate in conjunction with TFCLK to access the FIFOs at a high enough instantaneous rate as to avoid FIFO overflows. The ATM layer device may deassert TWRENB[4] at anytime it is unable to provide another byte.

Pin Name	Type	Pin No.	Function
TSOC	Input	36	Transmit Start of Cell (TSOC). This input marks the start of cell on the TDAT[7:0] bus. When TSOC is high, the first octet of the cell is present on the TDAT[7:0] stream. It is not necessary for TSOC to be present at each cell. An interrupt may be generated if TSOC is high during any byte other than the first byte. TSOC is sampled on the rising edge of TFCLK
TCA[4] TCA[3] TCA[2] TCA[1]	Output	57 56 55 54	Transmit Cell Available (TCA[4:1]). These output signals indicate when a cell is available in the transmit FIFO for the corresponding port. When high, TCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. When TCA goes low, it can be configured to indicate either that the corresponding transmit FIFO is near full and can accept no more than four writes or that the corresponding transmit FIFO is full. TCA[4:1] will thus transition low on the rising edge of TFLCK on which the 52nd or 48th byte is sampled. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells.
INTB	Output	32	Active low Open-Drain Interrupt (INTB). This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources, including the internal HDLC transceivers. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.
CSB	Input	113	Active low Chip Select (CSB). This signal must be low to enable S/UNI-MPH register accesses. If CSB is not used, (RDB and WRB determine register reads and writes) then it should be tied to an inverted version of RSTB.

Pin Name	Type	Pin No.	Function
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	17 16 15 14 13 12 11 10	Bidirectional Data Bus (D[7:0]). This bus is used during S/UNI-MPH read and write accesses.
RDB	Input	112	Active low Read Enable (RDB). This signal is pulsed low to enable a S/UNI-MPH register read access. The S/UNI-MPH drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
WRB	Input	111	Active low Write Strobe (WRB). This signal is pulsed low to enable a S/UNI-MPH register write access. The D[7:0] bus is clocked into the addressed register on the rising edge of WRB while CSB is low.
ALE	Input	114	Address Latch Enable (ALE). This signal latches the address bus contents, A[10:0], when low, allowing the S/UNI-MPH to be interfaced to a multiplexed address/data bus. When ALE is high, the address latches are transparent. ALE has an integral pull-up resistor.
RSTB	Input	110	Active low Reset (RSTB). This signal is set low to asynchronously reset the S/UNI-MPH. RSTB is a Schmitt-trigger input with an integral pull-up resistor.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	Input	117 118 119 120 121 122 123 124 125 126 127	Address Bus (A[10:0]). This bus selects specific registers during S/UNI-MPH register accesses.

Pin Name	Type	Pin No.	Function
TCK	Input	103	Test Clock (TCK). This signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	104	Test Mode Select (TMS). This signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	102	Test Data Input (TDI). This signal carries test data into the S/UNI-MPH via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate Output	101	Test Data Output (TDO). This signal carries test data out of the S/UNI-MPH via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	105	Active low Test Reset (TRSTB). This signal provides an asynchronous S/UNI-MPH test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence. Note that if not used, TRSTB must be connected to the RSTB input.
VDD_AC[2] VDD_AC[1] VDD_AC[0]	Power	88 50 18	Pad Ring Power (VDD_AC[2:0]). These pins should be connected to a well decoupled +5 V DC in common with VDD_DC[3:0]
VDD_DC[3] VDD_DC[2] VDD_DC[1] VDD_DC[0]	Power	116 86 52 20	DC Power (VDD_DC[3:0]). These pins should be connected to a well decoupled +5 V DC in common with VDD_AC[2:0].
VSS_AC[2] VSS_AC[1] VSS_AC[0]	Ground	87 51 19	Pad Ring Ground (VSS_AC[2:0]). These pins should be connected to GND in common with VSS_DC[3:0].

Pin Name	Type	Pin No.	Function
VSS_DC[3] VSS_DC[2] VSS_DC[1] VSS_DC[0]	Ground	115 85 53 21	DC Ground (VSS_DC[3:0]). These pins should be connected to GND in common with VSS_AC[2:0].

Notes on Pin Description:

1. VDD_DC[3:0] and VSS_DC[3:0] are the +5 V and ground connections, respectively, for the core circuitry and the DC drive of the output pads of the device. VDD_AC[2:0] and VSS_AC[2:0] are the +5 V and ground connections, respectively, for the AC switching of the pad ring circuitry of the device. These power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate. There is no low impedance connection within the S/UNI-MPH between the core, and pad ring supply rails. Failure to properly make these connections may result in improper operation or damage to the device.

2. Inputs RSTB, TMS, TDI, TRSTB and ALE have integral pull-up resistors.

3. The TDLSIG/TDLINT[4:1] pins have integral pull-up resistors and default to being inputs after a reset.

4. D[7:0], TCLKO[4:1], RCLKO, RDAT[7:0], RCA[4:1], RXPRTY, RSOC, TCA[4:1], and the TCAMPH and RCAMPH bidirectionals have 4mA drive capability. All other outputs and bidirectionals have 2mA drive capability.

5. All inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.

6. When an internal RFDL is enabled, the RDLINT[x] output goes high:

   1) when the number of bytes specified in the RFDL Interrupt Status/Control Register have been received on the data link,

   2) immediately on detection of RFDL FIFO buffer overrun,

   3) immediately on detection of end of message,

   4) immediately on detection of an abort condition, or,

   5) immediately on detection of the transition from receiving all ones to flags.

The interrupt is cleared at the start of the next RFDL Data Register read that results in an empty FIFO buffer. This is independent of the FIFO buffer fill level for which the interrupt is programmed. If there is still data remaining in the buffer, RDLINT will remain high. An interrupt due to a RFDL FIFO buffer overrun condition is not cleared on a RFDL Data Register read but on a RFDL Status Register read. The RDLINT output can always be forced low by disabling the RFDL (setting the EN bit in the RFDL Configuration Register to logic 0, or by disabling the internal HDLC receiver in the S/UNI-MPH Receive Data Link Configuration Register), or by forcing the RFDL to terminate reception (setting the TR bit in the RFDL Configuration Register to logic 1).

The RDLINT output may be forced low by disabling the interrupts with the RFDL Interrupt Status/Control Register. However, the internal interrupt latch is not cleared, and the state of this latch can still be read through the RFDL Interrupt Status/Control Register.

7. The RDLEOM[x] output goes high:

   1) immediately on detection of RFDL FIFO buffer overrun,

   2) when the data byte written into the RFDL FIFO buffer due to an end of message condition is read,

   3) when the data byte written into the RFDL FIFO buffer due to an abort condition is read, or,

   4) when the data byte written into the RFDL FIFO buffer due to the transition from receiving all ones to flags is read.

   RDLEOM[x] is set low by reading the RFDL Status Register or by disabling the RFDL.

8. For each TDLUDR[x] output:

   The TDLUDR[x] output goes high when the processor is unable to service the TDLINT[x] request for more data before a specific time-out period. This period is dependent upon the frequency of TDLCLK:

   1) for a TDLCLK frequency of 4 kHz (ESF FDL at the full 4 kHz rate), the time-out is 1.0 ms;

   2) for a TDLCLK frequency of 2 kHz (half the ESF FDL), the time-out is 2.0 ms;

9 FUNCTIONAL DESCRIPTION

9.1 Digital Receive Interface (DRIF)

The Digital Receive Interface provides control over the various input options available on the multifunctional digital receive pins RDP/RDD and RDN/RLCV/ROH. When configured for dual-rail input, the multifunctional pins become the RDP and RDN inputs. These inputs can be enabled to receive either return-to-zero (RZ) or non-return-to-zero (NRZ) signals; the NRZ input signals can be sampled on either the rising or falling edge of RCLKI. When the interface is configured for single-rail input, the multifunctional pins become the RDD and RLCV inputs, which can be sampled on either the rising or falling RCLKI edge. Finally, when the T1/E1 framers are bypassed, the multifunction pins become the RDD and ROH inputs, which support arbitrary bit rate interfaces such as the 6.312 Mbit J2 rate. The S/UNI-MPH contains internal logic that allows it to be interfaced directly to the Transwitch JT2F framer device. A single S/UNI-MPH along with four JT2Fs is used to implement a quad J2 user network interface.

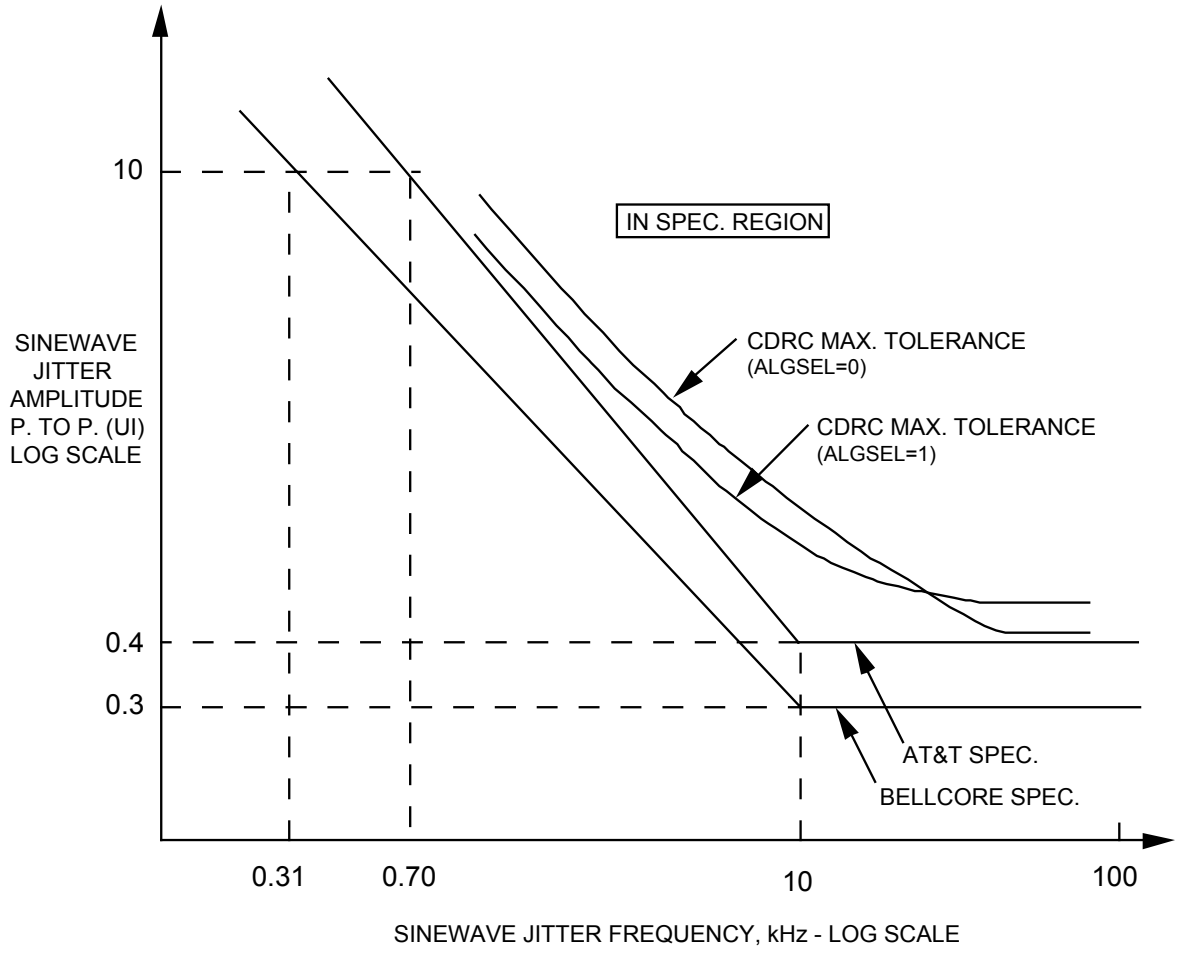
Clock and Data Recovery

The Clock and Data Recovery function is contained in the DRIF block and is active when clock recovery is enabled for T1 or E1 interfaces in the dual-rail input configuration. The CDRC provides clock and data recovery, B8ZS/HDB3 decoding, bipolar violation detection, and loss of signal detection. It recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop and recovers the NRZ data. Loss of signal is declared after exceeding a programmed threshold of 10, 31, 63, or 175 consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is removed after the occurrence of a single line pulse. An alternate loss of signal removal criteria requires that minimum pulse density requirements be satisfied before loss of signal is removed. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns.

The input jitter tolerance for T1 interfaces complies with the Bellcore Document TA-TSY-000170 and with the AT&T specification TR 62411. The tolerance is measured with a QRSS sequence (2^{20}-1 with 14 zero restriction). The CDRC block provides two algorithms for clock recovery that result in differing jitter tolerance characteristics. The first algorithm (when the ALGSEL register bit is logic 0) provides good low frequency jitter tolerance, but the high frequency tolerance is close to the TR 62411 limit. The second algorithm (when ALGSEL is logic 1) provides much better high frequency jitter tolerance, approaching 0.5UIpp (Unit Intervals peak-to-peak), at the expense of the low frequency

tolerance; the low frequency tolerance of the second algorithm is approximately 80% of that of the first algorithm. The T1 jitter tolerance with ALGSEL set to 1 and to 0 is shown in the following illustration.

Figure 6 - T1 Jitter Tolerance Specification



The input jitter tolerance for E1 interfaces complies with ITU-T Recommendation G.823. The tolerance is measured with a 2^{15}-1 sequence. The E1 jitter tolerance is with ALGSEL set to 1 and to 0 is shown in the following illustrations.

Figure 7 - E1 Jitter Tolerance Specification (ALGSEL = 1)

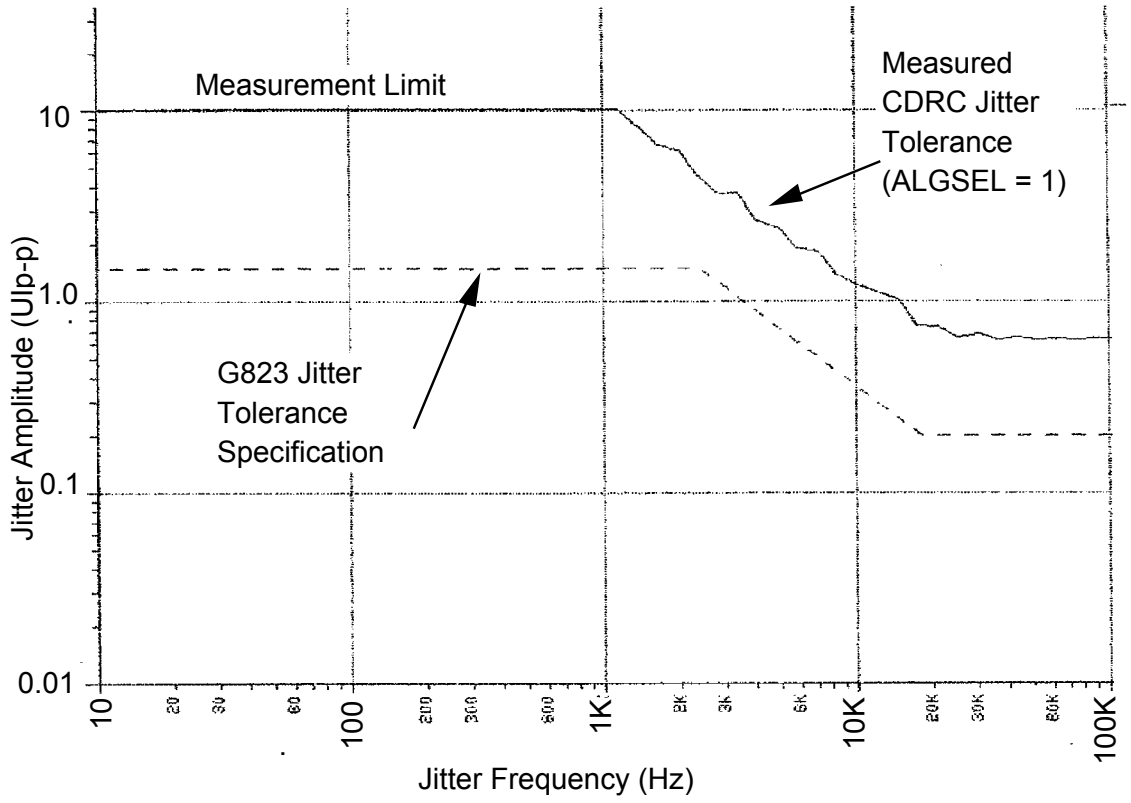
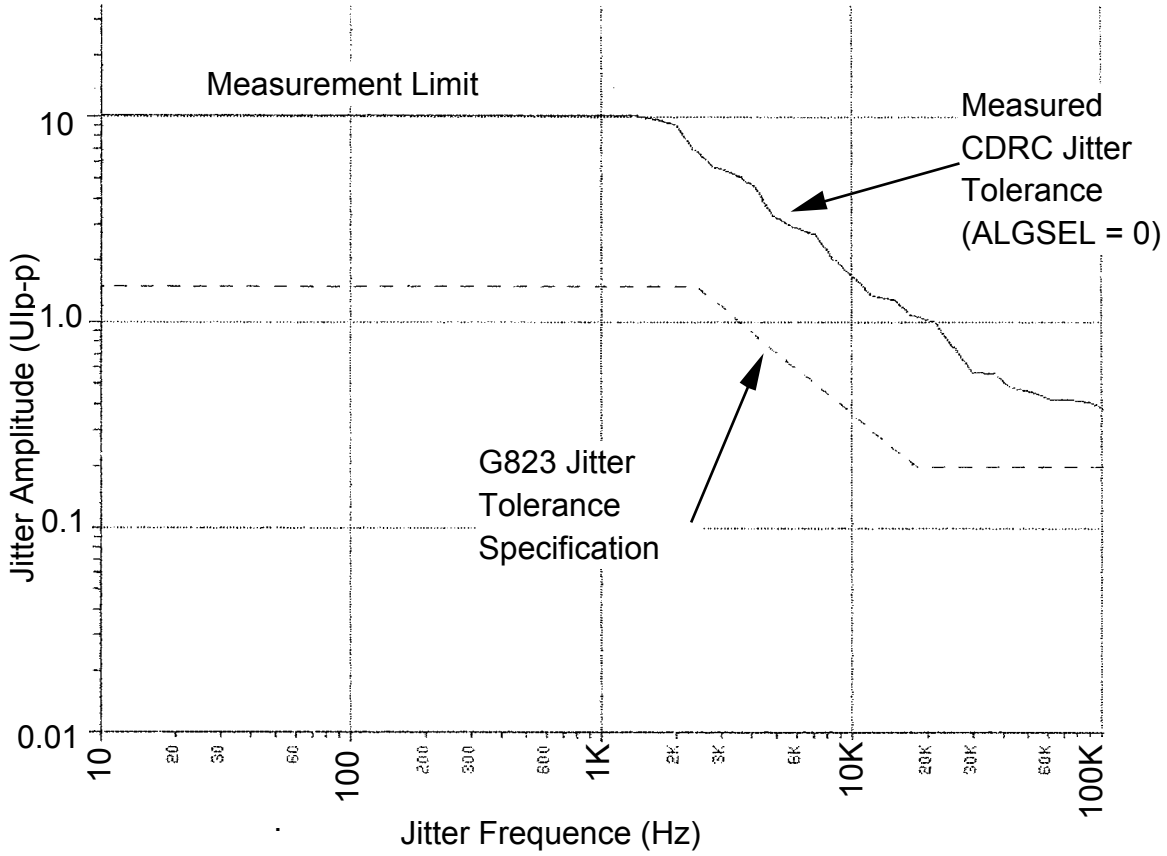


Figure 8 - E1 Jitter Tolerance Specification (ALGSEL = 0)



9.2 Pulse Density Violation Detector (PDVD)

The Pulse Density Violation Detection function is provided by the PDVD block. This block detects pulse density violations of the ANSI T1.403 requirement that there be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). The PDVD also detects periods of 16 consecutive zeros in the incoming data. Pulse density violation detection is provided through an internal register bit. An interrupt is generated to signal a 16 consecutive zero event or a change of state on the pulse density violation indication.

9.3 T1/E1 Framer (FRMR)

The framing function is provided by the FRMR block. This block searches for the framing bit position in the incoming data stream. It searches for the framing bit pattern for the following T1 frame formats: SF, and ESF. When searching for frame, the FRMR examines each of the 193 (SF), or each of the 4*193 (ESF) framing bit candidates. For the E1 frame format, the FRMR searches for frame alignment and CRC multiframe alignment in the incoming stream.

The time required to find frame alignment to an error-free PCM stream containing randomly distributed channel data (i.e. each bit in the channel data has a 50% probability of being 1 or 0) is dependent upon the framing format. For SF, the FRMR determines frame alignment within 4.4ms, 99 times out of 100. For ESF the FRMR determines frame alignment within 15ms, 99 times out of 100. For E1 formatted signals, the FRMR determines frame alignment within 1ms, 99 times out of 100.

When the FRMR has found T1 frame alignment, the incoming data is continuously monitored for framing bit errors, CRC-6 error events (ESF only), and severe errored framing events. The FRMR also detects loss of frame, based on a selectable ratio of framing bit errors.

When the FRMR has found E1 frame alignment, the incoming data is monitored for frame alignment signal bit errors. Upon detecting CRC multiframe alignment, the FRMR monitors the incoming data for CRC multiframe alignment pattern errors, and CRC-4 errors. The FRMR also detects loss of frame, and loss of CRC multiframe, based on user-selectable criteria.

The FRMR extracts the yellow alarm signal bits in T1-SF and T1-ESF framing formats. The FRMR extracts and debounces the remote alarm indication signal in the E1 framing format.

9.4 Alarm Integrator (ALMI)

The Alarm Integration function is provided by the ALMI block. This block detects the presence of T1 yellow, red, and AIS Carrier Fail Alarms (CFA) in SF and ESF formats. The block also detects the presence of E1 red CFA and AIS CFA. The alarm detection and integration is compatible with the specifications defined in ANSI T1.403-1989, TR-TSY-000191, and Q.516.

For T1 formats, the ALMI block declares the presence of yellow CFA when the yellow pattern has been received for 425 ms (± 50 ms); the yellow CFA is removed when the yellow pattern has been absent for 425 ms (± 50 ms). The presence of red CFA is declared when an out-of-frame condition has been present for 2.55 sec (± 40 ms); the red CFA is removed when the out-of-frame

condition has been absent for 16.6 sec (± 500 ms). The presence of AIS CFA is declared when an out-of-frame condition and all-ones in the data stream have been present for 1.5 sec (±100 ms); the AIS CFA is removed when the AIS condition has been absent for 16.8 sec (±500 ms).

For E1 formats, the ALMI block declares the presence of red CFA when an out-of-frame condition has been present for 104 ms (±6 ms); the red CFA is removed when the out-of-frame condition has been absent for 104 ms (±6 ms). The presence of AIS CFA is declared when an out-of-frame condition and all-ones in the data stream have been present for 104 ms (±6 ms); the AIS CFA is removed when the AIS condition has been absent for 104 ms (±6 ms).

CFA alarm detection algorithms operate in the presence of a random 10^{-3} bit error rate.

The ALMI also indicates the presence or absence of the T1 yellow, red, and AIS alarm signal conditions over 40 ms, 40ms, and 60 ms intervals, respectively, allowing an external microprocessor to integrate the alarm conditions via software with any user-specific algorithms. Alarm indication is provided through internal register bits.

9.5 T1 Inband Loopback Code Detector (IBCD)

The T1 Inband Loopback Code Detection function is provided by the IBCD block. This block detects the presence of either of two programmable loopback code sequences, ACTIVATE and DEACTIVATE, in either framed or unframed T1 data streams. The inband code sequences are expected to be overwritten by the framing bit in framed data streams. Each code sequence is defined as the repetition of the programmed code in the PCM stream for at least 5.1 seconds. The code sequence detection and timing is compatible with the specifications defined in T1.403, TA-TSY-000312, and TR-TSY-000303. ACTIVATE and DEACTIVATE code indication is provided through internal register bits. An interrupt is generated to indicate when either code status has changed.

9.6 Performance Monitor Counters (PMON)

The Performance Monitor Counters function is provided by the PMON block. For a T1 data stream, the PMON accumulates CRC-6 error events, frame synchronization bit error events, line code violation events, and loss of frame events, or optionally, change of frame alignment (COFA) events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second).

For an E1 data stream, the PMON accumulates CRC-4 error events, frame synchronization bit error events, line code violation events, and far end block

error events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second).

When the transfer clock signal is applied, the PMON transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed.

Generation of the transfer clock within the S/UNI-MPH is performed by writing to any counter register location. The holding register addresses are contiguous to facilitate polling operations.

9.7 T1 Bit Oriented Code Detector (RBOC)

The Bit Oriented Code detection function is provided by the RBOC block. This block detects the presence of 63 of the possible 64 bit oriented codes transmitted in the facility data link channel in T1-ESF framing format, as defined in ANSI T1.403 and in TR-TSY-000194.

Bit oriented codes are received on the facility data link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated at least 10 times. The RBOC can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times.

Valid BOCs are indicated through an internal status register. The BOC bits are set to all ones (111111) if no valid code has been detected. An interrupt is generated to signal when a detected code has been validated, or optionally, when a valid code is removed (i.e. the BOC bits go to all ones idle state).

9.8 HDLC Receiver (RFDL)

The HDLC Receiver function is provided by the RFDL block. The RFDL is a microprocessor peripheral used to receive LAPD/HDLC frames on the ESF facility data link (FDL) for T1 interfaces, or on timeslot 16 or the National use bits of timeslot 0 for E1 interfaces.

The RFDL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives frame data, and calculates the CRC-CCITT frame check sequence (FCS).

Received data is placed into a 4-level FIFO buffer. The Status Register contains bits which indicate overrun, end of message, flag detected, and buffered data available.

On end of message, the Status Register also indicates the FCS status and the number of valid bits in the final data byte. Interrupts are generated when one, two or three bytes (programmable via the RFDL configuration register) are stored in the FIFO buffer. Interrupts are also generated when the terminating flag sequence, abort sequence, or FIFO buffer overrun are detected.

When the internal HDLC receiver is disabled, the serial data extracted by the FRMR block is output on the RDLSIG[x] pin updated on the falling clock edge output on the RDLCLK[x] pin.

9.9 T1/E1 Framing Insertions (TRAN)

The Basic Transmitter function is provided by the TRAN block. The TRAN block inserts the T1-SF or T1-ESF framing for the 1.544 Mbit/s data stream or the E1 basic framing and CRC multiframe for the 2.048 Mbit/s data stream.

A data link is provided for T1- ESF and E1 framing formats. The TRAN interfaces to the XFDL and XBOC blocks to provide a variety of data link sources including bit oriented codes (T1-ESF format only) and LAPD messages. Support is provided for the transmission of framed or unframed inband code sequences (T1 format only) and transmission of AIS or yellow CFA signals for all formats.

The line code of the transmit data stream may be selected to be one of AMI, B8ZS, or HDB3.

9.10 T1 Inband Loopback Code Generator (XIBC)

The Inband Loopback Code Generator function is provided by the XIBC block. This block generates a stream of inband loopback codes to be inserted into a T1 data stream. The stream consists of continuous repetitions of a specific code and can be either framed or unframed. When the XIBC is enabled to generate a framed stream, the framing bit overwrites the inband code pattern. The contents of the code and its length are programmable from 3 to 8 bits. The XIBC interfaces directly to the TRAN Basic Transmitter block.

9.11 T1 Pulse Density Enforcer (XPDE)

The Pulse Density Enforcer function is provided by the XPDE block. Pulse density enforcement is enabled by a register bit within the XPDE.

This block monitors the transmit AMI-coded T1 stream, detecting when the stream is about to violate the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window. If a density violation is detected, the XPDE can be enabled to insert a logic 1 into the digital stream to ensure the resultant output no longer violates the pulse density requirement. When the XPDE is disabled from inserting logic 1s, the transmit stream from the TRAN is passed through unaltered.

9.12 T1 Bit Oriented Code Generator (XBOC)

The Bit Oriented Code Generator function is provided by the XBOC block. This block transmits 63 of the possible 64 bit oriented codes in the facility data link channel in T1-ESF framing format, as defined in ANSI T1.403.

Bit oriented codes are transmitted on the facility data link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. The transmitted bit oriented codes have priority over any data transmitted on the facility data link except for ESF yellow CFA. The code to be transmitted is programmed by writing the code register.

9.13 T1 HDLC Transmitter (T1 XFDL)

The HDLC Transmitter function is provided by the XFDL block. This block interfaces with the TRAN block. The XFDL is used under microprocessor or DMA control to transmit HDLC data frames in the facility data link for the T1-ESF frame format, or in timeslot 16 or the National bits of timeslot 0 for the E1 frame format.

The XFDL performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, idle, and abort sequence insertion. Data to be transmitted is provided on an interrupt-driven basis by writing to a double-buffered transmit data register. A CRC-CCITT frame check sequence is appended to the data frame, followed by idle flag sequences. If the transmit data register underflows, an abort sequence is automatically transmitted.

When enabled for use, the XFDL continuously transmits the flag character (01111110). Data bytes to be transmitted are written into the Transmit Data Register. After the parallel-to-serial conversion of each data byte, an interrupt is generated to signal the controller to write the next byte into the Transmit Data Register. After the last data frame byte is transmitted, the CRC word (if CRC insertion has been enabled), or a flag (if CRC insertion has not been enabled) is transmitted. The XFDL then returns to the transmission of flag characters.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort characters.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the Transmit Data Register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the TDLUDR signal. Optionally, the interrupt and underrun signals can be independently enabled to also generate an interrupt on the INTB output, providing a means to notify the controlling processor of changes in the XFDL operating status.

When the internal HDLC transmitter is disabled, the serial data to be transmitted in the facility data link or in timeslot 16 or timeslot 0 can be input on the TDLSIG[x] pin timed to the clock rate output on the TDLCLK[x] pin.

9.14 Digital Transmit Interface (DTIF)

The Digital Transmit Interface provides control over the various output options available on the multifunctional digital transmit pins TDP/TDD and TDN/TOHP. When configured for dual-rail output, the multifunctional pins become the TDP and TDN outputs. These outputs can be formatted as either return-to-zero (RZ) or non-return-to-zero (NRZ) signals and can be updated on either the rising or falling edge of TCLKO. When the interface is configured for single-rail output, or when the T1/E1 framers are bypassed, the multifunctional pins become the TDD and TOHO outputs, which can be enabled to be updated on either the rising or falling TCLKO edge. When the T1/E1 framers are bypassed, arbitrary bit rate interfaces, such as the 6.312 Mbit/s J2 rate may be supported.

9.15 Digital Jitter Attenuator

The Digital Jitter Attenuator (DJAT) function is contained in the DTIF block and is used to attenuate jitter in the transmit clock when required. The DJAT function is normally enabled if the S/UNI-MPH is loop-timed from RCLKO, or if the transmit clock (TCLKI) requires jitter attenuation before transmission. The block receives jittered data from the TRAN block and stores this data in a FIFO. The data emerges from the DJAT timed to the jitter attenuated clock, TCLKO.

The DJAT generates the jitter-free 1.544/2.048 MHz TCLKO clock by adaptively dividing the 24x XCLK input according to the phase difference between the generated TCLKO and the input data clock to DJAT (TCLKI or RCLKO). Phase variations in the input clock with a jitter frequency above 8.8 Hz (for the E1

format) or 6.6 Hz (for the T1 formats) are attenuated by 6 dB per octave of jitter frequency. Phase variations below these jitter frequencies are tracked by TCLKO.

Jitter Characteristics

The DJAT provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 28 UIpp of input jitter at jitter frequencies above 6 Hz for T1 interfaces or 9 Hz (for E1 interfaces). For jitter frequencies below 6/9 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In most applications DJAT will limit jitter tolerance at lower jitter frequencies only. The DJAT block meets the low frequency jitter tolerance requirements of AT&T TR 62411 for T1 interfaces, and ITU-T G.823 for E1 interfaces.

Outgoing jitter may be dominated by the generated residual jitter in cases where the incoming jitter is insignificant. This residual jitter is directly related to the use of the 24x clock for the digital phase locked loop.

For T1 interfaces, DJAT meets the jitter attenuation requirements of AT&T TR 62411. DJAT meets the implied jitter attenuation requirements for a TE or an NT1 specified in ANSI T1.408, and for a type II customer interface specified in ANSI T1.403.

For E1 interfaces, DJAT meets the jitter attenuation requirements of ITU-T Recommendations G.737, G.738, G.739, and G.742.

Jitter Tolerance

Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For DJAT, the input jitter tolerance is 29 Unit Intervals peak-to-peak (UIpp) for a T1 interface with a worst case frequency offset of 354 Hz. The input jitter tolerance is 35 UIpp for an E1 interface with a worst case frequency offset of 308 Hz. It is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK divided by 24 and that of the input data clock. These tolerances are shown in Figure 9 and Figure 10 below:

Figure 9 - T1 Jitter Tolerance

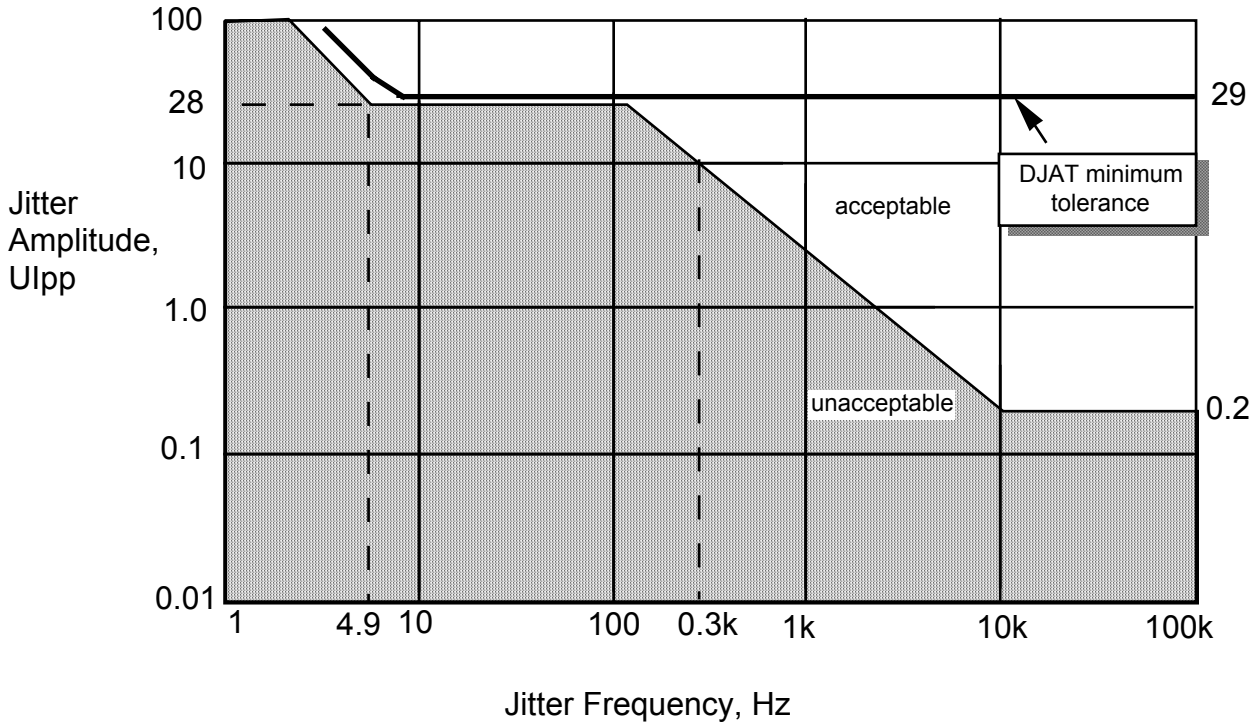
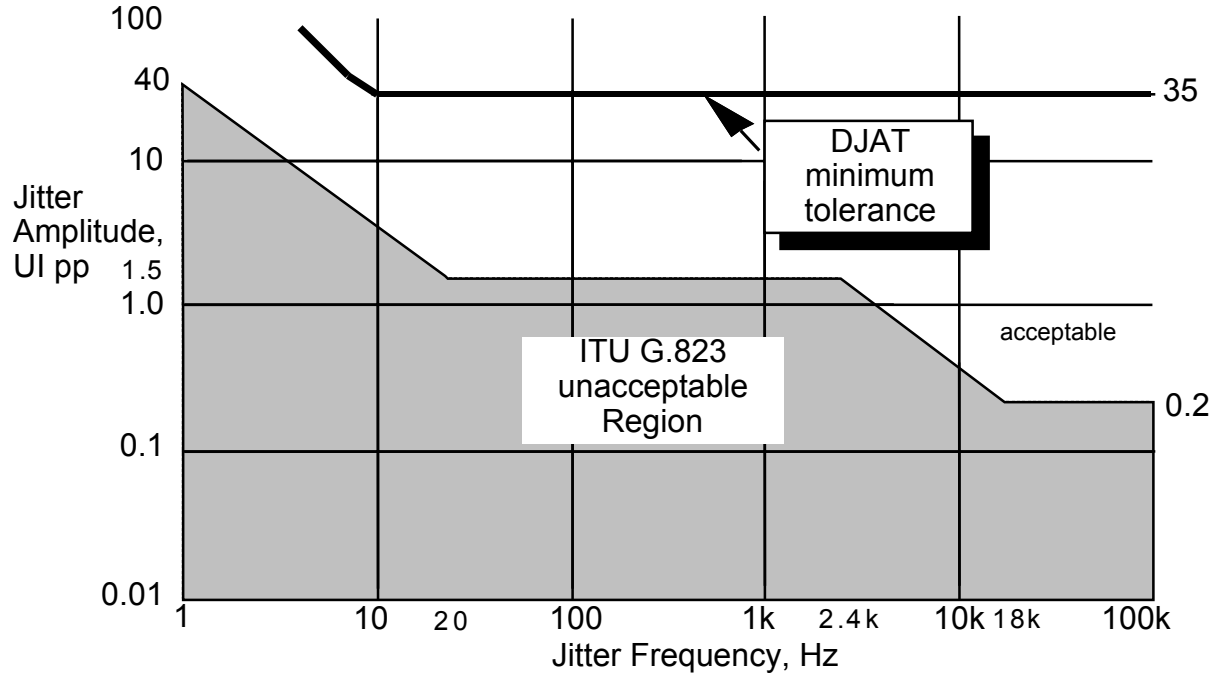


Figure 10 - E1 Jitter Tolerance



The accuracy of the XCLK frequency and that of the DJAT PLL reference input clock used to generate the jitter-free TCLKO have an effect on the minimum jitter tolerance. For T1 interfaces, the DJAT PLL reference clock accuracy can be ±200 Hz from 1.544 MHz, and the XCLK input accuracy can be ±100 ppm from 37.056 MHz. For E1 interfaces, the PLL reference clock accuracy can be ± 103 Hz from 2.048 MHz, and the XCLK input accuracy can be ±100 ppm from 49.152 MHz. The minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK/24 are shown in Figure 11 and Figure 12.

Figure 11 - DJAT Minimum Jitter Tolerance vs XCLK Accuracy (T1 Case)

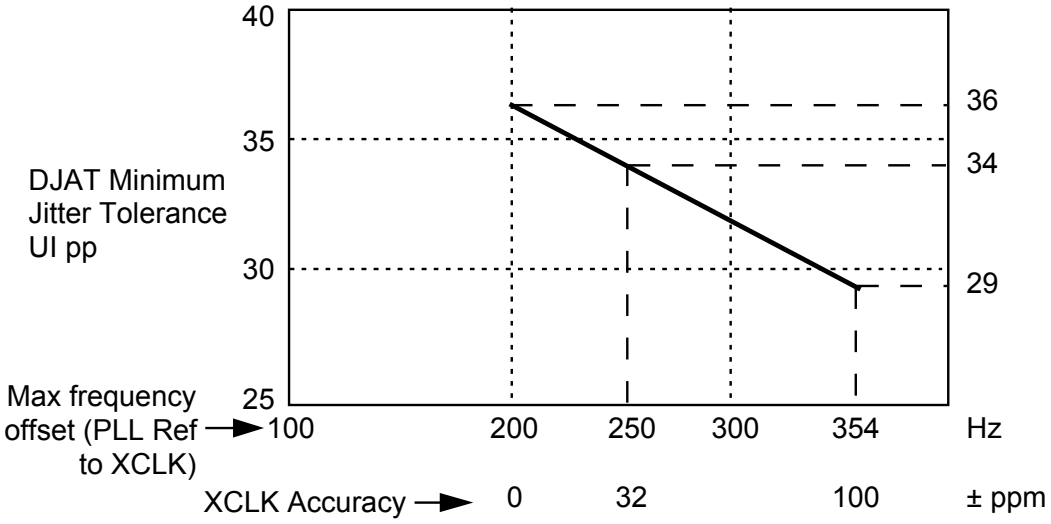
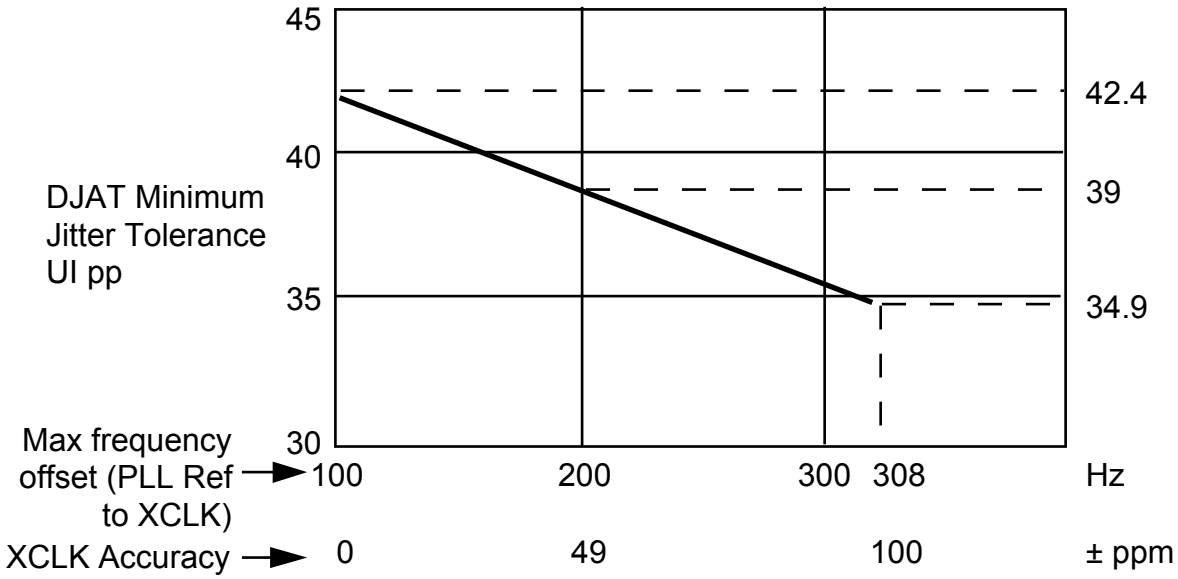


Figure 12 - DJAT Minimum Jitter Tolerance vs XCLK Accuracy (E1 Case)



Jitter Transfer

The output jitter for jitter frequencies from 0 to 6.6 Hz (for T1 interfaces) or from 0 to 8.8 Hz (for E1 interfaces) is no more than 0.1 dB greater than the input jitter, excluding the 0.042 UI residual jitter. Jitter frequencies above 6.6/8.8 Hz are

attenuated at a level of 6 dB per octave, as shown in Figure 13 and Figure 14 below:

Figure 13 - T1 Jitter Transfer

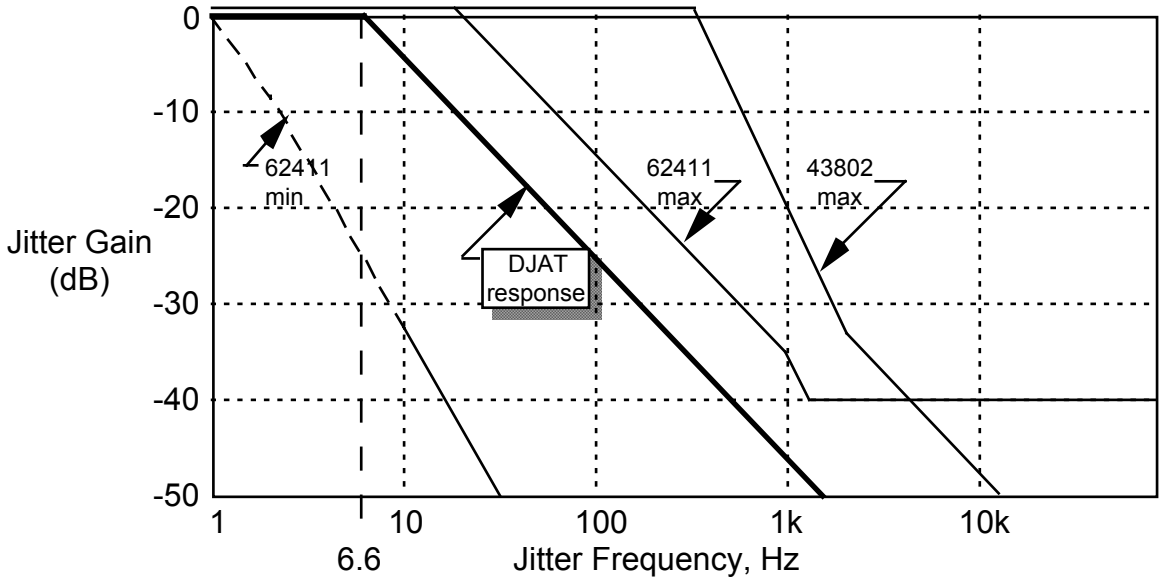
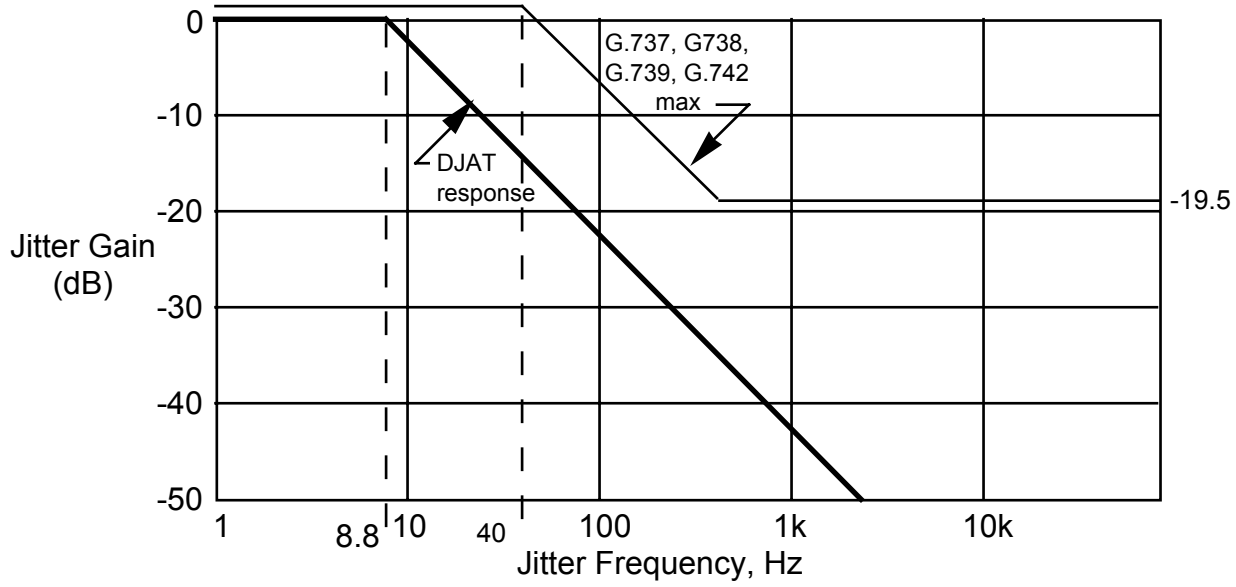


Figure 14 - E1 Jitter Transfer



9.16 Receive ATM Cell Processor (RXCP)

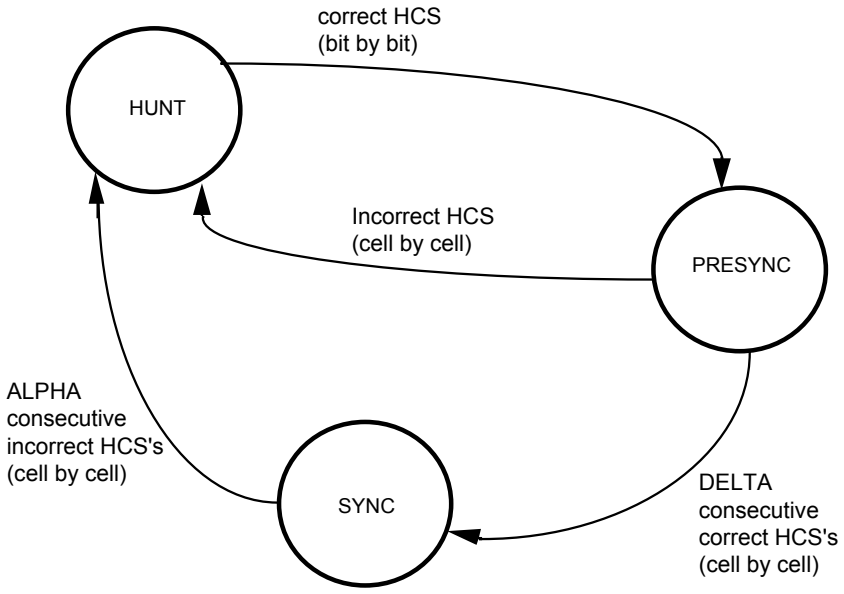
The Receive ATM Cell Processor (RXCP) Block integrates circuitry to support cell delineation, cell payload descrambling, header check sequence (HCS) verification and idle/unassigned cell filtering.

The RXCP cell delineates the framed T1 or E1 cell streams. Overhead bits (the framing bit for T1 interfaces, or timeslots 0 and 16 for E1 interfaces) are indicated by the FRMR block. Overhead bits in arbitrary rate interfaces are indicated by the ROHM input.

Cell delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the ATM cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries.

The RXCP performs a sequential bit by bit hunt for a correct HCS sequence. While performing this hunt, the cell delineation state machine is in the HUNT state. When a correct HCS is found, the RXCP locks on the particular cell boundary and enters the PRESYNC state. This state verifies that the previously detected HCS pattern was not a false indication. If the HCS pattern was a false indication then an incorrect HCS should be received within the next DELTA cells. At that point a transition back to the HUNT state is executed. If an incorrect HCS is not found in the PRESYNC state then a transition to the SYNC state is made. In this state synchronization is not relinquished until ALPHA consecutive incorrect HCS patterns are found. In such an event a transition is made back to the HUNT state. The state diagram of the cell delineation process is shown in Figure 15.

Figure 15 - Cell delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation method. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6 as recommended in ITU-T Recommendation I.432.

Loss of cell delineation (LCD) is detected by counting the number of incorrect cells while in the HUNT state. The counter value is stored in the RXCP LCD Count Threshold register. The threshold has a default value of 360 which results in an E1 format detection time of 77 ms, and a T1 format detection time of 100 ms.

The RXCP descrambles the cell payload field using the self synchronizing descrambler with a polynomial of $x^{43} + 1$. The cell header is not descrambled. Note that cell payload scrambling is optional in the S/UNI-MPH.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RXCP verifies the received HCS using the accumulation polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432.

The RXCP can be programmed to drop all cells containing an HCS error or to filter cells based on the HCS and/or the 4 octet cell header. Filtering according to a particular HCS and/or 4 octet header pattern is programmable through the

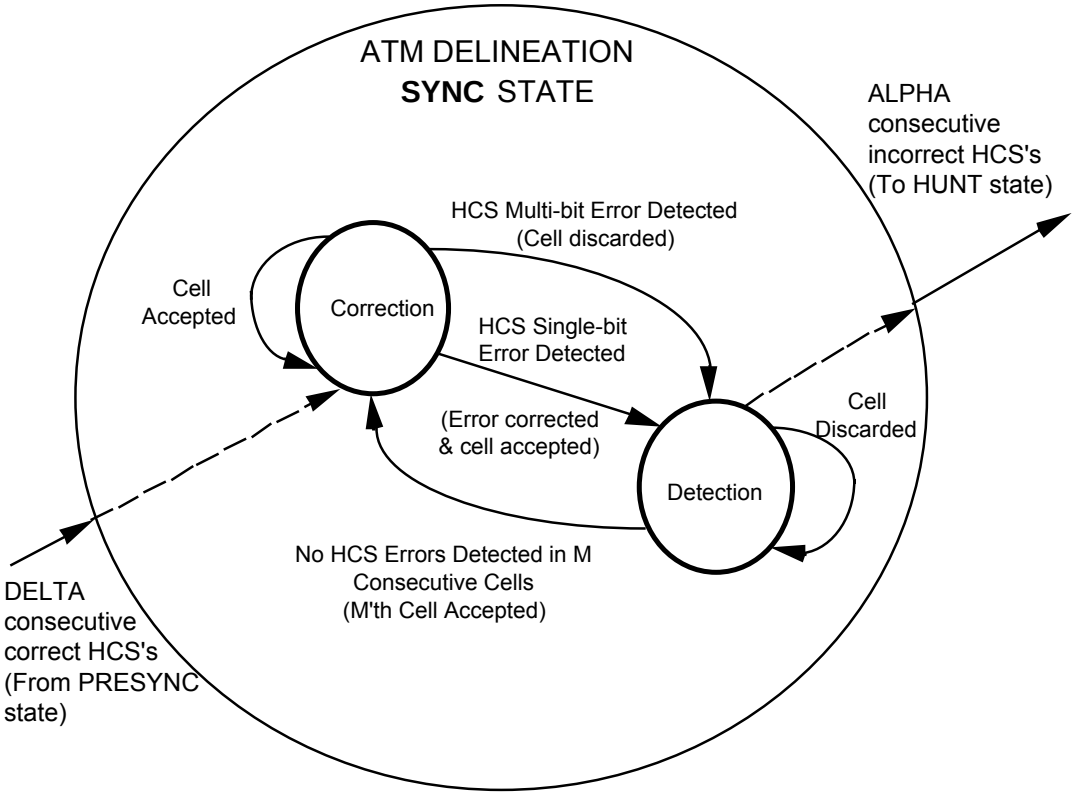
RXCP configuration/control registers. More precisely, filtering is performed when filtering is enabled or when HCS errors are found when HCS checking is enabled. Otherwise, all cells are passed on regardless of any error conditions. Cells are dropped if the HCS pattern is invalid or if the filtering 'Match Pattern' and 'Match Mask' registers are programmed with a certain blocking pattern. Idle cells are not automatically filtered. If they are required to be filtered, then that filtering criterion (i.e. the cell header pattern) must be programmed through the Idle/Unassigned Cell Pattern and Mask registers. For ATM cells, Idle/Unassigned cells are identified by the standardized header pattern of 'H00, 'H00, 'H00 and 'H01 in the first 4 octets followed by the valid HCS octet.

While the cell delineation state machine is in the SYNC state, the HCS verification circuit implements the state machine shown in figure 10.

In normal operation, the HCS verification state machine remains in the 'Correction' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single-bit errors are optionally corrected, and the resulting cell is passed to the FIFO. Upon detection of a single-bit error or a multi-bit error, the state machine transitions to the 'Detection' state.

A programmable hysteresis is provided when dropping cells based on HCS errors. When a cell with an HCS error is detected, the RXCP can be programmed to continue to discard cells until m (where m = 1, 2, 4, 8) cells are received with correct HCS. The mth cell is not discarded (see Figure 16). Note that the dropping of cells due to HCS errors only occurs while the cell delineation state machine is in the SYNC state (see Figure 15).

Figure 16 - HCS Verification State Diagram



The RXCP accumulates the number of received assigned cells, received unassigned/idle cells, cells containing a correctable HCS error and cells containing an uncorrectable HCS error, in saturating counters.

9.17 Receive ATM 4 Cell FIFO (RXFF)

The Receive FIFO (RXFF) provides FIFO management and the S/UNI-MPH receive cell interface. The receive FIFO can hold four cells (note that the effective working FIFO depth is actually three cells because if four complete cells are being held in the FIFO, the next information bit transmitted to the RXCP, even if it is part of a null cell, will cause a FIFO overflow). The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include filling the receive FIFO, indicating when the receive FIFO contains cells, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions.

A Saturn Compatible Interface (SCI-PHY™) FIFO is provided. This synchronous FIFO accepts a read clock (RFCLK) and read enable signal from the MPHY block. The receive FIFO output bus is tristated when the read enable is inactive. The interface indicates the start of a cell (RSOC) and the receive cell available status (RCA) when data is read from the receive FIFO (using the rising edges of RFCLK while read enable is active). The RCA status changes from available to unavailable when the FIFO is 4 byte read accesses away from being empty (or when the FIFO is empty, when REMPTY4 is logic 0).

This RXFF indicates FIFO overruns using a maskable interrupt and register bits. The FIFO is reset on FIFO overrun, causing up to 4 cells to be lost.

9.18 Transmit ATM Cell Processor (TXCP)

The Transmit Cell Processor (TXCP) Block integrates circuitry to support ATM cell payload scrambling, header check sequence (HCS) generation, and idle/unassigned cell generation.

The TXCP scrambles the cell payload field using the self synchronizing scrambler with polynomial $x^{43} + 1$. The header portion of the cells is not scrambled. Note that cell payload scrambling is optional in the S/UNI-MPH.

The HCS is generated using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the calculated HCS octet as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432. The resultant octet optionally overwrites the HCS octet in the transmit cell. When the transmit FIFO is empty, the TXCP inserts idle/unassigned cells. The idle/unassigned cell header is fully programmable using five internal registers. Similarly, the 48 octet information field is programmed with an 8 bit repeating pattern using an internal register. The TXCP accumulates the number of transmitted assigned cells in a saturating counter.

For T1/E1 formats, the cell octets are byte aligned with the transmission overhead (the framing bit for the T1 format, and timeslots 0/16 for the E1 format). For arbitrary bit rate interfaces, the cell octets are optionally aligned to the overhead indication signal (TOHI).

9.19 Transmit ATM 4 Cell FIFO (TXFF)

The Transmit FIFO (TXFF) provides FIFO management and the S/UNI-MPH transmit cell interface. The transmit FIFO can hold up to four cells. The FIFO depth may be programmed to one, two, three, or four cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include emptying cells from the transmit FIFO, indicating when the transmit FIFO is full, maintaining the transmit FIFO read and write pointers and detecting a FIFO overrun condition.

A Saturn Compatible Interface (SCI-PHY™) FIFO is provided. This synchronous FIFO accepts a write clock (TFCLK), a start of cell indication (TSOC), and a write enable signal from the MPHY block. The interface provides a transmit cell available status (TCA) which can transition from available to unavailable when the transmit FIFO is near full and can accept no more than 4 writes (when TFULL4 is logic 1) or when the FIFO is full and can accept no more writes (default).

The TXFF indicates FIFO overruns using a maskable interrupt and register bits. Writes to the TXFF while the FIFO is full (i.e. overruns) are ignored.

9.20 Saturn Compatible Multi-PHY Interface (MPHY)

The Saturn Compatible Multi-PHY Interface block (MPHY) permits the four receive cell FIFOs (RXFF) and the four transmit cell FIFOs (TXFF) to share a single cell interface on the S/UNI-MPH.

Two interface modes are supported: 1) multi-phy addressing (when the MPHEN input is high) and 2) direct phy selection (when the MPHEN input is low).

When multi-phy addressing is enabled, one of four possible transmit/receive FIFOs is selected by the TWA[1:0]/RRA[1:0] address signals respectively. The cell available signal for each of the four transmit/receive FIFOs is also selected by TWA[1:0]/RRA[1:0]. While a cell transfer is in progress to/from a particular FIFO, the cell available indications from the remaining three FIFOs may be polled using TWA[1:0] or RRA[1:0]. These indications are available on RCAMPH (for the three remaining RXFFs) and on TCAMPH (for the three remaining TXFFs). The cell available indication from the active FIFO is only valid at the end of the cell transfer (or four reads/writes before the end of the cell transfer depending on the configuration of the FIFO). The cell available indications are also directly available on TCA[4:1] and RCA[4:1] when the multi-phy addressing mode is enabled.

When direct phy selection is enabled, one of four possible transmit/receive FIFOs is selected by the corresponding TWRENB[4:1]/RRDENB[4:1] signal respectively. The cell available status for each of the transmit and receive FIFOs is directly available on RCA[4:1] and TCA[4:1].

9.21 Microprocessor Interface (MPIF)

The Microprocessor Interface allows the S/UNI-MPH to be configured, controlled and monitored using internal registers.

10 REGISTER DESCRIPTION

Table 1 - Normal Mode Register Memory Map

Address				Register
#1	# 2	# 3	# 4	
000H	100H	200H	300H	Receive Configuration
001H	101H	201H	301H	Transmit Configuration
002H	102H	202H	302H	Datalink Options
003H	103H	203H	303H	Receive Interface Configuration
004H	104H	204H	304H	Transmit Interface Configuration
005H	105H	205H	305H	Receive TS0 Datalink
006H	106H	206H	306H	Transmit TS0 Datalink
007H	107H	207H	307H	Transmit Timing Options
008H	108H	208H	308H	Interrupt Source #1
009H	109H	209H	309H	Interrupt Source #2
00AH	10AH	20AH	30AH	Diagnostics
00BH				Master Test
00CH				Revision/Chip ID/Global Monitoring Update
00DH				Source Selection/Interrupt ID
00EH				Clock Activity Monitor
	10BH	20BH	30BH	Reserved
	10CH	20CH	30CH	Reserved
	10DH	20DH	30DH	Reserved
	10EH	20EH	30EH	Reserved
00FH	10FH	20FH	30FH	Reserved
010H	110H	210H	310H	CDRC Configuration
011H	111H	211H	311H	CDRC Interrupt Enable
012H	112H	212H	312H	CDRC Interrupt Status

Address				Register
#1	# 2	# 3	# 4	
013H	113H	213H	313H	Alternate Loss of Signal
014H	114H	214H	314H	ALMI Configuration
015H	115H	215H	315H	ALMI Interrupt Enable
016H	116H	216H	316H	ALMI Interrupt Status
017H	117H	217H	317H	ALMI Alarm Detection Status
018H	118H	218H	318H	DJAT Interrupt Status
019H	119H	219H	319H	DJAT Reference Clock Divisor (N1) Control
01AH	11AH	21AH	31AH	DJAT Output Clock Divisor (N2) Control
01BH	11BH	21BH	31BH	DJAT Configuration
01CH	11CH	21CH	31CH	T1-FRMR Configuration
01DH	11DH	21DH	31DH	T1-FRMR Interrupt Enable
01EH	11EH	21EH	31EH	T1-FRMR Interrupt Status
01FH	11FH	21FH	31FH	Reserved
020H	120H	220H	320H	E1-FRMR block Framing Alignment Options
021H	121H	221H	321H	E1-FRMR Maintenance Mode Options
022H	122H	222H	322H	E1-FRMR Framing Status Interrupt Enable
023H	123H	223H	323H	E1-FRMR Maintenance/Alarm Status Interrupt Enable
024H	124H	224H	324H	E1-FRMR Framing Status Interrupt Indication
025H	125H	225H	325H	E1-FRMR Maintenance/Alarm Status Interrupt Indication
026H	126H	226H	326H	E1-FRMR Framing Status
027H	127H	227H	327H	E1-FRMR Maintenance/Alarm Status
028H	128H	228H	328H	E1-FRMR International/National Bits
029H	129H	229H	329H	

Address				Register
#1	# 2	# 3	# 4	
02AH	12AH	22AH	32AH	E1-FRMR block CRC Error Count - LSB
02BH	12BH	22BH	32BH	E1-FRMR block CRC Error Count - MSB
02CH - 02FH	12CH - 12FH	22CH - 22FH	32CH - 32FH	Reserved
030H	130H	230H	330H	RBOC Enable
031H	131H	231H	331H	RBOC Code Status
032H - 033H	132H - 133H	232H - 233H	332H - 333H	Reserved
034H	134H	234H	334H	XFDL Configuration
035H	135H	235H	335H	XFDL Interrupt Status
036H	136H	236H	336H	XFDL Transmit Data
037H	137H	237H	337H	Reserved
038H	138H	238H	338H	RFDL Configuration
039H	139H	239H	339H	RFDL Interrupt Control/Status
03AH	13AH	23AH	33AH	RFDL Status
03BH	13BH	23BH	33BH	RFDL Receive Data
03CH	13CH	23CH	33CH	IBCD Configuration
03DH	13DH	23DH	33DH	IBCD Interrupt Enable/Status
03EH	13EH	23EH	33EH	IBCD Activate Code
03FH	13FH	23FH	33FH	IBCD Deactivate Code
040H	140H	240H	340H	T1-TRAN Configuration
041H	141H	241H	341FH	T1-TRAN Alarm Transmit
042H	142H	242H	342H	XIBC Control
043H	143H	243H	343H	XIBC Loopback Code
044H	144H	244H	344H	E1-TRAN Configuration
045H	145H	245H	345H	E1-TRAN Transmit Alarm/Diagnostic Control

Address				Register
#1	# 2	# 3	# 4	
046H	146H	246H	346H	E1-TRAN International/National Control
047H	147H	247H	347H	Reserved
048H	148H	248H	348H	PMON Control/Status
049H	149H	249H	349H	PMON FER Count
04AH	14AH	24AH	34AH	PMON FEBE Count (LSB)
04BH	14BH	24BH	34BH	PMON FEBE Count (MSB)
04CH	14CH	24CH	34CH	PMON CRC Count (LSB)
04DH	14DH	24DH	34DH	PMON CRC Count (MSB)
04EH	14EH	24EH	34EH	PMON LCV Count (LSB)
04FH	14FH	24FH	34FH	PMON LCV Count (MSB)
050H - 054H	150H - 154H	250H - 254H	350H - 354H	Reserved
055H	155H	255H	355H	PDVD Interrupt Enable/Status
056H	156H	256H	356H	Reserved
057H	157H	257H	357H	XBOC Code
058H	158H	258H	358H	Reserved
059H	159H	259H	359H	XPDE Interrupt Enable/Status
05AH - 063H	15AH - 163H	25AH - 263H	35AH - 363H	Reserved
064H	164H	264H	364H	RXCP Uncorrectable HCS Error Count LSB
065H	165H	265H	365H	RXCP Uncorrectable HCS Error Count MSB
066H	166H	266H	366H	Reserved
067H	167H	267H	367H	Reserved
068H	168H	268H	368H	RXCP Correctable HCS Error Count LSB
069H	169H	269H	369H	RXCP Correctable HCS Error Count MSB

Address				Register
#1	# 2	# 3	# 4	
06AH	16AH	26AH	36AH	RXCP Idle/Unassigned Cell Count LSB
06BH	16BH	26BH	36BH	RXCP Idle/Unassigned Cell Count MSB
06CH	16CH	26CH	36CH	RXCP Receive Cell Count LSB
06DH	16DH	26DH	36DH	RXCP Receive Cell Count MSB
06EH	16EH	26EH	36EH	TXCP Transmit Cell Count LSB
06FH	16FH	26FH	36FH	TXCP Transmit Cell Count MSB
070H	170H	270H	370H	RXCP Control
071H	171H	271H	371H	RXCP Framing Control
072H	172H	272H	372H	RXCP Interrupt Enable/Status
073H	173H	273H	373H	RXCP Idle/Unassigned Cell Pattern: H1 octet
074H	174H	274H	374H	RXCP Idle/Unassigned Cell Pattern: H2 octet
075H	175H	275H	375H	RXCP Idle/Unassigned Cell Pattern: H3 octet
076H	176H	276H	376H	RXCP Idle/Unassigned Cell Pattern: H4 octet
077H	177H	277H	377H	RXCP Idle/Unassigned Cell Mask: H1 octet
078H	178H	278H	378H	RXCP Idle/Unassigned Cell Mask: H2 octet
079H	179H	279H	379H	RXCP Idle/Unassigned Cell Mask: H3 octet
07AH	17AH	27AH	37AH	RXCP Idle/Unassigned Cell Mask: H4 octet
07BH	17BH	27BH	37BH	RXCP User-Programmable Cell Pattern: H1 octet
07CH	17CH	27CH	37CH	RXCP User-Programmable Cell Pattern: H2 octet
07DH	17DH	27DH	37DH	RXCP User-Programmable Cell Pattern: H3 octet

Address				Register
#1	# 2	# 3	# 4	
07EH	17EH	27EH	37EH	RXCP User-Programmable Cell Pattern: H4 octet
07FH	17FH	27FH	37FH	RXCP User-Programmable Cell Mask: H1 octet
080H	180H	280H	380H	RXCP User-Programmable Cell Mask: H2 octet
081H	181H	281H	381H	RXCP User-Programmable Cell Mask: H3 octet
082H	182H	282H	382H	RXCP User-Programmable Cell Mask: H4 octet
083H	183H	283H	383H	RXCP HCS Control/Status
084H	184H	284H	384H	RXCP LCD Count Threshold
085H - 087H	185H - 187H	285H - 287H	385H - 387H	Reserved
088H	188H	288H	388H	TXCP Control
089H	189H	289H	389H	TXCP Interrupt Enable/Status
08AH	18AH	28AH	38AH	TXCP Idle/Unassigned Cell Pattern: H1 octet
08BH	18BH	28BH	38BH	TXCP Idle/Unassigned Cell Pattern: H2 octet
08CH	18CH	28CH	38CH	TXCP Idle/Unassigned Cell Pattern: H3 octet
08DH	18DH	28DH	38DH	TXCP Idle/Unassigned Cell Pattern: H4 octet
08EH	18EH	28EH	38EH	TXCP Idle/Unassigned Cell Pattern: H5 octet
08FH	18FH	28FH	38FH	TXCP Idle/Unassigned Cell Payload
090H - 0FFH	190H - 1FFH	290H - 2FFH	390H - 3FFH	Reserved
400H-7FFH				Reserved for Test

11 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-MPH. Normal mode registers (as opposed to test mode registers) are selected when A[10] is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-MPH to determine the programming state of the chip.

3. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.

   Writing into read-only normal mode register bit locations does not affect S/UNI-MPH operation unless otherwise noted.

Registers 000H, 100H, 200H and 300H: Receive Configuration

Bit	Type	Function	Default
Bit 7	R/W	WORDERR	0
Bit 6	R/W	CNTNFAS	0
Bit 5	R/W	RXDMAGAT	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	MODE[1]	0
Bit 0	R/W	MODE[0]	0

These registers are used to configure the receive interfaces of the S/UNI-MPH.

WORDERR:

When the E1 format is enabled, the WORDERR bit determines how frame alignment signal (FAS) errors are reported. When WORDERR is logic 1, one or more errors in the seven bit FAS word results in a single framing error count. When WORDERR is logic 0, each error in a FAS word results in a single framing error count.

CNTNFAS:

When the E1 format is enabled, the CNTNFAS bit determines whether non-frame alignment signal (NFAS) errors are reported. When the CNTNFAS bit is a logic 1, a zero in bit 2 of time slot 0 of NFAS frames results in an increment of the framing error count. If WORDERR is also a logic 1, the word is defined as the eight bits comprising the FAS pattern and bit 2 of time slot 0 of the next NFAS frame. When the CNTNFAS bit is a logic 0, only errors in the FAS affect the framing error count.

RXDMAGAT:

The RXDMAGAT bit selects the gating of the RDLINT[x] output with the RDLEOM[x] output when the internal HDLC receiver is used with DMA. When RXDMAGAT is set to logic 1, the RDLINT[x] DMA output is gated with the RDLEOM output so that RDLINT is forced to logic 0 when RDLEOM is logic 1. When RXDMAGAT is set to logic 0, the RDLINT[x] and RDLEOM[x] outputs operate independently.

MODE [1:0]:

The MODE[1:0] bits determine the configuration of each physical interface receiver in the S/UNI-MPH. *The four interfaces must be configured identically* by writing these bits in each of the four Receive Configuration registers.

MODE[1]	MODE[0]	Configuration
0	0	1.544 Mbit/s T1 ATM UNI
0	1	2.048 Mbit/s E1 ATM UNI
1	0	6.312 Mbit/s J2 ATM UNI This configuration requires an external J2 framer.
1	1	Arbitrary Format UNI (≤ 25 Mbit/s) This configuration relies on an external device to identify the overhead bits in the arbitrary transmission format.

Registers 001H, 101H, 201H and 301H: Transmit Configuration

Bit	Type	Function	Default
Bit 7	R/W	LCDEN	1
Bit 6	R/W	AISEN	1
Bit 5	R/W	REDEN	1
Bit 4	R/W	OOFEN	1
Bit 3	R/W	LOSEN	1
Bit 2	R/W	TAISEN	0
Bit 1	R/W	MODE[1]	0
Bit 0	R/W	MODE[0]	0

These registers are used to configure the transmit interfaces of the S/UNI-MPH.

LCDEN:

The LCDEN bit enables the receive loss of cell delineation indication to automatically generate a receive failure indication in the transmit stream. This bit operates regardless of framer selected (T1 or E1). When LCDEN is logic 1, declaration of the LCD alarm causes a yellow alarm (T1) or remote alarm indication (E1) to be transmitted for the duration of the LCD alarm. When LCDEN is logic 0, assertion of the LCD alarm does not cause transmission of a receive failure indication.

AISEN:

The AISEN bit enables the alarm indication signal carrier failure alarm to automatically generate a receive failure indication in the transmit stream. This bit operates regardless of framer selected (T1 or E1). When AISEN is logic 1, declaration of the AIS CFA causes a yellow alarm (T1) or remote alarm indication (E1) to be transmitted for the duration of the CFA. When AISEN is logic 0, assertion of AIS CFA does not cause transmission of a receive failure indication.

REDEN:

The REDEN bit enables the red carrier failure alarm (persistent out of frame) indication to automatically generate a receive failure indication in the transmit stream. This bit operates regardless of the format selected (T1 or E1) When REDEN is logic 1, declaration of the red CFA causes a yellow alarm (T1) or remote alarm indication (E1) to be transmitted for the duration of the

CFA. When REDEN is logic 0, assertion of red CFA does not cause transmission of a receive failure indication.

OOFEN:

The OOFEN bit enables the receive out of frame indication to automatically generate a receive failure indication in the transmit stream. This bit operates regardless of the format selected (T1 or E1). When OOFEN is logic 1, declaration of the OOF alarm causes a yellow alarm (T1) or remote alarm indication (E1) to be transmitted for the duration of the OOF alarm. When OOFEN is logic 0, assertion of the OOF alarm does not cause transmission of a receive failure indication.

LOSEN:

The LOSEN bit enables the receive loss of signal indication to automatically generate a receive failure indication in the transmit stream. This bit operates regardless of the format selected (T1 or E1). When LOSEN is logic 1, declaration of the LOS alarm causes a yellow alarm (T1) or remote alarm indication (E1) to be transmitted for the duration of the LOS alarm. The LOS alarm is removed when the pulse density requirements for the T1 or E1 format are satisfied. When LOSEN is logic 0, assertion of the LOS alarm does not cause transmission of a receive failure indication.

TAISEN:

When the T1 or E1 format is selected, the TAISEN bit enables the generation of an unframed all-ones AIS alarm on the TDP/TDD[x] and TDN/TOHO[x] multifunction pins. When TAISEN is set to logic 1 and TUNI is set to logic 0, the bi-polar TDP[x] and TDN[x] outputs are forced to pulse alternately, creating an all-ones signal; when TAISEN and TUNI are both set to logic 1, the uni-polar TDD[x] output is forced to all-ones. When TAISEN is set to logic 0, the TDP/TDD[x] and TDN/TOHO[x] multifunction outputs operate normally. The transition to transmitting AIS on the TDP[x] and TDN[x] outputs is done in such a way as to not introduce any bipolar violations.

MODE [1:0]:

The MODE[1:0] bits determine the configuration of each physical interface transmitter in the S/UNI-MPH. *The four interfaces must be configured identically* by writing these bits in each of the four Transmit Configuration registers.

MODE[1]	MODE[0]	Configuration
0	0	1.544 Mbit/s T1 ATM UNI

MODE[1]	MODE[0]	Configuration
0	1	2.048 Mbit/s E1 ATM UNI
1	0	6.312 Mbit/s J2 ATM UNI This configuration requires an external J2 framer.
1	1	Arbitrary Format UNI (≤ 25 Mbit/s) This configuration relies on an external device to insert the overhead bits in the arbitrary transmission format.

Registers 002H, 102H, 202H and 302H: Datalink Options

Bit	Type	Function	Default
Bit 7	R/W	RXDMASIG	0
Bit 6		Unused	X
Bit 5	R/W	TXDMASIG	0
Bit 4		Unused	X
Bit 3	R/W	RDLINTE	0
Bit 2	R/W	RDLEOME	0
Bit 1	R/W	TDLINTE	0
Bit 0	R/W	TDLUDRE	0

These registers allow software to configure the datalink options of each T1 or E1 interface.

RXDMASIG:

The RXDMASIG bit selects the internal HDLC receiver (RFDL) data-received interrupt (INT) and end-of-message (EOM) signals to be output on the RDLINT[x] and RDLEOM[x] pins. When RXDMASIG is set to logic 1, the RDLINT[x] and RDLEOM[x] output pins can be used by a DMA controller to process the datalink. When RXDMASIG is set to logic 0, the RFDL INT and EOM signals are no longer available to a DMA controller; the signals on RDLINT[x] and RDLEOM[x] become the extracted datalink data and clock, RDLSIG[x] and RDLCLK[x]. In this mode, the data stream available on the RDLSIG[x] output corresponds to the extracted facility datalink for T1-ESF, or to the extracted timeslot 0 National bits or timeslot 16 for E1.

TXDMASIG:

The TXDMASIG bit selects the internal HDLC transmitter (XFDL) request for service interrupt (INT) and data underrun (UDR) signals to be output on the TDLINT[x] and TDLUDR[x] pins. When TXDMASIG is set to logic 1, the TDLINT[x] and TDLUDR[x] output pins can be used by a DMA controller to service the datalink. When TXDMASIG is set to logic 0, the XFDL INT and UDR signals are no longer available to a DMA controller; the signals on TDLINT[x] and TDLUDR[x] become the serial datalink data input and clock, TDLSIG[x] and TDLCLK[x]. In this mode an external controller is responsible for formatting the data stream presented on the TDLSIG[x] input to correspond to the facility datalink in T1-ESF, or to the extracted timeslot 0 National bits or timeslot 16 for E1.

RDLINTE:

The RDLINTE bit enables the RFDL received-data interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the RFDL without needing to interface to the DMA control signals. When RDLINTE is set to logic 1, an event causing an interrupt in the RFDL (which is visible on the RDLINT[x] output pin when RXDMASIG is logic 1) also causes an interrupt to be generated on the INTB output. When RDLINTE is set to logic 0, an interrupt event in the RFDL does not cause an interrupt on INTB.

RDLEOME:

The RDLEOME bit enables the RFDL end-of-message interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the RFDL without needing to interface to the DMA control signals. When RDLEOME is set to logic 1, an end-of-message event causing an EOM interrupt in the RFDL (which is visible on the RDLEOM[x] output pin when RXDMASIG is logic 1) also causes an interrupt to be generated on the INTB output. When RDLEOME is set to logic 0, an EOM interrupt event in the RFDL does not cause an interrupt on INTB. NOTE: within the RFDL, an end-of-message event causes an interrupt on both the EOM and INT RFDL interrupt outputs. See the Operation section for further details on using the RFDL.

TDLINTE:

The TDLINTE bit enables the XFDL request for service interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the XFDL without needing to interface to the DMA control signals. When TDLINTE is set to logic 1, an request for service interrupt event in the XFDL (which is visible on the TDLINT[x] output pin when TXDMASIG is logic 1) also causes an interrupt to be generated on the INTB output. When TDLINTE is set to logic 0, an interrupt event in the XFDL does not cause an interrupt on INTB.

TDLUDRE:

The TDLUDRE bit enables the XFDL transmit data underrun interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the XFDL without needing to interface to the DMA control signals. When TDLUDRE is set to logic 1, an underrun event causing an interrupt in the XFDL (which is visible on the TDLUDR[x] output pin when TXDMASIG is logic 1) also causes an interrupt to be generated on the INTB output. When TDLUDRE is set to logic 0, an underrun event in the XFDL does not cause an interrupt on INTB.

Registers 003H, 103H, 203H and 303H: Receive Interface Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BPV	0
Bit 4	R/W	RDNINV	0
Bit 3	R/W	RDPINV	0
Bit 2	R/W	RUNI	0
Bit 1	R/W	RFALL	0
Bit 0		Unused	X

These registers enable the Receive Interface to handle the various input waveform formats.

BPV:

When the T1 or E1 format is selected, the BPV bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPV is set to logic 1, only BPVs not part of a valid B8ZS or HDB3 signature generate an LCV indication and increment the PMON LCV counter. When BPV is set to logic 0, both BPVs not part of a valid B8ZS signature and excessive zeros (EXZ) generate an LCV indication and increment the PMON LCV counter. Excessive zeros is a sequence of zeros greater than 15 bits long for a T1 AMI-coded signal, greater than 7 bits long for a T1 B8ZS-coded signal, and greater than 3 bits long for an E1 AMI or HDB3-coded signal.

RDPINV,RDNINV:

The RDPINV and RDNINV bits enable the Receive Interface to logically invert the signals received onmultifunction pins RDP/RDD[x] and RDN/RLCV/ROH[x], respectively. When RDPINV is set to logic 1, the interface inverts the signal on the RDP/RDD[x] input. When RDPINV is set to logic 0, the interface passes the RDP/RDD[x] signal unaltered. When RDNINV is set to logic 1, the interface inverts the signal on the RDN/RLCV/ROH[x] input. When RDNINV is set to logic 0, the interface passes the RDN/RLCV/ROH[x] signal unaltered.

RUNI:

When the T1 or E1 format is selected, the RUNI bit enables the interface to receive uni-polar digital data and line code violation indications on the multifunction pins RDP/RDD[x] and RDN/RLCV/ROH[x]. When RUNI is set to logic 1, the RDP/RDD[x] and RDN/RLCV/ROH[x] multifunction pins become the data and line code violation inputs, RDD[x] and RLCV[x], sampled on the selected RCLKI[x] edge. When RUNI is set to logic 0, the RDP/RDD[x] and RDN/RLCV/ROH[x] multifunction pins become the positive and negative pulse inputs, RDP[x] and RDN[x]. If RUNI is set to logic 1, the DCR bit in the CDRC Configuration Register must also be set to logic 1. The RUNI bit is ignored if either the J2 or Arbitrary framing formats are selected.

RFALL:

The RFALL bit enables the Receive Interface to sample the multifunction pins on the falling RCLKI[x] edge when clock recovery is disabled. When RFALL is set to logic 1, the interface is enabled to sample the RDP/RDD[x] and RDN/RLCV/ROH[x] inputs on the falling RCLKI[x] edge. When RFALL is set to logic 0, the interface is enabled to sample the inputs on the rising RCLKI[x] edge.

Registers 004H, 104H, 204H and 304H: Transmit Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	TOCTA	0
Bit 6	R/W	TOHINV	0
Bit 5	R/W	TDNINV	0
Bit 4	R/W	TDPINV	0
Bit 3	R/W	TUNI	0
Bit 2	R/W	TFALL	0
Bit 1	R/W	TRISE	0
Bit 0	R/W	TRZ	0

These registers enable the Transmit Interface to generate the required digital output waveform format.

TOCTA:

The TOCTA bit configures the interface to octet-align the transmit cell stream to the transmission overhead. This bit has no effect when T1, E1 or J2 formats are selected, since octet alignment is specified for these formats. When the arbitrary format is selected and TOCTA is set to logic 1, the ATM cell octets are aligned to the arbitrary transmission format overhead boundaries (as delineated by the TOHI input). The number of TCLKI periods between transmission format overhead bit positions must be divisible by 8. When TOCTA is set to logic 0, no octet alignment is performed, and there is no restriction on the number of TCLKI periods between transmission format overhead bit positions.

TOHINV:

The TOHINV bit enables the Transmit Interface to internally invert the signal on the TFPI/TOHI multifunction pin, changing its active polarity. When TOHINV is set to logic 1, the TFPI/TOHI input is active low. When TOHINV is set to logic 0, the TFPI/TOHI input is active high.

TDPINV,TDNINV:

The TDPINV and TDNINV bits enable the Transmit Interface to logically invert the signals output on the TDP/TDD[x] and TDN/TOHO[x] multifunction pins, respectively. When TDPINV is set to logic 1, the TDP/TDD[x] output is inverted. When TDPINV is set to logic 0, the TDP/TDD[x] output is not

inverted. When TDNINV is set to logic 1, the TDN/TOHO[x] output is inverted. When TDNINV is set to logic 0, the TDN/TOHO[x] output is not inverted.

TUNI:

When the T1 or E1 format is selected, the TUNI bit enables the transmit interface to generate unipolar digital outputs on the TDP/TDD[x] pin. When TUNI is set to logic 1, the TDP/TDD[x] multifunction pin becomes the unipolar output TDD[x], updated on the selected TCLKO edge. When TUNI is set to logic 0, the TDP/TDD[x] and TDN/TOHO[x] multifunction pins become the bipolar outputs TDP[x] and TDN[x], also updated on the selected TCLKO[x] edge. The TUNI bit is ignored if either the J2 or Arbitrary framing formats are selected.

TFALL:

The TFALL bit enables the Transmit Interface to sample the multifunction pin TFPI/TOHI on the falling TCLKI edge. When TFALL is set to logic 1, the interface is enabled to sample the TFPI/TOHI input on the falling TCLKI edge. When TFALL is set to logic 0, the interface is enabled to sample the inputs on the rising TCLKI edge.

TRISE:

The TRISE bit configures the interface to update the multifunction outputs on the rising edge of TCLKO[x]. When TRISE is set to logic 1, the interface is enabled to update the TDP/TDD[x] and TDN/TOHO[x] output pins on the rising TCLKO[x] edge. When TRISE is set to logic 0, the interface is enabled to update the outputs on the falling TCLKO[x] edge.

TRZ:

The TRZ bit configures the interface to transmit bipolar return-to-zero formatted waveforms. When TRZ is set to logic 1, the interface is enabled to generate the TDP[x] and TDN[x] output signals as RZ waveforms with duration equal to half the TCLKO[x] period. When TRZ is set to logic 0, the interface is enabled to generate the TDP[x] and TDN[x] output signals as NRZ waveforms with duration equal to the TCLKO[x] period, updated on the selected edge of TCLKO[x]. The TRZ bit can only be used when TUNI is set to logic 0.

Registers 005H, 105H, 205H and 305H: Receive TS0 Data Link

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SACE	0
Bit 5	R	SACI	0
Bit 4	R/W	RXSA4EN	1
Bit 3	R/W	RXSA5EN	0
Bit 2	R/W	RXSA6EN	0
Bit 1	R/W	RXSA7EN	0
Bit 0	R/W	RXSA8EN	0

These registers are used when the E1 format is selected to choose timeslot 16 or the required subset of timeslot 0 National bits that constitute the receive data link.

SACE:

The SACE bit enables the generation of an interrupt whenever there is a change in the National bits that are not extracted to form a data link. Changes in the National bits are not debounced, i.e. the interrupt is generated immediately when the current value of the National bits differs from the previous value. The value of the National bits can be read in the FRMR International/National Bits Register.

SACI:

The SACI bit is set to logic one whenever there is a change in the National bits that are not extracted to form a data link. The SACI bit is cleared following a read of this register.

RXSA4EN, RXSA5EN, RXSA6EN, RXSA7EN and RXSA8EN:

The RXSAxEN bits control the extraction of a data link from the received Time Slot 0 National Use bits (Sa4 through Sa8).

If the RXDMASIG bit from the Datalink Options Register is a logic 1, the data link bits are terminated by the internal HDLC receiver; otherwise, the data link is presented on RDLSIG. If the RXSA4EN is logic 1, the RDLSIG value is extracted from bit 4 of Time Slot 0 of non-frame alignment signal frames. If the RXSA8EN is logic 1, the RDLSIG value is extracted from bit 8 of Time Slot 0 of non-frame alignment signal frames. The other enable bits operate in

an analogous fashion. A clock pulse is generated on RDLCLK for each enable that is logic 1. Any combination enable bits is allowed resulting in a data rate between 4 kbit/s and 20 kbit/s.

If all RXSAEN[4:0] bits are set to logic 0, Timeslot 16 is extracted and treated as a data link. If RXDMASIG is logic 0, Timeslot16 is made available on the RDLSIG output and RDLCLK is an associated 64 kHz clock. If RXDMASIG is logic 1, the data link is terminated by the HDLC receiver and the RDLINT/RDLSIG and RDLEOM/RDLCLK pins operate as a data link interrupt (RDLINT) and a end-of-message (RDLEOM) indication.

Registers 006H, 106H, 206H and 306H: Transmit TS0 Data Link

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TXSA4EN	1
Bit 3	R/W	TXSA5EN	0
Bit 2	R/W	TXSA6EN	0
Bit 1	R/W	TXSA7EN	0
Bit 0	R/W	TXSA8EN	0

These registers are used when the E1 format is selected to choose timeslot 16 or the required subset of timeslot 0 National bits that constitute the transmit data link.

TXSA4EN, TXSA5EN, TXSA6EN, TXSA7EN and TXSA8EN:

The TXSAxEN bits control the insertion of a data link into the Time Slot 0 National Use bits (Sa4 through Sa8).

These bits only have effect if the TRAN block Configuration DLEN bit is logic 0 or if the TRAN block Configuration SIGEN bit is logic 1. The TXSAxEN bits take priority over the FDIS bit of the E1-TRAN block Configuration register. The data link bits are still inserted if FDIS is logic 1.

If the TXDMASIG bit is a logic 1, the data link bits are sourced by the internal HDLC transmitter; otherwise, the bits are sourced from the TDLSIG pin. If the TXSA4EN bit is logic 1, the TDLSIG value is written into bit 4 of Time Slot 0 of non-frame alignment signal frames. If the TXSA8EN bit is logic 1, the TDLSIG value is written into bit 8 of Time Slot 0 of non-frame alignment signal frames. The other enable bits operate in an analogous fashion. A clock pulse is generated on TDLCLK for each enable that is logic 1. Any combination of enable bits is allowed, resulting in a data rate between 4 kbit/s and 20 kbit/s. Clearing all disables insertion. Any National Use bits which are not included in the data link are sourced from E1 TRAN block International/National Control register.

Registers 007H, 107H, 207H and 307H: Transmit Timing Options

Bit	Type	Function	Default
Bit 7	R/W	FIFOBYP	0
Bit 6	R/W	XCLKSEL	0
Bit 5		Unused	0
Bit 4	R/W	OCLKSEL	0
Bit 3	R/W	TREF[1]	0
Bit 2	R/W	TREF[0]	0
Bit 1		Unused	X
Bit 0		Unused	X

When the T1 or E1 format is selected, these registers allow software to configure the options of the transmit timing section.

FIFOBYP:

The FIFOBYP bit enables the transmit input signals to DJAT to be bypassed around the FIFO to the outputs. When jitter attenuation is not being used, the DJAT FIFO can be bypassed to reduce the delay through the transmitter section by typically 24 bits. When FIFOBYP is set to logic 1, the inputs to DJAT are routed around the FIFO to the outputs. When FIFOBYP is set to logic 0, the transmit data passes through the DJAT FIFO. When the T1 or E1 format is not enabled, the FIFO is automatically bypassed.

XCLKSEL:

The XCLKSEL bit selects the source of the high-speed clock used in the CDRC and FRMR blocks. When XCLKSEL is set to logic 1, the XCLK input signal is used as the high-speed clock to these blocks. XCLK must be driven with clock that is 8 times the nominal bit rate (12.352 MHz for T1 or 16.384 MHz for E1). When XCLKSEL is set to logic 0, the high-speed clock is driven by XCLK divided by 3. XCLK must be driven with a clock that is 24 times the nominal bit rate (37.056MHz for T1 or 49.152 MHz for E1). XCLK must be set to logic 0 when jitter attenuation is enabled.

OCLKSEL:

The OCLKSEL bit selects the source of the Digital Jitter Attenuator FIFO output clock signal. When OCLKSEL is set to logic 1, the DJAT FIFO output clock is driven with the transmit reference clock as selected by the TREF[1:0] inputs. In this mode the jitter attenuation is disabled and the input clock must

be jitter-free. When OCLKSEL is set to logic 0, the DJAT FIFO output clock is driven with an internal jitter attenuated bit rate clock (1.544 MHz for T1 or 2.048 MHz for E1). FIFOBYP must be set to logic 1 if OCLKSEL is set to logic 1.

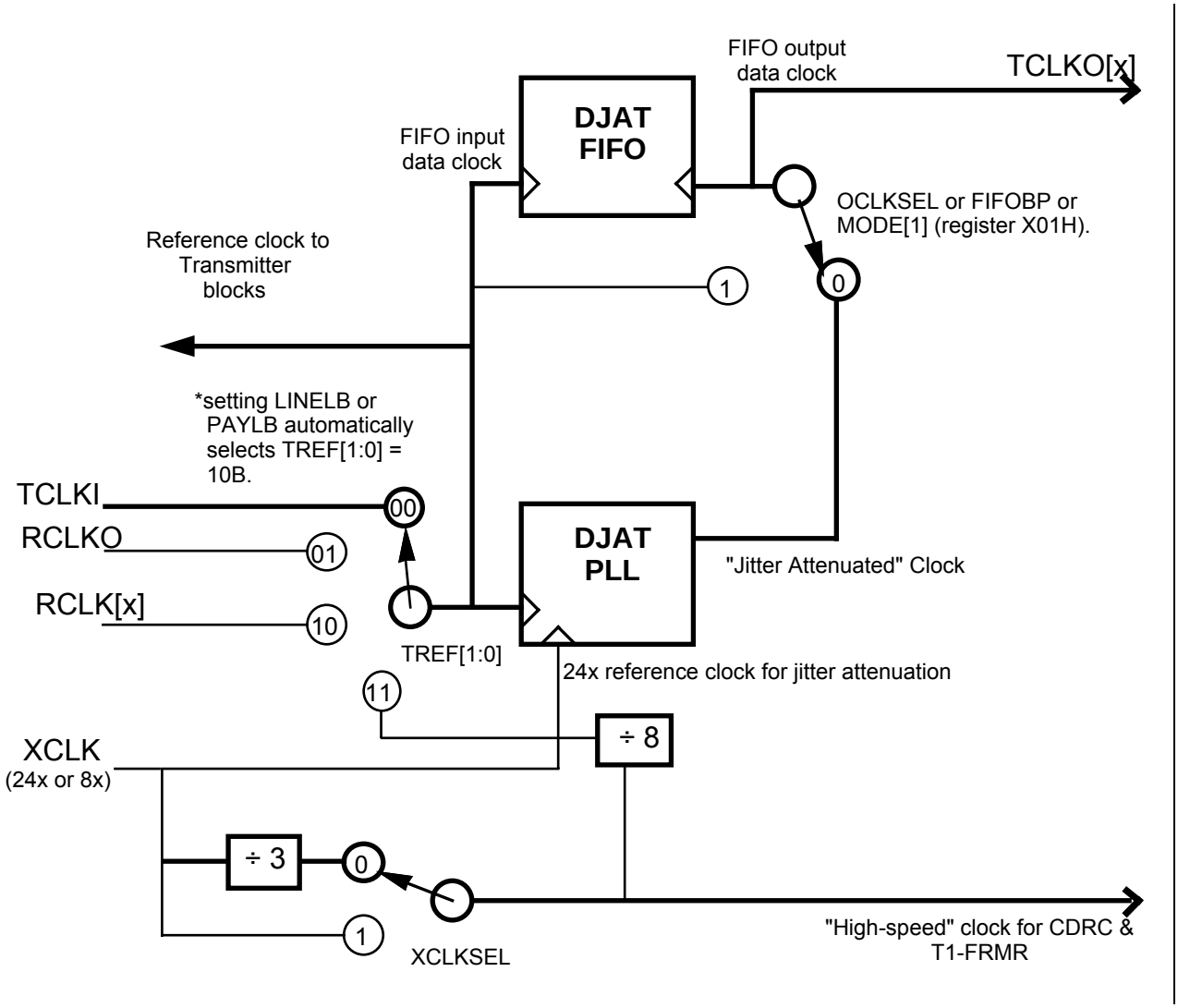
TREF[1:0]:

The TREF[1:0] bits select the transmit reference clock source as shown in the following table.:

TREF1	TREF0	Transmit Reference Source
0	0	TCLKI input.
0	1	Receive clock output (RCLKO) as selected by the RCLK[1:0] bits in the Source Selection/Interrupt ID register.
1	0	Receive clock from the RCLKI[x] input or recovered from the RDP[x]/RDN[x] inputs.
1	1	XCLK input divided by 8 or by 24 depending on the setting of the XCLKSEL bit.

Upon reset of the S/UNI-MPH, these bits are set to zero, selecting digital jitter attenuation with TCLKO[x] referenced to TCLK. Figure 17 illustrates the various bit setting options, with the reset condition highlighted.

Figure 17 - Transmit Timing Options



Registers 008H, 108H, 208H and 308H: Interrupt Source #1

Bit	Type	Function	Default
Bit 7	R	DJAT	0
Bit 6	R	IBCD	0
Bit 5	R	FRMR	0
Bit 4	R	PDVD	0
Bit 3	R	SAC	0
Bit 2	R	RFDL	0
Bit 1	R	RBOC	0
Bit 0	R	ALMI	0

These registers allow software to determine the block which produced the interrupt on the INTB output pin. The SAC bit is set if the SACI bit in the Receive TS0 Data Link register is set and is enabled to generate an interrupt

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Registers 009H, 109H, 209H and 309H: Interrupt Source #2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PMON	0
Bit 5	R	TXPRTY	0
Bit 4	R	XPDE	0
Bit 3	R	RXCP	0
Bit 2	R	TXCP	0
Bit 1	R	XFDL	0
Bit 0	R	CDRC/ALTLOS	0

These registers allow software to determine the block which produced the interrupt on the INTB output pin.

Reading these registers does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Registers 00AH, 10AH, 20AH and 30AH: Diagnostics and FIFO Parity Control

Bit	Type	Function	Default
Bit 7	R/W	TEVEN	0
Bit 6	R/W	REVEN	0
Bit 5	R/W	PAYLB	0
Bit 4	R/W	LINELB	0
Bit 3		Unused	X
Bit 2	R/W	DIALB	0
Bit 1	R/W	TPERRE	0
Bit 0	R	TPERRI	0

These registers allow software to enable the diagnostic mode of each interface and the control the fifo parity functions.

TEVEN:

The TEVEN bit selects the type of parity calculated and compared on the transmit synchronous FIFO interface. When TEVEN is logic 1, even parity is calculated across the TDAT[7:0] bus and compared to the incoming parity bit on TXPRTY. If there is a mismatch, the parity error indication, TPERRI, is forced to logic 1, and an interrupt is generated, if enabled. When TEVEN is logic 0, odd parity is calculated across TDAT[7:0] and compared to TXPRTY. Again, a parity error is indicated if there is a mismatch.

REVEN:

The REVEN bit selects the type of parity calculated and output on the receive synchronous FIFO interface. When REVEN is logic 1, even parity is calculated across the RDAT[7:0] bus and indicated on the outgoing parity bit, RXPRTY. When REVEN is logic 0, odd parity is calculated across RDAT[7:0] and indicated on RXPRTY.

PAYLB:

When the T1 or E1 format is selected, the PAYLB bit selects payload loopback. When PAYLB is set to logic 1, the received data output from the FRMR is internally connected to the transmit data input of the TRAN. The framing bit (T1 format) or timeslots 0 and 16 (E1 format) are reinserted by the TRAN prior to transmission. When PAYLB is set to logic 0, the payload loopback mode is disabled.

LINELB:

The LINELB bit selects the line loopback mode, where the data input on RDP/RDD[x] and RDN/RLCV/ROH[x] is connected to TDP/TDD[x] and TDN/TOHO[x] respectively. When LINELB is set to logic 1, the line loopback mode is enabled. When LINELB is set to logic 0, the line loopback mode is disabled. When either the J2 or arbitrary framing modes are selected, DJAT is disabled, and LINELB will reroute the RDD[x], ROH[x], and RCLKI[x] directly to TDD[x], TOHO[x], and TCLKO[x] respectively. For the J2 framing format, if the TOHO[x] output is desired to be the multi-frame pulse, PAYLB should be used instead of LINELB.

DIALB:

The DIALB bit selects the diagnostic loopback mode, where the transmit data stream is connected to the receive datastream. When DIALB is set to logic 1, the diagnostic digital loopback mode is enabled. When DIALB is set to logic 0, the diagnostic loopback mode is disabled.

TPERRE:

The TPERRE bit is an interrupt enable. When TPERRE is logic 1, a parity error detected on the transmit FIFO interface causes a microprocessor interrupt to be generated. When TPERRE is logic 0, a parity error does not cause an interrupt.

TPERRI:

When the TPERRI bit is logic 1, it indicates that a parity error was detected on the incoming transmit FIFO interface. When TPERRI is logic 0, no parity error was detected. Reading this register clears this bit to logic 0.

Register 00BH: Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	A_TM[9]	X
Bit 5	R/W	A_TM[8]	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select S/UNI-MPH test features. All bits, except for PMCTST and A_TM[9:8], are reset to zero by a hardware reset of the S/UNI-MPH. A software reset of the S/UNI-MPH does not affect the state of the bits in this register. Refer to the Test Features Description section for more information.

A_TM[9]:

The state of the A_TM[9] bit internally replaces the input address line A[9] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

A_TM[8]:

The state of the A_TM[8] bit internally replaces the input address line A[8] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

PMCTST:

The PMCTST bit is used to configure the S/UNI-MPH for PMC's manufacturing tests. When PMCTST is set to logic 1, the S/UNI-MPH microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin

high causes the S/UNI-MPH to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the S/UNI-MPH for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-MPH . While the HIZIO bit is a logic 1, all output pins of the S/UNI-MPH except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

Register 00CH: Revision/Chip ID/Global Monitoring Update

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[2]	1
Bit 5	R	TYPE[1]	0
Bit 4	R	TYPE[0]	1
Bit 3	R	TIP	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

RESET:

The RESET bit allows software to asynchronously reset the S/UNI-MPH. The software reset is equivalent to setting the RSTB input pin low. When a logic 1 is written to RESET, the S/UNI-MPH is reset. When a logic 0 is written to RESET, the reset is removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

TYPE[2:0]:

The TYPE[2:0] bits allow software to identify this device as the S/UNI-MPH member of the S/UNI family of products.

TIP:

The TIP bit is set to a logic one when any value with Bit 7 set to logic 0 is written to this register. Such a write initiates an accumulation interval transfer and loads all the performance meter registers in the PMON, RXCP, and TXCP blocks. TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete. Note that the transmit and receive line side clocks must be toggling for TIP to be cleared.

ID[2:0]:

The ID[2:0] bits allows software to identify the version level of the S/UNI-MPH.

Registers 00DH Source Selection/Interrupt ID

Bit	Type	Function	Default
Bit 7	R	INT4	0
Bit 6	R	INT3	0
Bit 5	R	INT2	0
Bit 4	R	INT1	0
Bit 3			X
Bit 2			X
Bit 1	R/W	RCLKO[1]	0
Bit 0	R/W	RCLKO[0]	0

This register provides interrupt identification and RCLKO source selection.

INT4, INT3, INT2, INT1:

The INTx bit will be high if the xth S/UNI-MPH interface causes the INTB pin to transition low.

RCLKO[1:0]:

The RCLKO[1:0] bits select the source for the receive clock output on the RCLKO pin.

RCLKO[1]	RCLKO[0]	RCLKO Source
0	0	The RCLKI[1] input or the clock recovered from RDP[1] and RDN[1].
0	1	The RCLKI[2] input or the clock recovered from RDP[2] and RDN[2].
1	0	The RCLKI[3] input or the clock recovered from RDP[3] and RDN[3].
1	1	The RCLKI[4] input or the clock recovered from RDP[4] and RDN[4].

Registers 00EH Clock Activity Monitor

Bit	Type	Function	Default
Bit 7	R	XCLKIA	0
Bit 6	R	RCLKI1A	0
Bit 5	R	RCLKI2A	0
Bit 4	R	RCLKI3A	0
Bit 3	R	RCLKI4A	0
Bit 2	R	TCLKIA	0
Bit 1	R	TFCLKA	0
Bit 0	R	RFCLKA	0

This register provides activity monitoring on S/UNI-MPH clock inputs.

XCLKA:

The XCLKA bit monitors for low to high transitions on the XCLK input. XCLKA is set high on a rising edge of XCLK, and is set low when this register is read.

RCLKI1A, RCLKI2A, RCLKI3A, RCLKI4A:

The RCLKIxA bits monitors for low to high transitions on the RCLKI[x] inputs. RCLKIxA is set high on a rising edge of RCLKI[x], and is set low when this register is read.

TCLKIA:

The TCLKIA bit monitors for low to high transitions on the TCLKI input. TCLKIA is set high on a rising edge of TCLKI, and is set low when this register is read.

TFCLKA:

The TFCLKA bit monitors for low to high transitions on the TFCLK input. TFCLKA is set high on a rising edge of TFCLK, and is set low when this register is read.

RFCLKA:

The RFCLKA bit monitors for low to high transitions on the RFCLK input. RFCLKA is set high on a rising edge of RFCLK, and is set low when this register is read.

Register 010H, 110H, 210H and 310H: CDRC Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6	R/W	LOS[1]	0
Bit 5	R/W	LOS[0]	0
Bit 4	R/W	DCR	0
Bit 3	R/W	SYNC	0
Bit 2	R/W	ALGSEL	0
Bit 1	R/W	O162	0
Bit 0	R/W	Reserved	0

Reserved:

The reserved bits must be programmed with a logic 0

AMI:

The alternate mark inversion (AMI) bit selects the line code of the incoming E1 or DS1 signal. A logic 1 selects AMI line code; a logic 0 selects HDB3 (E1 format) or B8ZS (T1 format).

LOS[1:0]:

The LOS[1:0] bits select the loss of signal declaration threshold. For example, if the threshold is set to 10, the 11th consecutive zero causes the declaration of LOS. LOS is removed when a single non-zero pulse is detected in the receive stream. The LOS declaration thresholds are shown in the table below:

LOS[1]	LOS[0]	Threshold (bit periods)
0	0	10 (E1 format selected) 15 (T1 format or AMI line code selected)
0	1	31
1	0	63
1	1	175

DCR:

The disable clock recovery (DCR) bit is used when RDP/RDD[x] and RDN/RLCV[x] contain NRZ formatted data. When DCR is a logic 1, the RCLKI[x] input contains the recovered clock. When DCR is a logic 0, the clock is recovered from the RDP[x] and RDN[x] inputs.

SYNC:

The SYNC bit enables synchronization of the recovered clock (RCLKI[x]) to the 8x clock when clock recovery is disabled. When SYNC is a logic 1, RCLKI[x] transitions are synchronized to the rising edges of the 8x clock. This bit must be set to logic 1 when clock recovery is disabled in T1 mode (DCR is a logic 1, MODE[1:0] in Receive Configuration register is 00B). This bit must be set to logic 0 if in E1 mode (MODE[1:0] in Receive Configuration register is 01B).

ALGSEL:

The Algorithm Select (ALGSEL) bit specifies the algorithm used by the DPLL for clock and data recovery. The choice of algorithm determines the high frequency input jitter tolerance of the CDRC. When ALGSEL is set to logic 1, the CDRC jitter tolerance is increased to approach 0.5UIpp for jitter frequencies above 20KHz. When ALGSEL is set to logic 0, the jitter tolerance is increased for frequencies below 20KHz (i.e. the tolerance is improved by 20% over that of ALGSEL=1 at these frequencies), but the tolerance approaches 0.4UIpp at the higher frequencies.

O162:

When the E1 format is selected and the AMI bit is logic 0, the Recommendation O.162 compatibility select bit (O162) allows selection between two line code definitions:

1.) If O162 is a logic 0, a line code violation is indicated if the serial stream does not match the verbatim HDB3 definition given in Recommendation G.703. A bipolar violation that is not part of an HDB3 signature or a bipolar violation in an HDB3 signature that is the same polarity as the last bipolar violation results in a line code violation indication.

2.) If O162 is a logic 1, a line code violation is indicated by a LCV output pulse if a bipolar violation is of the same polarity as the last bipolar violation, as per Recommendation O.162.

Registers 011H, 111H, 211H and 311H: CDRC Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LCVE	0
Bit 6	R/W	LOSE	0
Bit 5	R/W	LCSDE	0
Bit 4	R/W	EXZE	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The bit positions LCVE, LOSE, LCSDE and EXZE of this register are interrupt enables to select which of the status events (Line Code Violation , Loss Of Signal, B8ZS/HDB3 Signature Detection, or Excessive Zeros Detection), either singly or in combination, are enabled to generate an interrupt on the INTB pin when they are detected. A logic 1 bit in the corresponding bit position enables the detection of these signals to generate an interrupt; a logic 0 bit in the corresponding bit position disables that signal from generating an interrupt.

Registers 012H, 112H, 212H and 312H: CDRC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	LCVI	0
Bit 6	R	LOSI	0
Bit 5	R	LCSDI	0
Bit 4	R	EXZI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOS	0

The bit positions LCVI, LOSI, LCSDI and EXZI of this register indicate which of the status events generated an interrupt. A logic 1 in these bit positions indicate that the corresponding event was detected; a logic 0 in these bit positions indicate that no corresponding event has been detected. The bit positions LCVI, LCSDI and EXZI are set on the assertion of a line code violation, a line code signature detection, and excessive zeros detection, respectively. LOSI is set on a change of state of the LOS alarm. Bits LCVI, LOSI, LCSDI and EXZI are cleared by reading this register. The current state of the LOS alarm can be determined by reading bit 0 of this register.

Registers 013H, 113H, 213H and 313H: Alternate Loss of Signal Status

Bit	Type	Function	Default
Bit 7	R/W	ALTLOSE	0
Bit 6	R	ALTLOSI	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ALTLOS	X

The alternate loss of signal status provides a more stringent criteria for the deassertion of the alarm than the LOS indication in the CDRC Interrupt Status register.

ALTLOSE:

If the ALTLOSE bit is a logic 1, an interrupt is generated when the ALTLOS status bit changes state.

ALTLOSI:

The ALTLOSI bit is set high when the ALTLOS status bit changes state. It is cleared when this register is read.

ALTLOS:

The ALTLOS bit is asserted based on the LOS[1:0] threshold selected in the CDRC Configuration register. The ALTLOS bit is deasserted only after pulse density requirements have been met. The pulse density requirements for the T1 format specify that there must be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). The pulse density requirements for the E1 format specify that 255 bit periods are observed during which no sequence of four zeros is detected.

Registers 014H, 114H, 214H and 314H: ALMI Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ESF	0
Bit 3	R/W	FMS1	0
Bit 2	R/W	FMS0	0
Bit 1		Unused	X
Bit 0		Unused	X

These registers allow selection of the T1 framing format and the data rate of the Facility Data Link in ESF to allow operation of the CFA detection algorithms.

ESF, FMS[1], FMS[0]:

The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

ESF	FMS1	FMS0	Mode
0	0	0	Select SF format
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Select ESF framing format & 4 kbit FDL Data Rate
1	0	1	Select ESF framing format & 2 kbit FDL Data Rate
1	1	0	Select ESF framing format & 2 kbit FDL Data Rate
1	1	1	Reserved

Registers 015H, 115H, 215H and 315H: ALMI Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	FASTD	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	YELE	0
Bit 1	R/W	REDE	0
Bit 0	R/W	AISE	0

These registers select which of the three T1 Carrier Failure Alarms (CFA) can generate an interrupt when their logic state changes and enables the "fast" deassertion mode of operation.

FASTD:

The FASTD bit enables the "fast" deassertion of red and AIS alarms. When FASTD is set to a logic 1, deassertion of red alarm occurs within 120 ms of going in frame. Deassertion of AIS alarm occurs within 180 ms of either detecting a 60 ms interval containing 127 or more zeros, or going in frame. When FASTD is set to a logic 0, red and AIS alarm deassertion times remain as defined in the ALMI description.

Reserved:

The reserved bit must be programmed to logic 0 for correct operation.

YELE,REDE,AISE:

A logic 1 in the enable bit positions (YELE, REDE, AISE) enables a state change in the corresponding CFA to generate an interrupt; a logic 0 in the enable bit positions disables any state changes to generate an interrupt. The enable bits are independent; any combination of yellow, red, and AIS CFA's can be enabled to generate an interrupt.

Registers 016H, 116H, 216H and 316H: ALMI Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	YELI	0
Bit 4	R	REDI	0
Bit 3	R	AISI	0
Bit 2	R	YEL	0
Bit 1	R	RED	0
Bit 0	R	AIS	0

This registers indicates which of the three T1 CFAs have changed state in bit positions 5 through 3; and indicate the current state of each T1 CFA in bit positions 2 through 0. A logic 1 in the status positions (YELI, REDI, AISI) indicate that a state change in the corresponding CFA has occurred; a logic 0 in the status positions indicates that no state change has occurred. The status bit positions (bits 5 through 3) are cleared when this register is read.

Registers 017H, 117H, 217H and 317H: ALMI Alarm Detection Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	REDD	X
Bit 1	R	YELD	X
Bit 0	R	AISD	X

These registers indicate the presence or absence of one or more T1 OOF occurrences within the last 40ms; the presence or absence of T1 yellow alarm over the last 40ms; and indicate the presence or absence of the AIS signal over the last 60ms.

REDD:

When REDD is a logic 1, one or more T1 out of frame events have occurred during the last 40ms interval. When REDD is a logic 0, no out of frame events have occurred within the last 40ms interval.

YELD:

When YELD is logic 1, a valid yellow signal was present during the last 40ms interval. When YELD is logic 0, the yellow signal was absent during the last 40ms interval. For each T1 framing format, a valid YELLOW signal is deemed to be present if:

- bit 2 of each channel is not logic 0 for 16 or fewer times during the 40 ms interval for the SF framing format;
- the 16-bit yellow bit oriented code is received error-free 8 or more times during the interval for the ESF framing format with a 4 kHz data link;
- the 16-bit yellow bit oriented code is received error-free 4 or more times during the interval for the ESF framing format with a 2 kHz data link.

AISD:

When AISD is logic 1, a valid AIS signal was present during the last 60ms interval. When AISD is logic 0, the AIS signal was absent during the last 60ms interval. A valid AIS signal is deemed to be present during a 60 ms interval if the out of frame condition has persisted for the entire interval and the received stream is not zero for 126 or fewer periods.

Registers 018H, 118H, 218H and 318H: DJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	0
Bit 0	R	UNDI	0

These registers contain the indication of the DJAT FIFO status.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred.

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred.

Register 019H, 119H, 219H and 319H: DJAT Reference Clock Divisor (N1) Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

These registers define an 8-bit binary number, N1, which is one less than the magnitude of the divisor used to scale down the DJAT PLL reference clock input. The REF divisor magnitude, (N1+1), is the ratio between the frequency of REF input and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit in the DJAT Configuration register is high, will also reset the FIFO.

Registers 01AH, 11AH, 21AH and 31AH: DJAT Output Clock Divisor (N2) Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

These registers define an 8-bit binary number, N2, which is one less than the magnitude of the divisor used to scale down the DJAT smooth output clock signal. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit is high, will also reset the FIFO.

Registers 01BH, 11BH, 21BH and 31BH: DJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	1
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	SYNC	1
Bit 0	R/W	LIMIT	1

These registers control the operation of the DJAT FIFO read and write pointers and controls the generation of interrupt by the FIFO status.

Reserved:

This bit should be set to logic 1 for proper operation.

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, then the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions. The CENT bit can only be set to logic 1 if the SYNC bit in this register is set to logic 0.

OVRE,UNDE:

The OVRE and UNDE bits control the generation of an interrupt on the microprocessor INTB pin when a FIFO error event occurs. When OVRE or UNDE is set to logic 1, an overrun event or underrun event, respectively, is allowed to generate an interrupt on the INTB pin. When OVRE or UNDE is set to logic 0, the FIFO error events are disabled from generating an interrupt.

SYNC:

The SYNC bit enables the PLL to synchronize the phase delay between the FIFO input and output data to the phase delay between reference clock input and smooth output clock at the PLL. For example, if the PLL is operating so that the smooth output clock lags the reference clock by 24 UI, then the synchronization pulses that the PLL sends to the FIFO will force its output data to lag its input data by 24 UI. If the SYNC bit is set to 1, the Clock Divisors (Registers x19H and x1AH) must be set such that N1+1 and N2+1 is a multiple of 48.

LIMIT:

The LIMIT bit enables the PLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one unit interval (UI) of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 1, the PLL jitter attenuation is limited. When LIMIT is set to logic 0, the PLL is allowed to operate normally.

Registers 01CH, 11CH, 21CH and 31CH: T1-FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	M2O[1]	0
Bit 6	R/W	M2O[0]	0
Bit 5	R/W	ESFFA	0
Bit 4	R/W	ESF	0
Bit 3	R/W	FMS1	0
Bit 2	R/W	FMS0	0
Bit 1		Unused	X
Bit 0		Unused	X

These registers select the framing format and the frame loss criteria used by the T1-FRMR.

M2O[1:0]:

The M2O[1:0] bits select the ratio of errored to total framing bits before declaring out of frame in SF and ESF framing formats.

M2O[1:0]	Framing bit error ratio to declare OOF
00	2 out of 4
01	2 out of 5
10	2 out of 6
11	Reserved

ESFFA:

The ESFFA bit selects one of two framing algorithms for ESF frame search in the presence of mimic framing patterns in the incoming data. A logic 0 selects the ESF algorithm where the T1-FRMR does not declare inframe while more than one framing bit candidate is following the framing pattern in the incoming data. A logic 1 selects the ESF algorithm where a CRC-6 calculation is performed on each framing bit candidate, and is compared against the CRC bits associated with the framing bit candidate to determine the most likely framing bit position.

ESF, FMS[1], FMS[0]:

These bits are used to select the required T1 framing format. The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the following table:

ESF	FMS1	FMS0	Mode
0	0	0	Select SF format
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Select ESF framing format & 4 kbit FDL Data Rate
1	0	1	Select ESF framing format & 2 kbit FDL Data Rate using frames 3, 7, 11, 15, 19, and 23.
1	1	0	Select ESF framing format & 2 kbit FDL Data Rate using frames 1, 5, 9, 13, 17, and 21.
1	1	1	Reserved

Registers 01DH, 11DH, 21DH and 31DH: T1-FRMR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	COFAE	0
Bit 4	R/W	FERE	0
Bit 3	R/W	BEEE	0
Bit 2	R/W	SFEE	0
Bit 1	R/W	MFPE	0
Bit 0	R/W	INFRE	0

These registers select which of the MFP, COFA, FER, BEE, SFE, or INFR events generates an interrupt on the microprocessor INTB pin when their state changes or their event condition is detected.

Reserved:

The reserved bit must be programmed to logic 0 for correct operation.

COFAE:

The COFAE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the new alignment differs from the previous alignment. When COFAE is set to logic 1, the declaration of a change of frame alignment is allowed to generate an interrupt. When COFAE is set to logic 0, a change in the frame alignment does not generate an interrupt.

FERE:

The FERE bit enables the generation of an interrupt when a framing bit error has been detected. When FERE is set to logic 1, the detection of a framing bit error is allowed to generate an interrupt. When FERE is set to logic 0, any error in the framing bits does not generate an interrupt.

BEEE:

The BEEE bit enables the generation of an interrupt when a bit error event has been detected. A bit error event is defined as framing bit errors for SF formatted data, and CRC-6 errors for ESF formatted data. When BEEE is set to logic 1, the detection of a bit error event is allowed to generate an interrupt.

When BEEE is set to logic 0, bit error events are disabled from generating an interrupt.

SFEE:

The SFEE bit enables the generation of an interrupt when a severely errored framing event has been detected. A severely errored framing event is defined as 2 or more framing bit errors during the current superframe for SF and ESF formatted data. When SFEE is set to logic 1, the detection of a severely errored framing event is allowed to generate an interrupt. When SFEE is set to logic 0, severely errored framing events are disabled from generating an interrupt.

MFPE:

The MFPE bit enables the generation of an interrupt when the frame find circuitry detects the presence of framing bit mimics. The occurrence of a mimic is defined as more than one framing bit candidate following the frame alignment pattern. When MFPE is set to logic 1, the assertion or deassertion of the detection of a mimic is allowed to generate an interrupt. When MFPE is set to logic 0, the detection of a mimic framing pattern is disabled from generating an interrupt.

INFRE:

The INFRE bit enables the generation of an interrupt when the frame find circuitry changes state. When INFRE is set to logic 1, the assertion or deassertion of the "inframe" state is allowed to generate an interrupt. When INFRE is set to logic 0, a change in the "inframe" state is disabled from generating an interrupt.

Registers 01EH, 11EH, 21EH and 31EH: T1-FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	0
Bit 6	R	FERI	0
Bit 5	R	BEEI	0
Bit 4	R	SFEI	0
Bit 3	R	MFPI	0
Bit 2	R	INFRI	0
Bit 1	R	MFP	0
Bit 0	R	INFR	0

These registers indicate whether a change of frame alignment, a framing bit error, a bit error event, or a severely errored framing event generated an interrupt. These registers also indicate whether a mimic framing pattern was detected or whether there was a change in the framing state of the frame circuitry.

COFAI,FERI,BEEI,SFEI:

A logic 1 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the occurrence of the corresponding event generated an interrupt; a logic 0 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the corresponding event did not generate an interrupt.

MFPI:

A logic 1 in the MFPI status bit position indicates that the assertion or deassertion of the mimic detection indication has generated an interrupt; a logic 0 in the MFPI bit position indicates that no change in the state of the mimic detection indication occurred.

INFRI:

A logic 1 in the INFRI status bit position indicates that a change in the state of the frame alignment circuitry generated an interrupt; a logic 0 in the INFRI status bit position indicates that no state change occurred.

MFP,INFR:

The bit position MFP and INFR indicate the current state of the mimic detection and of the frame alignment circuitry.

The interrupt and the status bit positions (COFAI, FERI, BEEI, SFEI, MFPI, and INFRI) are cleared to logic 0 when this register is read.

Registers 020H, 120H, 220H and 320H: E1-FRMR Frame Alignment Options

Bit	Type	Function	Default
Bit 7	R/W	CRCEN	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	AFAA	0
Bit 4	R/W	CHKSEQ	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	REFR	0
Bit 1	R/W	REFCRCE	0
Bit 0	R/W	REFRDIS	0

These registers select the various framing formats and framing algorithms supported by the E1-FRMR blocks.

Reserved:

The reserved bits must be programmed to logic 0 for correct operation.

CRCEN:

The CRCEN bit enables the E1-FRMR to frame to the CRC multiframe. When the CRCEN bit is logic 1, the E1-FRMR searches for CRC multiframe alignment and monitors for errors in the alignment. A logic 0 in the CRCEN bit position disables searching for multiframe and suppresses the OOCMF, CRCE, CMFER, and FEBE E1-FRMR statuses, forcing them to logic 0.

AFAA:

The AFAA bit enables an alternate framing algorithm. If AFAA is a logic zero, frame alignment is declared after a correct FAS, a logic 1 in bit 2 of time slot 0 of the next frame and finally another FAS in the third frame are found. If one of the conditions fails, the next bit position is checked for valid framing. If AFAA is a logic one, the framing is similar to the above, but adds a "hold-off" feature. If bit2 or the second 7-bit FAS conditions fail, the same byte location is checked again in the subsequent frames before checking the next bit position for frame alignment.

CHKSEQ:

The CHKSEQ bit enables the use of the check sequence to verify the correct frame alignment in the presence of random imitative frame alignment signals.

A logic 1 in the CHKSEQ bit position enables the use of the check sequence algorithm in addition to the basic frame find algorithms; a logic 0 disables the use of the check sequence algorithm.

REFR:

A transition from logic 0 to logic 1 in the REFR bit position forces the re-synchronization to a new frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to generate subsequent re-synchronizations.

REFCRCE:

The REFCRCE bit enables excessive CRC errors (≥ 915 errors in one second) to force a re-synchronization to a new frame alignment. Setting the REFCRCE bit position to logic 1 enables reframe due to excessive CRC errors; setting the REFCRCE bit to logic 0 disables CRC errors from causing a reframe.

REFRDIS:

The REFRDIS bit disables reframing under any error condition once frame alignment has been found; reframing can be initiated by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the E1-FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur based on the various error criteria (FER, excessive CRC errors, etc).

Registers 021H, 121H, 221H and 321H: E1-FRMR Maintenance Mode Options

Bit	Type	Function	Default
Bit 7	R/W	FASC	0
Bit 6	R/WBit2C	0	
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	RADEB	0
Bit 2	R/W	Reserved	0
Bit 1	R	CMFACT	X
Bit 0	R	EXCRCE	X

Reserved:

The reserved bits must be programmed to logic 0 for correct operation.

FASC:

The FASC bit selects the criterion used to declare loss of frame alignment signal: a logic 0 in the FASC bit position enables declaration of loss of frame alignment when 3 consecutive frame alignment patterns have been received in error; a logic 1 in the FASC bit position enables declaration of loss of frame when 4 consecutive frame alignment pattern errors are detected.

BIT2C:

The BIT2C bit enables the additional criterion that loss of frame is declared when bit 2 in time slot 0 of NFAS frames has been received in error on 3 consecutive occasions: a logic 1 in the BIT2C position enables declaration of loss of frame alignment when bit 2 is received in error; a logic 0 in BIT2C enables declaration of loss of frame alignment based on the setting of FASC, only.

RADEB:

The RADEB bit selects the amount of debouncing applied to the Remote Alarm Indication before the RRA is allowed to change state: a logic 0 in the RADEB bit position enables the RRA output to change to the logic value contained in the Remote Alarm bit position (bit 3 of NFAS frames) when the received Remote Alarm bit value has been in the same state for 2 consecutive NFAS frames; a logic 1 in the RADEB bit position enables the

RRA output to change when the Remote Alarm bit has been in the same state for 3 consecutive NFAS frames.

CMFACT:

The CMFACT bit is an active high status bit indicating that the CRC Multiframe Find algorithm has been active for more than 8ms, thereby initiating a reframe if the CRCEN bit is set to logic 1. The CMFACT bit is reset to logic 0 after the register is read.

EXCRCE:

The EXCRCE bit is an active high status bit indicating that excessive CRC evaluation errors (i.e. ≥915 error in one second) have occurred, thereby initiating a reframe if enabled by the REFCRCE bit of the Frame Alignment Options register. The EXCRCE bit is reset to logic 0 after the register is read.

Registers 022H, 122H, 222H and 322H: E1-FRMR Framing Status Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	OOFE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	OOCMFE	0
Bit 3	R/W	COFAE	0
Bit 2	R/W	FERE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	CMFERE	0

Reserved:

The reserved bits must be programmed to logic 0 for correct operation.

OOFE, and OOCMFE:

A logic 1 in bits OOFE and OOCMFE enables the generation of an interrupt on a change of state of OOF and OOCMF bits, respectively, of the E1-FRMR Framing Status register.

COFAE:

A logic 1 in the COFAE bit enables the generation of an interrupt when the position of the frame alignment has changed.

FERE:

A logic 1 in the FERE bit enables the generation of an interrupt when an error has been detected in the frame alignment signal.

CMFERE:

A logic 1 in the CMFERE bit enables the generation of an interrupt when an error has been detected in the CRC multiframe alignment signal.

Registers 023H, 123H, 223H and 323H: E1-FRMR Maintenance/Alarm Status Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	RRAE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	REDE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	FEBEE	0
Bit 0	R/W	CRCEE	0

Reserved:

The reserved bits must be programmed to logic 0 for correct operation.

RRAE , AISDE, REDE, and AISE:

A logic one in bits RRAE, AISDE, REDE, or AISE enables the generation of an interrupt on a change of state of the RRA, AISD, RED, and AIS bits, respectively, of the E1-FRMR Maintenance/Alarm Status register.

FEBEE:

When the FEBEE bit is a logic one, an interrupt is generated when a logic zero is received in the Si bits of frames 13 or 15.

CRCEE:

When the CRCEE bit is a logic one, an interrupt is generated when calculated CRC differs from the received CRC remainder.

Registers 024H, 124H, 224H and 324H: E1-FRMR Framing Status Interrupt Indication

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	OOFI	X
Bit 5		Unused	X
Bit 4	R	OOCMFI	X
Bit 3	R	COFAI	X
Bit 2	R	FERI	X
Bit 1		Unused	X
Bit 0	R	CMFERI	X

A logic 1 in any bit position of these registers indicates which framing status has changed state.

OOFI, OOCMFI, and COFAI:

OOFI, OOCMFI, and COFAI indicate when the corresponding status has changed state. These bits are cleared when this register is read.

FERI, CMFERI:

FERI, CMFERI indicate when a framing error or CRC multiframe error event has been detected; these bits will be set if one or more errors have occurred since the last register read. These bits are cleared when this register is read.

Registers 025H, 125H, 225H and 325H: E1-FRMR Maintenance/Alarm Status Interrupt Indication

Bit	Type	Function	Default
Bit 7	R	RRAI	X
Bit 6		Unused	X
Bit 5	R	AISDI	X
Bit 4		Unused	X
Bit 3	R	REDI	X
Bit 2	R	AISI	X
Bit 1	R	FEBEI	X
Bit 0	R	CRCEI	X

A logic 1 in any bit position of these registers indicates which maintenance or alarm status has changed state.

RRAI, AISDI, REDI, and AISI:

RRAI, AISDI, REDI, and AISI indicate when the corresponding E1-FRMR Maintenance/Alarm Status register bit has changed state from logic 0 to logic 1 or vice-versa. These bits are cleared when this register is read.

FEBEI:

The FEBEI bit becomes a logic one when a FEBE indication is received in the Si bits of frames 13 or 15. This bit is cleared when this register is read.

CRCEI:

The CRCEI bit becomes a logic one when a calculated CRC differs from the received CRC remainder. This bit is cleared when this register is read.

Registers 026H, 126H, 226H and 326H: E1-FRMR Framing Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	OOF	X
Bit 5		Unused	X
Bit 4	R	OOCMF	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Reading these registers returns the current state value of the OOF and OOCMF framing statuses.

OOF:

The OOF bit is a logic 1 when basic frame alignment has been lost. The OOF bit is a logic 0 once frame alignment has been regained.

OOCMF:

The OOCMF bit is a logic 1 when the CRC multiframe alignment has been lost. The OOCMF bit is a logic 0 when CRC multiframe has been acquired.

Registers 027H, 127H, 227H and 327H: E1-FRMR Maintenance/Alarm Status

Bit	Type	Function	Default
Bit 7	R	RRA	X
Bit 6		Unused	X
Bit 5	R	AISD	X
Bit 4		Unused	X
Bit 3	R	RED	X
Bit 2	R	AIS	X
Bit 1		Unused	X
Bit 0		Unused	X

Reading these registers returns the current state value of the RRA, AISD, RED, and AIS maintenance/alarm statuses.

RRA:

The RRA bit is a logic one when the "A" bit (bit 3 in time slot 0 of the non-frame alignment signal frame) has been a logic one for 2 or 3 consecutive non-frame alignment signal frames, as determined by the RADEB bit in the E1-FRMR Maintenance Mode Options register.

AISD:

The AISD bit is a logic one after an unframed pattern of all ones with less than 3 zeros in two consecutive frame times (512 bits) has been detected. The AISD bit is updated every 512 bit times.

RED:

The RED bit is a logic one if an out of frame condition has persisted for 104 ms. The RED bit returns to a logic zero when a out of frame condition has been absent for 104 ms.

AIS:

The AIS bit is a logic one when an unframed all-ones condition has persisted for 104 ms. The AIS bit returns to a logic zero when the AIS condition has been absent for 104 ms.

Registers 028H, 128H, 228H and 328H: E1-FRMR International/National Bits

Bit	Type	Function	Default
Bit 7	R	Si[1]	X
Bit 6	R	Si[0]	X
Bit 5	R	RAWRA	X
Bit 4	R	Sn[4]	X
Bit 3	R	Sn[5]	X
Bit 2	R	Sn[6]	X
Bit 1	R	Sn[7]	X
Bit 0	R	Sn[8]	X

Reading this register returns the current bit value of the International and National bits collected over 2 consecutive frames. The Si[1] bit position corresponds to the value contained in the International bit position in the FAS frame; the Si[0], RAWRA, and Sn[4:8] bit positions correspond to the values contained in the International, Remote Alarm Indication, and National bit positions in the NFAS frame. This register is updated after time slot 0 of every NFAS frame and the contents are valid for 2 frames (250µs). The contents of this register are latched during the read, however the individual bits should not be considered to constitute a byte value (i.e. the 5 national bits should not be considered as indicating 1 of 32 possible values since it is possible that the individual bits are not all from the same time instant due to the asynchronous nature of the microprocessor reads). If the bits are to be interpreted as binary values, care should be taken to ensure a coherent set of bit values by reading the register at least twice.

The Si0, RAWRA and Sn[4:8] bits map to the timeslot 0 NFAS as follows:

Bit Position							
1	2	3	4	5	6	7	8
Si[0]	1	RAWRA	Sn[4]	Sn[5]	Sn[6]	Sn[7]	Sn[8]

Registers 02AH, 12AH, 22AH and 32AH: E1-FRMR CRC Error Counter - LSB

Bit	Type	Function	Default
Bit 7	R	CRCE7	X
Bit 6	R	CRCE6	X
Bit 5	R	CRCE5	X
Bit 4	R	CRCE4	X
Bit 3	R	CRCE3	X
Bit 2	R	CRCE2	X
Bit 1	R	CRCE1	X
Bit 0	R	CRCE0	X

These registers contain the least significant byte of the 10-bit CRC error counter value, updated every second.

Registers 02BH, 12BH, 22BH and 32BH: E1-FRMR CRC Error Counter - MSB

Bit	Type	Function	Default
Bit 7	R	OVR	0
Bit 6	R	NEWDATA	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CRCE9	X
Bit 0	R	CRCE8	X

These registers contain the most significant two bits of the 10-bit CRC error counter value, updated every second.

NEWDATA:

The NEWDATA flag bit indicates that the counter register contents have been updated with a new count value accumulated over the last 1 second interval. It is set to logic 1 when the CRC error counter data is transferred into the counter registers, and is reset to logic 0 when this register is read. This bit can be polled to determine the 1 second timing boundary used by the FRMR.

OVR:

The OVR flag bit indicates that the counter register contents have not been read within the last 1 second interval, and therefore have been over-written. It is set to logic 1 if CRC error counter data is transferred into the counter registers before the previous data has been read out, and is reset to logic 0 when this register is read.

This CRC error count is distinct from that of PMON because it is guaranteed to be an accurate count of the number of CRC error in one second; whereas, PMON relies on externally initiated transfers which may not be one second apart.

Registers 030H, 130H, 230H and 330H: RBOC Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	BOCE	0

These registers select the validation criteria to be used in determining a valid T1 bit oriented code (BOC) and enables generation of an interrupt on a change in code status.

IDLE:

The IDLE bit position enables the generation of an interrupt when there is a transition from a validated BOC to idle code (all ones). A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

AVC:

The AVC bit position selects the validation criteria used in determining a valid BOC. A logic 1 in the AVC bit position selects an "alternate" validation criterion of 4 out of 5 matching BOCs; a logic 0 selects the 8 out of 10 matching BOC criterion.

BOCE:

The BOCE bit position enables the generation of an interrupt on the INTB pin when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

Registers 031H, 131H, 231H and 331H: RBOC Code Status

Bit	Type	Function	Default
Bit 7	R	IDLEI	0
Bit 6	R	BOCI	0
Bit 5	R	BOC[5]	1
Bit 4	R	BOC[4]	1
Bit 3	R	BOC[3]	1
Bit 2	R	BOC[2]	1
Bit 1	R	BOC[1]	1
Bit 0	R	BOC[0]	1

These registers indicate the current state value of the BOC[5:0] bits and indicates whether an interrupt was generated by a change in the code value.

IDLEI:

The IDLEI bit position indicates whether a transition from a valid BOC to idle code (all ones) was detected. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle code was detected; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.

BOCI:

The BOCI bit position indicates whether a valid BOC code was detected. A logic 1 in the BOCI bit position indicates that a validated BOC code was detected; a logic 0 in the BOCI bit position indicates that no BOC has been detected. BOCI is cleared to logic 0 when the register is read.

Registers 034H, 134H, 234H and 334H: XFDL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	EOM	0
Bit 3	R/W	INTE	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	0
Bit 0	R/W	EN	0

EN:

The enable bit (EN) controls the overall operation of the XFDL. When the EN bit is set to a logic 1, the XDFL is enabled and flag sequences are sent until data is written into the XFDL Transmit Data register. When the EN bit is set to logic 0, the XFDL is disabled.

CRC:

The CRC enable bit controls the generation of the CRC-CCITT frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CRC-CCITT generator and the appends the 16 bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CRC-CCITT with generator polynomial = $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 11111110 code to be transmitted after the last byte from the XFDLTransmit Data Register is transmitted. Aborts are continuously sent until this bit is reset to a logic 0.

INTE:

The INTE bit enables the generation of an interrupt via the TDLINT[x] output. Setting the INTE bit to logic 1 enables the generation of an interrupt; setting INTE to logic 0 disables the generation of an interrupt. If the TDLINTE bit is also set to logic 1 in the Datalink Options register, the interrupt generated on the TDLINT[x] output is also generated on the microprocessor INTB pin.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared before transmission of the next data packet begins.

Registers 035H, 135H, 235H and 335H: XFDL Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	INT	1
Bit 0	R/W	UDR	0

INT:

The INT bit indicates when the XFDL is ready to accept a new data byte for transmission. The INT bit is set to a logic 1 when the previous byte in the XFDL Transmit Data register has been loaded into the parallel to serial converter and a new byte can be written into the XFDL Transmit Data register. The INT bit is set to a logic 0 while new data is in the Transmit Data register. The INT bit is not disabled by the INTE bit in the configuration register.

UDR:

The UDR bit indicates when the XFDL has underrun the data in the XFDL Transmit Data register. The UDR bit is set to a logic 1 if the parallel to serial conversion of the last byte in the XFDL Transmit Data register has completed before the new byte was written into the XFDL Transmit Data register. Once an underrun has occurred, the XFDL transmits an ABORT, followed by a flag, and waits to transmit the next valid data byte. If the UDR bit is still set after the transmission of the flag the XFDL will continuously transmit the all-ones idle pattern. **The UDR bit can only be cleared by writing a logic 0 to the UDR bit position in this register.**

Registers 036H, 136H, 236H and 336H: XFDL Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD7	X
Bit 6	R/W	TD6	X
Bit 5	R/W	TD5	X
Bit 4	R/W	TD4	X
Bit 3	R/W	TD3	X
Bit 2	R/W	TD2	X
Bit 1	R/W	TD1	X
Bit 0	R/W	TD0	X

Data written to this register is serialized and transmitted on the data link least significant bit first. The XFDL signals when the next data byte is required by setting the TDLINT[x] output high (if enabled) and by setting the INT bit in the XFDL Interrupt Status register high. When INT and/or TDLINT[x] is set, the Transmit Data register must be written with the new data within 4 data bit periods to prevent the occurrence of an underrun.

Registers 038H, 138H, 238H and 338H: RFDL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN:

The enable bit (EN) controls the overall operation of the RFDL. When set, the RDFL is enabled; when reset, the RFDL is disabled. When the block is disabled, the FIFO and interrupts are all cleared; however, the programming of the Enable/Status Register is not affected. When the block is enabled, it will immediately begin looking for flags.

TR:

Setting the terminate reception bit (TR) forces the RFDL to immediately terminate the reception of the current HDLC frame, empty the FIFO, clear the interrupts, and begin searching for a new flag sequence. The RFDL handles the TR input in the same manner as if the EN bit had been cleared and then set. The TR bit in the Configuration register will reset itself after a rising and falling edge have occurred on the datalink clock input to the RFDL once the write to this register has completed. If the Configuration register is read after this time, the TR bit value returned will be zero.

Registers 039H, 139H, 239H and 339H: RFDL Interrupt Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTC1	0
Bit 1	R/W	INTC0	0
Bit 0	R	INT	0

INTC1,INTC0:

The INTC1 and INTC0 bits control when an interrupt is asserted based on the number of received data bytes in the FIFO as follows:

INTC1	INTC0	Description
0	0	Disable interrupts (All sources)
0	1	Enable interrupt when FIFO receives data
1	0	Enable interrupt when FIFO has 2 bytes of data
1	1	Enable interrupt when FIFO has 3 bytes of data

INT:

The INT bit reflects the status of the external RDLINT[x] interrupt unless the INTC1 and INTC0 bits are set to disable interrupts. In that case, the RDLINT[x] output is forced to 0 and the INT bit of the RFDL Interrupt Control/Status register will reflect the state of the internal interrupt latch.

In addition to the FIFO fill status, interrupts are also generated for EOM (end of message), OVR (FIFO overrun), detection of the abort sequence while not receiving all ones, and on detection of the first flag while receiving all ones. The interrupt is reset by a RFDL Receive Data Register read that empties the FIFO, unless the cause of the interrupt was due to a FIFO overrun. The interrupt due to a FIFO overrun is cleared by a Status register read, by disabling the block, or by setting TR high.

The contents of the RFDL Interrupt Control/Status register should only be changed when the RFDL is disabled to prevent any erroneous interrupt generation.

Registers 03AH, 13AH, 23AH and 33AH: RFDL Status

Bit	Type	Function	Default
Bit 7	R	FE	1
Bit 6	R	OVR	0
Bit 5	R	FLG	0
Bit 4	R	EOM	0
Bit 3	R	CRC	0
Bit 2	R	NVB2	1
Bit 1	R	NVB1	1
Bit 0	R	NVB0	1

NVB[2:0]:

The NVB[2:0] bit positions indicate the number of valid bits in the RFDL Receive Data Register byte. It is possible that not all of the bits in the Receive Data Register are valid when the last data byte is read since the data frame can be any number of bits in length and not necessarily an integral number of bytes. The Receive Data Register is filled from the MSB to the LSB bit position, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0]. A NVB[2:0] value of 000 binary indicates that only the MSB in the register is valid. NVB[2:0] is only valid when the EOM bit is a logic 1 and the FLG bit is a logic 1 and the OVR bit is a logic 0.

CRC:

The CRC bit is set if a CRC error was detected in the last received HDLC frame. The CRC bit is only valid when EOM is logic 1 and FLG is a logic 1 and OVR is a logic 0.

On an interrupt generated from the detection of first flag, reading this register will return invalid NVB[2:0] and CRC bits, even though the EOM bit is logic 1 and the FLG bit is logic 1.

EOM:

The End of Message bit (EOM) follows the RDLEOM[x] output. It is set when:

1) The last byte in the HDLC frame (EOM) is being read from the RFDL Receive Data Register,

2) An abort sequence is detected while not in the receiving all-ones state and the byte, written to the FIFO due to the detection of the abort sequence, is being read from the FIFO,

3) The first flag has been detected and the dummy byte, written into the FIFO when the RFDL changes from the receiving all-ones state to the receiving flags state, is being read from the FIFO,

4) Immediately on detection of FIFO overrun.

The EOM bit is passed through the FIFO with the Data so that the Status will correspond to the Data just read from the FIFO.

FLG:

The flag bit (FLG) is set if the RFDL has detected the presence of the HDLC flag sequence (01111110) in the data. FLG is reset only when the HDLC abort sequence (01111111) is detected in the data or when the RFDL is disabled. This bit is passed through the FIFO with the Data so that the Status will correspond to the Data just read from the FIFO. The reception of bit-oriented codes over the data link will also force an abort due to its eight ones pattern.

OVR:

The Receiver Overrun bit (OVR) is set when data is written over unread data in the FIFO. This bit is not reset until after the Status register is read. While OVR is high, the RFDL and FIFO are held in the reset state, causing the FLG and EOM bits in the status register to be reset also.

FE:

The FIFO Empty bit (FE) is high when the last FIFO entry is read and goes low when the FIFO is loaded with new data.

If the RFDL Receive Data register is read while there is no valid data, then a FIFO underrun condition occurs. The underrun condition is reflected in the Status register by forcing all bits to logic zero on the first Status register read immediately following the Received Data register read which caused the underrun condition.

Registers 03BH, 13BH, 23BH and 33BH: RFDL Receive Data

Bit	Type	Function	Default
Bit 7	R	RD7	X
Bit 6	R	RD6	X
Bit 5	R	RD5	X
Bit 4	R	RD4	X
Bit 3	R	RD3	X
Bit 2	R	RD2	X
Bit 1	R	RD1	X
Bit 0	R	RD0	X

RD0 corresponds to the first bit of the serial byte received by the RFDL.

These registers are actually 4 level FIFOs. If data is available, the FE bit in the Status register is low. If INTC[1:0] (in the Enable/Status register) is set to 01, the Receive Data register must be read within 31 data bit periods to prevent an overrun. If INTC[1:0] is set to 11 the Receiver Data register must be read within 15 data bit periods.

When an overrun is detected, an interrupt is generated and the FIFO is held cleared until the Status register is read. When the HDLC abort sequence (01111111) is detected in the data an ABORT interrupt is generated and the data that has been shifted into the serial to parallel converter is written into the FIFO.

A read of the Receive Data register increments the FIFO pointer at the end of the read. If the Receive Data register read causes a FIFO underrun, then the pointer is inhibited from incrementing. The underrun condition will be signaled in the next Status read by returning all zeros.

Registers 03CH, 13CH, 23CH and 33CH: IBCD Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	DSEL1	0
Bit 2	R/W	DSEL0	0
Bit 1	R/W	ASEL1	0
Bit 0	R/W	ASEL0	0

These registers provide the selection of the Activate and De-activate T1 loopback code lengths (from 3 bits to 8 bits) as follows:

DEACTIVATE Code		ACTIVATE Code		CODE LENGTH
DSEL1	DSEL0	ASEL1	ASEL0	
0	0	0	0	5 bits
0	1	0	1	6 (or 3*) bits
1	0	1	0	7 bits
1	1	1	1	8 (or 4*) bits

***Note:**

3 and 4 bit code sequences can be accommodated by configuring the IBCD for 6 or 8 bits and by programming two repetitions of the code sequence.

Reserved:

The reserved bit must be programmed to logic 0 for correct operation.

Registers 03DH, 13DH, 23DH and 33DH: IBCD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R	LBACP	0
Bit 6	R	LBDCP	0
Bit 5	R/W	LBAE	0
Bit 4	R/W	LBDE	0
Bit 3	R	LBAI	0
Bit 2	R	LBDI	0
Bit 1	R	LBA	0
Bit 0	R	LBD	0

LBACP,LBDCP:

The LBACP and LBDCP bits indicate when the corresponding loopback code is present during a 39.8 ms interval.

LBAE:

The LBAE bit enables the assertion or deassertion of the inband Loopback Activate (LBA) detect indication to generate an interrupt on the INTB pin. When LBAE is set to logic 1, any change in the state of the LBA detect indication generates an interrupt. When LBAE is set to logic 0, no interrupt is generated by changes in the LBA detect state.

LBDE:

The LBDE bit enables the assertion or deassertion of the inband Loopback Deactivate (LBD) detect indication to generate an interrupt on the INTB pin. When LBDE is set to logic 1, any change in the state of the LBD detect indication generates an interrupt. When LBDE is set to logic 0, no interrupt is generated by changes in the LBD detect state.

LBAI,LBDI:

The LBAI and LBDI bits indicate which of the two expected loopback codes has changed state. A logic 1 in these bit positions indicate that a state change in that code has occurred; a logic 0 in these bit positions indicate that no state change has occurred.

LBA,LBD:

The LBA and LBD bits indicate the current state of the corresponding loopback code detect indication. A logic 1 in these bit positions indicate the presence of that code has been detected; a logic 0 in these bit positions indicate the absence of that code.

Registers 03EH, 13EH, 23EH and 33EH: IBCD Activate Code

Bit	Type	Function	Default
Bit 7	R/W	ACT7	0
Bit 6	R/W	ACT6	0
Bit 5	R/W	ACT5	0
Bit 4	R/W	ACT4	0
Bit 3	R/W	ACT3	0
Bit 2	R/W	ACT2	0
Bit 1	R/W	ACT1	0
Bit 0	R/W	ACT0	0

This 8 bit register selects the Activate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8 bit register. For example, if code sequence is a repeating 00001, then the first 8 bits of two repetitions (0000100001) is programmed into the register, i.e.00001000. Note that bit ACT7 corresponds to the first code bit received.

Registers 03FH, 13FH, 23FH and 33FH: IBCD Deactivate Code

Bit	Type	Function	Default
Bit 7	R/W	DACT7	0
Bit 6	R/W	DACT6	0
Bit 5	R/W	DACT5	0
Bit 4	R/W	DACT4	0
Bit 3	R/W	DACT3	0
Bit 2	R/W	DACT2	0
Bit 1	R/W	DACT1	0
Bit 0	R/W	DACT0	0

This 8 bit register selects the Deactivate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8 bit register. For example, if code sequence is a repeating 001, then the first 8 bits of three repetitions (001001001) is programmed into the register, i.e.00100100. Note that bit DACT7 corresponds to the first code bit received.

Registers 040H, 140H, 240H and 340H: T1-TRAN Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	B8ZS	0
Bit 4	R/W	ESF	0
Bit 3	R/W	FMS1	0
Bit 2	R/W	FMS0	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

The reserved bit must be programmed to logic 0 for correct operation.

B8ZS:

The B8ZS bit enables B8ZS line coding. When B8ZS is a logic 1, the transmit T1 stream is B8ZS encoded. When B8ZS is a logic 0, the transmit T1 stream is AMI encoded.

ZCS1	ZCS0	Zero Code Suppression Format
0	0	None
0	1	GTE Zero Code Suppression (Bit 8 of an all zero channel byte is replaced by a one, except in signalling frames where bit 7 is forced to a one.)
1	0	DDS Zero Code Suppression (All zero data byte replaced with "10011000")
1	1	Bell Zero Code Suppression (Bit 7 of an all zero channel byte is replaced by a one.)

ESF, FMS[1], FMS[0]:

These bits are used to select the required T1 framing format. The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

ESF	FMS1	FMS0	Mode
0	0	0	Select SF format
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Select ESF framing format & 4 kbit FDL Data Rate
1	0	1	Select ESF framing format & 2 kbit FDL Data Rate (frames 3, 7, 11, 15, 19, 23)
1	1	0	Select ESF framing format & 2 kbit FDL Data Rate (frames 1, 5, 9, 13, 17, 21).
1	1	1	Reserved

Registers 041H, 141H, 241H and 341H: T1-TRAN Alarm Transmit

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	XYEL	0
Bit 0	R/W	XAIS	0

These registers control the transmission of T1 yellow or AIS Carrier Failure Alarms (CFA).

XYEL:

The XYEL bit enables the TRAN to generate a yellow alarm in the appropriate framing format. When XYEL is set to logic 1, the TRAN is enabled to set bit 2 of each channel to logic 0 for SF format and to transmit repetitions of 1111111100000000 (the yellow alarm bit oriented code) on the facility data link for ESF format. When XYEL is set to logic 0, the TRAN is disabled from generating the yellow alarm.

XAIS:

The XAIS bit enables the TRAN to generate an unframed all-ones AIS alarm. When XAIS is set to logic 1, the TDP/TDN[x] outputs are forced to pulse alternately, creating an all-ones signal. When XAIS is set to logic 0, the TDP/TDN[x] outputs operate normally.

Registers 042H, 142H, 242H and 342H: XIBC Control

Bit	Type	Function	Default
Bit 7	R/W	EN	0
Bit 6	R/W	UF	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	CL1	0
Bit 0	R/W	CL0	0

These registers control the transmission of T1 inband loopback activate and deactivate codes.

EN:

The EN bit controls whether the inband code is transmitted or not. A logic 1 in the EN bit position enables transmission of inband codes; a logic 0 in the EN bit position disables inband code transmission.

UF:

The UF bit controls whether the code is transmitted framed or unframed. A logic 1 in the UF bit position selects unframed inband code transmission; a logic 0 in the UF bit position selects framed inband code transmission. Note: the UF register bit controls the T1-TRAN directly and is not qualified by the EN bit. When UF is set to logic 1, the TRAN is disabled and no framing is inserted regardless of the setting of EN. *The UF bit should only be written to logic 1 when the EN bit is set, and should be cleared to logic 0 when the EN bit is cleared.*

CL1, CL0:

The bit positions CL[1:0] (bits 1 & 0) of this register indicate the length of the inband loopback code sequence, as follows:

CL1	CL0	Code Length
0	0	5
0	1	6
1	0	7
1	1	8

Codes of 3 or 4 bits in length may be accommodated by treating them as half of a double-sized code (i.e. a 3-bit code would use the 6-bit code length setting).

Registers 043H, 143H, 243H and 343H: XIBC Loopback Code

Bit	Type	Function	Default
Bit 7	R/W	IBC7	X
Bit 6	R/W	IBC6	X
Bit 5	R/W	IBC5	X
Bit 4	R/W	IBC4	X
Bit 3	R/W	IBC3	X
Bit 2	R/W	IBC2	X
Bit 1	R/W	IBC1	X
Bit 0	R/W	IBC0	X

These registers contain the inband loopback code pattern to be transmitted. The code is transmitted most significant bit (IBC7) first, followed by IBC6 and so on. The code, regardless of the length, must be aligned with the MSB always in the IBC7 position (e.g., a 5-bit code would occupy the IBC7 through IBC2 bit positions). To transmit a 3-bit or a 4-bit code pattern, the pattern must be paired to form a double-sized code (i.e., the 3-bit code '011' would be written as the 6-bit code '011011').

Registers 044H, 144H, 244H and 344H: E1-TRAN Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6	R/W	SIGEN	1
Bit 5	R/W	DLEN	1
Bit 4	R/W	GENCRC	0
Bit 3	R/W	FDIS	0
Bit 2	R/W	FEBEDIS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

These registers configure the TRAN block when E1 format is enabled

Reserved:

The reserved bit must be programmed to logic 0 for correct operation.

AMI:

The AMI bit enables AMI line coding when set to logic 1; when it is set to logic 0, the HDB3 line coding is enabled.

SIGEN, DLEN:

The SIGEN and DLEN bits select the signalling data source for Time Slot 16 (TS16) as follows:

SIGEN	DLEN	MODE
0	0	TS16 insertion disabled. TS16 is set to all ones.
0	1	TS16 insertion enabled. TS16 data is taken directly from the TDLSIG input or from the HDLC transmitter.
1	0	Reserved.
1	1	TS16 insertion disabled. TS16 is set to all ones.

When channel associated signalling (CAS) is enabled, the format of the input BTSIG stream is selected by the DLEN bit. A logic 1 in the DLEN bit position selects the PMC compatible format in which the BTSIG stream contains the

signalling data nibble in the lower four bits of the time slot byte. A logic 0 in the DLEN bit position is reserved and should not be used.

GENCRC:

The GENCRC bit enables generation of the CRC multiframe. When GENCRC is a logic 1, the E1-TRAN generates the CRC multiframe alignment signal, calculates and inserts the CRC bits, and if enabled by FEBEDIS, inserts the FEBE indication in the spare bit positions. When GENCRC is set to logic 0, the CRC generation is disabled. The CRC bits are then set to the logic value contained in the Si[1] bit position in the International/National Bit Control Register and bit 1 of the NFAS frames are set to the value of Si[0] bit.

FDIS:

The FDIS bit value controls the generation of the framing alignment signal. A logic 1 in the FDIS bit position disables the generation of the framing pattern in TS0. A logic 0 in FDIS enables the generation of the framing pattern, replacing TS0 of frames 0,2,4,6,8,10,12,14 with the frame alignment signal. When FDIS is a logic 1, framing is globally disabled and the values in controls bits GENCRC and FEBEDIS are ignored.

Note that the above is true only if the AIS bit in the Transmit Alarm / Diagnostic Control Register is a logic 0. If AIS is logic 1, the output bit stream becomes all ones unconditionally.

GENCRC and FEBEDIS:

When FDIS is a logic 0, the bit values used for the International and National bits are dependent upon the values of the GENCRC and FEBEDIS configuration bits, as follows:

GENCRC	FEBEDIS	Source of International/National bits
0	X	Bit Si[1] of the International/National Control Register is used for the International bit in the frame alignment signal (FAS) frames and the Si[0] bit is used for the International bit in the non-frame alignment signal (NFAS) frames. Bits Sn[4:8] in the register are used for the National bits in NFAS frames.

GENCRC	FEBEDIS	Source of International/National bits
1	0	The calculated CRC bits are used for the International bit in the FAS frames and the generated CRC multiframe alignment signal and the FEBE bits are used for the International bit in the NFAS frames. Bit positions Sn[4:0] in the International/National Control Register are used for the National bits in NFAS frames.
1	1	The calculated CRC bits are used for the International bit in the FAS frames and the generated CRC multiframe alignment signal is used for the International bit in the NFAS frames, with the Si[1:0] bits in the International/National Control Register used for the spare bits. Bit positions Sn[4:0] in the register are used for the National bits in NFAS frames.

Registers 045H, 145H, 245H and 345H: E1-TRAN Transmit Alarm/Diagnostic Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	FPATINV	0
Bit 5	R/W	SPLRINV	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	REMAIS	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	AIS	0

Reserved:

The reserved bit must be programmed to logic 0 for correct operation.

FPATINV:

The FPATINV bit is a diagnostic control bit. When set to logic 1, FPATINV forces the frame alignment signal (FAS) written into TS0 to be inverted (i.e., the correct FAS, 0011011, is substituted with 1100100). When set to logic 0, the FAS is unchanged.

SPLRINV:

The SPLRINV bit is a diagnostic control bit. When set to logic 1, SPLRINV forces the "spoiler bit" written into bit 2 of TS0 of NFAS frames to be inverted (i.e., the spoiler bit is forced to 0); when set to logic 0, the spoiler bit is unchanged.

REMAIS:

The REMAIS bit controls the transmission of the remote alarm indication signal. A logic 1 in the REMAIS bit position causes bit 3 of NFAS frames to be forced to logic 1; otherwise, bit 3 of NFAS frames is determined by the settings in the Transmit Configuration Register.

AIS:

The AIS bit enables the TRAN to generate an unframed all-ones AIS alarm. When AIS is set to logic 1, the TDP/TDN[x] outputs are forced to pulse

alternately, creating an all-ones signal. When AIS is set to logic 0, the TDP/TDN[x] outputs operate normally.

Registers 046H, 146H, 246H and 346H: E1-TRAN International/National Control

Bit	Type	Function	Default
Bit 7	R/W	Si[1]	1
Bit 6	R/W	Si[0]	1
Bit 5		Unused	X
Bit 4	R/W	Sn[4]	1
Bit 3	R/W	Sn[5]	1
Bit 2	R/W	Sn[6]	1
Bit 1	R/W	Sn[7]	1
Bit 0	R/W	Sn[8]	1

Sn[4:8]:

Sn[4:8] of this register are substituted in bit positions 4 to 8, respectively, of TS0 of each NFAS frame when framing generation (FDIS = 0) is enabled. When FDIS is logic 1, the contents of this register are ignored and replaced with either the TS0 datalink bits (if enabled) or random arbitrary data from the serial input to the E1 TRAN block.

Si[1:0]:

The bits Si[1] and Si[0] correspond to the International bits. The Si[1] and Si[0] bits can be programmed to any value and will be inserted into bit 1 of each FAS frame and NFAS frame, respectively, when CRC multiframe generation is disabled. When CRC multiframe generation is enabled, both Si[1] and Si[0] are ignored if FEBE indication is enabled; if FEBEDIS is a logic 1 the values programmed in the Si[1] and Si[0] bit positions are inserted into the spare bit locations of frame 13 and frame 15, respectively, of the CRC multiframe.

Registers 048H, 148H, 248H and 348H: PMON Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INT	0
Bit 0	R	OVR	0

These registers enable an interrupt to be generated on the INTB pin whenever counter data is transferred into the holding registers. The configuration register also contains status information as to whether the holding registers have been overrun.

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt. A logic 0 bit in the INTE position disables the generation of an interrupt.

INT:

The INT bit is the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer has occurred. A logic 0 indicates that no transfer has occurred. The interrupt is cleared (acknowledged) by reading this register.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

11.1 Registers x49-x4FH: Latching Performance Data

All the Performance Data registers for one of the four interfaces on the S/UNI-MPH are updated as a group by writing to any of the PMON count registers (addresses x49H-x4FH). A write to any of these locations loads performance data located in the PMON block into the internal holding registers. The data contained in the holding registers can then be subsequently read by microprocessor accesses into the PMON block count register address space. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed. NOTE: it is necessary to write to one, and only one, count register address to latch all the count data register values into the holding registers and to reset all the counters for each polling cycle.

Alternately, one may write to the Global Monitoring Update register (00CH) to transfer the contents of each of the four PMON blocks, along with ATM cell monitoring information from each of the four RXCP and TXCP blocks at the same time. The transfer in progress (TIP) bit in register 00CH is polled to determine when the transfer is complete.

Registers 049H, 149H, 249H and 349H: PMON Framing Bit Error Count

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FER[6]	X
Bit 5	R	FER[5]	X
Bit 4	R	FER[4]	X
Bit 3	R	FER[3]	X
Bit 2	R	FER[2]	X
Bit 1	R	FER[1]	X
Bit 0	R	FER[0]	X

These registers indicate the number of framing bit error events that occurred during the previous accumulation interval. When T1-SF format is enabled, the counter accumulates Ft and Fs bit errors. When T1-ESF format is enabled, the counter accumulates Fe bit errors. When E1 format is enabled, the counter accumulates frame alignment signal (FAS) bit errors.

Registers 04AH, 14AH, 24AH and 34AH: PMON Far End Block Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Registers 04BH, 14BH, 24BH and 34BH: PMON Far End Block Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

When the E1-CRC multiframe format is enabled, these registers indicate the number of far end block error events that occurred during the previous accumulation interval.

Registers 04CH, 14CH, 24CH and 34CH: PMON CRC Error Count LSB

Bit	Type	Function	Default
Bit 7	R	CRCE[7]	X
Bit 6	R	CRCE[6]	X
Bit 5	R	CRCE[5]	X
Bit 4	R	CRCE[4]	X
Bit 3	R	CRCE[3]	X
Bit 2	R	CRCE[2]	X
Bit 1	R	CRCE[1]	X
Bit 0	R	CRCE[0]	X

Registers 04DH, 14DH, 24DH and 34DH: PMON CRC Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CRCE[9]	X
Bit 0	R	CRCE[8]	X

These registers indicate the number of CRC error events that occurred during the previous accumulation interval. When T1-ESF format is enabled, the counter accumulates CRC-6 errors. When E1-CRC multiframe format is enabled, the counter accumulates CRC-4 errors.

Registers 04EH, 14EH, 24EH and 34EH: PMON Line Code Violation Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Registers 04FH, 14FH, 24FH and 34FH: PMON Line Code Violation Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

These registers indicate the number of LCV error events that occurred during the previous accumulation interval. An LCV event is defined as the occurrence of a Bipolar Violation or Excessive Zeros (>7 consecutives zeros for T1 B8ZS, >15 consecutive zeros for T1 AMI, or >3 consecutive zeros for E1 AMI or E1 HDB3). The counting of Excessive Zeros can be disabled by the BPV bit of the Receive Interface Configuration register.

Registers 055H, 155H, 255H and 355H: PDVD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	PDV	0
Bit 3	R	Z16DI	0
Bit 2	R	PDVI	0
Bit 1	R/W	Z16DE	0
Bit 0	R/W	PDVE	0

These registers are used to monitor pulse density violations when the T1 format is enabled.

PDVE:

The PDVE bit enables an interrupt to be generated on the INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist. When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt is generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation state occurs. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read.

PDV:

The PDV bit indicates the current state of the pulse density violation detector. When PDV is a logic 1, a violation of the pulse density rule has been

detected. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time. Therefore, reading this bit may not return a logic 1 even though a pulse density violation has occurred.

Registers 057H, 157H, 257H and 357H: XBOC Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BC[5]	1
Bit 4	R/W	BC[4]	1
Bit 3	R/W	BC[3]	1
Bit 2	R/W	BC[2]	1
Bit 1	R/W	BC[1]	1
Bit 0	R/W	BC[0]	1

These registers enable the XBOC to generate a bit oriented code and selects the 6-bit code to be transmitted.

When this register is written with any 6-bit code other than 111111, that code will be transmitted repeatedly in the T1-ESF Facility Data Link with the format 111111110[BC0][BC1][BC2][BC3][BC4][BC5]0, overwriting any HDLC packets currently being transmitted. When the register is written with 111111, the XBOC is disabled.

Registers 059H, 159H, 259H and 359H: XPDE Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	STUFE	0
Bit 6	R/W	STUFF	0
Bit 5	R	STUFI	0
Bit 4	R	PDV	0
Bit 3	R	Z16DI	0
Bit 2	R	PDVI	0
Bit 1	R/W	Z16DE	0
Bit 0	R/W	PDVE	0

These registers are used to enforce a minimum pulse density in the transmit stream when the T1 format is enabled.

STUFE:

The STUFE bit enables the occurrence of pulse stuffing to generate an interrupt on INTB. When STUFE is set to logic 1, an interrupt is generated on the occurrence of a bit stuff. When STUFE is a logic 0, bit stuffing occurrences do not generate an interrupt on INTB.

STUFF:

The STUFF bit enables pulse stuffing to occur upon detection of a violation of the pulse density rule. Bit stuffing is performed in such a way that the resulting data stream no longer violates the pulse density rule. When STUFF is set to logic 1, bit stuffing is enabled and the STUFI bit indicates the occurrence of bit stuffs. When STUFF is a logic 0, bit stuffing is disabled and the PDVI bit indicates an occurance of a pulse density violation. Also, when STUFF is a logic 0, transmit data passes through XPDE unaltered.

STUFI:

The STUFI bit is valid when pulse stuffing is active. This bit indicates when a bit stuff occurred to eliminate a pulse density violation. When pulse stuffing is active, PDVI remains logic 0, indicating that the stuffing has removed the density violation. The STUFI bit is reset to logic 0 once this register is read.

PDV:

The PDV bit indicates the current state of the pulse density violation detector. When PDV is a logic 1, a violation of the pulse density rule exists. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading this bit may not return a logic 1 even though a pulse density violation has occurred. When the XPDE is enabled for pulse stuffing, PDV remains logic 0.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether the corresponding interrupt enables are enabled or disabled. When STUFF is set to logic 1, the PDVI and Z16DI bits are forced to logic 0.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the INTB pin when 16 consecutive zeros are detected in the transmit T1 stream. When Z16DE is set to logic 1, interrupt generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVE:

The PDVE bit enables an interrupt to be generated on the INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist (if STUFE is logic 0). When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

Registers 064H, 164H, 264H and 364H: RXCP Uncorrectable HCS Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	UHCSE[7]	X
Bit 6	R	UHCSE[6]	X
Bit 5	R	UHCSE[5]	X
Bit 4	R	UHCSE[4]	X
Bit 3	R	UHCSE[3]	X
Bit 2	R	UHCSE[2]	X
Bit 1	R	UHCSE[1]	X
Bit 0	R	UHCSE[0]	X

Registers 065H, 165H, 265H and 365H: RXCP Uncorrectable HCS Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	UHCSE[11]	X
Bit 2	R	UHCSE[10]	X
Bit 1	R	UHCSE[9]	X
Bit 0	R	UHCSE[8]	X

UHCSE[11:0]:

UHCSE[11:0] represents the number of uncorrectable header check sequence (UHCS) errors that have been detected since the last time the UHCSE error counter was polled. The counter (and all other counters in the S/UNI-MPH) is polled by writing to the Global Monitoring register (00CH). Such a write transfers the internally accumulated count to the UHCSE Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. The transfer in progress (TIP) bit in register 00CH is polled to determine when the transfer is complete. The CPPM counters in each quadrant can also be polled by writing to any address from X60H to X6FH (where X is a value from 0 to 3). UHCS errors are not accumulated when the RXCP has declared an out of cell delineation defect state.

Note that every time that the RXCP loses cell delineation and goes from the SYNC state to the HUNT state (see the Cell Delineation State Diagram located in the Receive ATM Cell Processor (RXCP) Functional Description section), the UHCSE counter will lose 1 occurance of an UHCSE (eg. UHCSE count will be 6 instead of 7 on 1 transition to the HUNT state).

Registers 068H, 168H, 268H and 368H: RXCP Correctable HCS Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	CHCSE[7]	X
Bit 6	R	CHCSE[6]	X
Bit 5	R	CHCSE[5]	X
Bit 4	R	CHCSE[4]	X
Bit 3	R	CHCSE[3]	X
Bit 2	R	CHCSE[2]	X
Bit 1	R	CHCSE[1]	X
Bit 0	R	CHCSE[0]	X

Registers 069H, 169H, 269H and 369H: RXCP Correctable HCS Error Event Count MSB

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R	CHCSE[11]
Bit 2	R	CHCSE[10]
Bit 1	R	CHCSE[9]
Bit 0	R	CHCSE[8]

CHCSE[11:0]:

CHCSE[11:0] represents the number of correctable header check sequence (CHCS) errors that have been detected since the last time the CHCSE error counter was polled. The counter (and all other counters in the S/UNI-MPH) is polled by writing to the Global Monitoring register (00CH). Such a write transfers the internally accumulated count to the CHCSE Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. The transfer in progress (TIP) bit in register 00CH is polled to determine when the transfer is complete. The CPPM counters in each quadrant can also be polled by writing to any address from X60H to X6FH (where X is a value from 0 to 3). CHCS errors are not accumulated when the RXCP has declared an out of cell delineation defect state.

Registers 06AH, 16AH, 26AH and 36AH: RXCP Idle/Unassigned Cell Count LSB

Bit	Type	Function	Default
Bit 7	R	UICELL[7]	X
Bit 6	R	UICELL[6]	X
Bit 5	R	UICELL[5]	X
Bit 4	R	UICELL[4]	X
Bit 3	R	UICELL[3]	X
Bit 2	R	UICELL[2]	X
Bit 1	R	UICELL[1]	X
Bit 0	R	UICELL[0]	X

Registers 06BH, 16BH, 26BH and 36BH: RXCP Idle/Unassigned Cell Count MSB

Bit	Type	Function	Default
Bit 7	R	UICELL[15]	X
Bit 6	R	UICELL[14]	X
Bit 5	R	UICELL[13]	X
Bit 4	R	UICELL[12]	X
Bit 3	R	UICELL[11]	X
Bit 2	R	UICELL[10]	X
Bit 1	R	UICELL[9]	X
Bit 0	R	UICELL[8]	X

UICELL [15:0]:

UICELL[15:0] represents the number of idle/unassigned cells that have been dropped since the last time the idle/unassigned cell counter was polled. Note that this counter operates only when idle/unassigned cell filtering is enabled. The counter (and all other counters in the S/UNI-MPH) is polled by writing to the Global Monitoring register (00CH). Such a write transfers the internally accumulated count to the UICELL Cell Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. The transfer in progress (TIP) bit in register 00CH is polled to determine when the transfer is complete. The CPPM counters in each quadrant can also be polled by writing to any address from X60H to X6FH (where X is a value from 0 to 3). Idle/Unassigned Cells are not accumulated when the RXCP has declared an out of cell delineation defect state.

Registers 06CH, 16CH, 26CH and 36CH: RXCP Receive Cell Count LSB

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Registers 06DH, 16DH, 26DH and 36DH: RXCP Receive Cell Count MSB

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

RCELL[15:0]:

RCELL[15:0] represents the aggregate number of cells that have been written to the receive FIFO since the last time the idle/unassigned cell counter was polled. Note that this counter represents the number error-free (or error-corrected), assigned cells that have been received when idle/unassigned cell filtering and HCS error filtering are enabled. The counter (and all other counters in the S/UNI-MPH) is polled by writing to the Global Monitoring register (00CH). Such a write transfers the internally accumulated count to the UICELL Cell Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. The transfer in progress (TIP) bit in register 00CH is polled to determine when the transfer is complete. The CPPM counters in each quadrant can also be polled by writing to any address from X60H to X6FH (where X is a value from 0 to 3). Cells are not passed through the RXCP when an out of cell delineation defect state is declared.

Registers 06EH, 16EH, 26EH and 36EH: TXCP Transmit Cell Count LSB

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Registers 06FH, 16FH, 26FH and 36FH: TXCP Transmit Cell Count MSB

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

TCELL[15:0]:

TCELL[15:0] represents the aggregate number of assigned cells that have been transmitted since the last time the transmit cell counter was polled. The counter (and all other counters in the S/UNI-MPH) is polled by writing to the Global Monitoring register (00CH). Such a write transfers the internally accumulated count to the UICELL Cell Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. The transfer in progress (TIP) bit in register 00CH is polled to determine when the transfer is complete. The CPPM counters in each quadrant can also be polled by writing to any address from X60H to X6FH (where X is a value from 0 to 3).

Registers 070H, 170H, 270H and 370H: RXCP Control

Bit	Type	Function	Default
Bit 7	R/W	HCSPASS	0
Bit 6	R/W	HCSDQDB	0
Bit 5	R/W	HCSADD	0
Bit 4	R/W	HCK	0
Bit 3	R/W	BLOCK	0
Bit 2	R/W	DSCR	0
Bit 1	R	OOCDV	X
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the receive FIFO. When a logic 1 is written to FIFORST, the FIFO is immediately emptied, and incoming assigned cells are ignored. When a logic 0 is written to FIFORST, the receive FIFO operates normally.

OOCDV:

The OOCDV bit indicates the current out of cell delineation defect state. When an HCS error is detected in seven consecutive cells, OOCDV is set to logic 1. When six consecutive cells containing no HCS errors are detected, OOCDV is set to logic 0.

DSCR:

The DSCR bit controls cell payload descrambling using the self-synchronizing polynomial $x^{43} + 1$. When a logic 1 is written to DSCR, payload descrambling is enabled. When a logic 0 is written to DSCR, payload descrambling is disabled.

BLOCK:

The BLOCK bit enables idle/unassigned and user-programmable cell filtering. When a logic 1 is written to BLOCK, idle/unassigned cells or user-programmed cells corresponding to the pattern specified in the Idle/Unassigned Cell Pattern and User-programmable Cell Pattern Registers, and their associated Cell Mask Registers, are blocked. When a logic 0 is written to BLOCK, only idle/unassigned cells or user-programmed cells corresponding to the pattern specified in the Idle/Unassigned Cell Pattern and

User-programmable Cell Pattern Registers, and their associated Cell Mask Registers, are passed through the FIFO.

HCK:

The HCK bit controls a FIFO data path integrity check. The integrity check consists of inserting either an alternating AAH/55H pattern, or a fixed 55H pattern, in the HCS octet location as selected by the FIXPAT bit in the RXCP Framing Control register. The AA/55H pattern alternates with each cell written to the FIFO. An external device reading cells from the receive FIFO verifies that either the alternating or the fixed pattern is present in the cell stream. Any pattern discrepancy indicates a failure in the receive data path. When a logic 1 is written to HCK, the data path integrity check is enabled, and the HCS octet location is overwritten with the alternating pattern. When a logic 0 is written to HCK, the received HCS value is passed unaltered through the FIFO.

HCSADD:

The HCSADD bit enables the addition of the coset polynomial $x^6 + x^4 + x^2 + 1$ to the received HCS octet before comparison with the calculated result as required by the ATM Forum UNI specification. When a logic 1 is written to HCSADD, the coset polynomial is added to the HCS. When a logic 0 is written to HCSADD, the unmodified HCS value is compared with the calculated result.

HCSDQDB:

The HCSDQDB bit controls the cell header octets included in the HCS calculation. When a logic 1 is written to HCSDQDB, header octets two, three, and four are used in the HCS calculation as required by the IEEE-802.6 DQDB specification. When a logic 0 is written to HCSDQDB, all four header octets are used in the HCS calculation as required by the ATM Forum UNI specification, and the ITU-T Recommendation I.432.

HCSPASS:

The HCSPASS bit enables cells containing HCS errors to be passed through the receive FIFO. When a logic 1 is written to HCSPASS, cells containing detectable HCS errors are written to the receive FIFO. When a logic 0 is written to HCSPASS, cells containing detectable HCS errors are dropped. Note that all cells are dropped while an out of cell delineation defect is detected.

Registers 071H, 171H, 271H and 371H: RXCP Framing Control

Bit	Type	Function	Default
Bit 7	R/W	REMPTY4	0
Bit 6	R/W	LCDE	0
Bit 5	R	LCDI	X
Bit 4	R	LCD	X
Bit 3	R/W	FIXPAT	0
Bit 2	R/W	DETHYST[1]	0
Bit 1	R/W	DETHYST[0]	0
Bit 0	R/W	Reserved	0

RESERVED:

The Reserved bit can be programmed to either 1 or 0.

DETHYST[1:0]:

The DETHYST[1:0] bits control the cell acceptance threshold after an HCS error is detected. This feature is enabled when the HCSPASS bit in the RXCP Control Register is written with a logic 0. Upon detecting an HCS error, cells continue to be dropped until a number of consecutive cells are received that contain no HCS errors. The number of consecutive cells is indicated below:

DETHYST[1:0]	Cell Acceptance Threshold
00	The first cell containing an error-free HCS
01	The second consecutive cell containing no HCS errors.
10	The fourth consecutive cell containing no HCS errors.
11	The eighth consecutive cell containing no HCS errors.

FIXPAT:

The FIXPAT bit enables the insertion of a fixed 55H pattern into the HCS when the FIFO data path integrity check is enabled by the HCK bit in the RXCP Control register. When FIXPAT is logic 1, the pattern forced into the

HCS byte exiting the FIFO is 55H. When FIXPAT is logic 0, the pattern force in the HCS byte is an alternating AAH/55H pattern which alternate every cell.

LCD:

The LCD bit indicates the state of the Loss of Cell Delineation indication. When LCD is logic 1, an out of cell delineation (OCD) defect has persisted for a programmable time (see the RXCP LCD Count Threshold register),

LCDI:

The LCDI bit is set to logic 1 when the state of loss of cell delineation (LCD) changes. The LCDI bit position is set to logic 0 when this register is read.

LCDE:

The LCDE bit enables the generation of an interrupt when the LCD state changes. When a logic 1 is written to the LCDE bit position, the interrupt generation is enabled.

REMPTY4:

The REMPTY4 bit selects the amount of advance indication given on the receive cell available (RCA) signal. When REMPTY4 is logic 1, RCA is deasserted when the receive FIFO is almost empty and can accept no more than four byte read requests before having no more cells available to be read. When REMPTY4 is logic 0, RCA is deasserted to logic 0 when the receive FIFO can accept no more read requests (if a read request is made while RCA is low, the read request is ignored).

Registers 072H, 172H, 272H and 372H: RXCP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	OOCDE	0
Bit 6	R/W	HCSE	0
Bit 5	R/W	FIFOE	0
Bit 4	R	OOCDI	X
Bit 3	R	UHCSI	X
Bit 2	R	Reserved	X
Bit 1	R	FOVRI	X
Bit 0		Unused	X

FOVRI:

The FOVRI bit is set to logic 1 when the receive FIFO has overrun. The FOVRI bit position is set to logic 0 when this register is read.

Reserved:

This bit provides no useful functional information for S/UNI-MPH applications.

UHCSI:

The UHCSI bit is set to logic 1 when an uncorrectable header check sequence (HCS) error is detected. The UHCSI bit position is set to logic 0 when this register is read.

OOCDI:

The OOCDI bit is set to logic 1 when an out of cell delineation (OOCD) defect is detected or removed. The OOCD defect state is contained in the RXCP Control Register. The OOCDI bit position is set to logic 0 when this register is read.

FIFOE:

The FIFOE bit enables the generation of an interrupt a receive FIFO overrun, or a change of cell alignment (COCA) is detected. When a logic 1 is written to FIFOE, the interrupt generation is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt when an HCS error is detected. When a logic 1 is written to HCSE, the interrupt generation is enabled.

OOCDE:

The OOCDE bit enables the generation of an interrupt when an out of cell delineation defect is declared or removed. When a logic 1 is written to OOCDE, the interrupt generation is enabled.

Registers 073H, 173H, 273H and 373H: RXCP Idle/Unassigned Cell Pattern: H1 octet

Bit	Type	Function	Default
Bit 7	R/W	CP[7]	0
Bit 6	R/W	CP[6]	0
Bit 5	R/W	CP[5]	0
Bit 4	R/W	CP[4]	0
Bit 3	R/W	CP[3]	0
Bit 2	R/W	CP[2]	0
Bit 1	R/W	CP[1]	0
Bit 0	R/W	CP[0]	0

CP[7:0]:

The CP[7:0] bits contain the idle/unassigned cell header pattern to match in the first octet (H1) of the received cell in conjunction with the H1 octet mask. The BLOCK bit, in the RXCP Control Register, determines whether to block or pass cells matching this pattern. This register should be set to 00H when filtering the standard idle/unassigned cell pattern.

Registers 074H, 174H, 274H and 374H: RXCP Idle/Unassigned Cell Pattern: H2 octet

Bit	Type	Function	Default
Bit 7	R/W	CP[7]	0
Bit 6	R/W	CP[6]	0
Bit 5	R/W	CP[5]	0
Bit 4	R/W	CP[4]	0
Bit 3	R/W	CP[3]	0
Bit 2	R/W	CP[2]	0
Bit 1	R/W	CP[1]	0
Bit 0	R/W	CP[0]	0

CP[7:0]:

The CP[7:0] bits contain the idle/unassigned cell header pattern to match in the second octet (H2) of the received cell in conjunction with the H2 octet mask. The BLOCK bit, in the RXCP Control Register, determines whether to block or pass cells matching this pattern. This register should be set to 00H when filtering the standard idle/unassigned cell pattern.

Registers 075H, 175H, 275H and 375H: RXCP Idle/Unassigned Cell Pattern: H3 octet

Bit	Type	Function	Default
Bit 7	R/W	CP[7]	0
Bit 6	R/W	CP[6]	0
Bit 5	R/W	CP[5]	0
Bit 4	R/W	CP[4]	0
Bit 3	R/W	CP[3]	0
Bit 2	R/W	CP[2]	0
Bit 1	R/W	CP[1]	0
Bit 0	R/W	CP[0]	0

CP[7:0]:

The CP[7:0] bits contain the idle/unassigned cell header pattern to match in the third octet (H3) of the received cell in conjunction with the H3 octet mask. The BLOCK bit, in the RXCP Control Register, determines whether to block or pass cells matching this pattern. This register should be set to 00H when filtering the standard idle/unassigned cell pattern.

Registers 076H, 176H, 276H and 376H: RXCP Idle/Unassigned Cell Pattern: H4 octet

Bit	Type	Function	Default
Bit 7	R/W	CP[7]	0
Bit 6	R/W	CP[6]	0
Bit 5	R/W	CP[5]	0
Bit 4	R/W	CP[4]	0
Bit 3	R/W	CP[3]	0
Bit 2	R/W	CP[2]	0
Bit 1	R/W	CP[1]	0
Bit 0	R/W	CP[0]	0

CP[7:0]:

The CP[7:0] bits contain the idle/unassigned cell header pattern to match in the fourth octet (H4) of the received cell in conjunction with the H4 octet mask. The BLOCK bit, in the RXCP Control Register, determines whether to block or pass cells matching this pattern. By default, unassigned cells are transmitted. This register should be set to 01H to filter idle cells.

Registers 077H, 177H, 277H and 377H: RXCP Idle/Unassigned Cell Mask: H1 octet

Bit	Type	Function	Default
Bit 7	R/W	CPM[7]	0
Bit 6	R/W	CPM[6]	0
Bit 5	R/W	CPM[5]	0
Bit 4	R/W	CPM[4]	0
Bit 3	R/W	CPM[3]	0
Bit 2	R/W	CPM[2]	0
Bit 1	R/W	CPM[1]	0
Bit 0	R/W	CPM[0]	0

CPM[7:0]:

The CPM[7:0] bits contain the idle/unassigned cell header mask for the first octet (H1) of the received cell. This mask is applied to the H1 octet pattern. A logic 1 in any CPM[n] bit enables the corresponding bit in the H1 Idle/Unassigned Cell Pattern Register to be compared with the received H1 octet. A logic 0 causes the masking of the corresponding bit. This register should be set to FFH when filtering the standard unassigned cell pattern.

Registers 078H, 178H, 278H and 378H: RXCP Idle/Unassigned Cell Mask: H2 octet

Bit	Type	Function	Default
Bit 7	R/W	CPM[7]	0
Bit 6	R/W	CPM[6]	0
Bit 5	R/W	CPM[5]	0
Bit 4	R/W	CPM[4]	0
Bit 3	R/W	CPM[3]	0
Bit 2	R/W	CPM[2]	0
Bit 1	R/W	CPM[1]	0
Bit 0	R/W	CPM[0]	0

CPM[7:0]:

The CPM[7:0] bits contain the idle/unassigned cell header mask for the second octet (H2) of the received cell. This mask is applied to the H2 octet pattern. A logic 1 in any CPM[n] bit enables the corresponding bit in the H2 Idle/Unassigned Cell Pattern Register to be compared with the received H2 octet. A logic 0 causes the masking of the corresponding bit. This register should be set to FFH when filtering the standard unassigned cell pattern.

Registers 079H, 179H, 279H and 379H: RXCP Idle/Unassigned Cell Mask: H3 octet

Bit	Type	Function	Default
Bit 7	R/W	CPM[7]	0
Bit 6	R/W	CPM[6]	0
Bit 5	R/W	CPM[5]	0
Bit 4	R/W	CPM[4]	0
Bit 3	R/W	CPM[3]	0
Bit 2	R/W	CPM[2]	0
Bit 1	R/W	CPM[1]	0
Bit 0	R/W	CPM[0]	0

CPM[7:0]:

The CPM[7:0] bits contain the idle/unassigned cell header mask for the third octet (H3) of the received cell. This mask is applied to the H3 octet pattern. A logic 1 in any CPM[n] bit enables the corresponding bit in the H3 Idle/Unassigned Cell Pattern Register to be compared with the received H3 octet. A logic 0 causes the masking of the corresponding bit. This register should be set to FFH when filtering the standard unassigned cell pattern.

Registers 07AH, 17AH, 27AH and 37AH: RXCP Idle/Unassigned Cell Mask: H4 octet

Bit	Type	Function	Default
Bit 7	R/W	CPM[7]	0
Bit 6	R/W	CPM[6]	0
Bit 5	R/W	CPM[5]	0
Bit 4	R/W	CPM[4]	0
Bit 3	R/W	CPM[3]	0
Bit 2	R/W	CPM[2]	0
Bit 1	R/W	CPM[1]	0
Bit 0	R/W	CPM[0]	0

CPM[7:0]:

The CPM[7:0] bits contain the idle/unassigned cell header mask for the fourth octet (H4) of the received cell. This mask is applied to the H4 octet pattern. A logic 1 in any CPM[n] bit enables the corresponding bit in the H4 Idle/Unassigned Cell Pattern Register to be compared with the received H4 octet. A logic 0 causes the masking of the corresponding bit. This register should be set to FFH when filtering the standard unassigned cell pattern.

Registers 07BH, 17BH, 27BH and 37BH: RXCP User-Programmable Match Pattern: H1 octet

Bit	Type	Function	Default
Bit 7	R/W	UPH1[7]	0
Bit 6	R/W	UPH1[6]	0
Bit 5	R/W	UPH1[5]	0
Bit 4	R/W	UPH1[4]	0
Bit 3	R/W	UPH1[3]	0
Bit 2	R/W	UPH1[2]	0
Bit 1	R/W	UPH1[1]	0
Bit 0	R/W	UPH1[0]	0

UPH1[7:0]:

This register contains the pattern to match in the first octet (H1) of the received cell in conjunction with User-Programmable Match Mask for H1. The BLOCK bit, in the RXCP Configuration/ Control register, determines whether to pass or discard cells matching this pattern.

Registers 07CH, 17CH, 27CH and 37CH: RXCP User-Programmable Match Pattern: H2 octet

Bit	Type	Function	Default
Bit 7	R/W	UPH2[7]	0
Bit 6	R/W	UPH2[6]	0
Bit 5	R/W	UPH2[5]	0
Bit 4	R/W	UPH2[4]	0
Bit 3	R/W	UPH2[3]	0
Bit 2	R/W	UPH2[2]	0
Bit 1	R/W	UPH2[1]	0
Bit 0	R/W	UPH2[0]	0

UPH2[7:0]:

This register contains the pattern to match in the second octet (H2) of the received cell in conjunction with the User-Programmable Match Mask for H2. The BLOCK bit, in the RXCP Configuration/Control register, determines whether to pass or discard cells matching this pattern.

Registers 07DH, 17DH, 27DH and 37DH: RXCP User-Programmable Match Pattern: H3 octet

Bit	Type	Function	Default
Bit 7	R/W	UPH3[7]	0
Bit 6	R/W	UPH3[6]	0
Bit 5	R/W	UPH3[5]	0
Bit 4	R/W	UPH3[4]	0
Bit 3	R/W	UPH3[3]	0
Bit 2	R/W	UPH3[2]	0
Bit 1	R/W	UPH3[1]	0
Bit 0	R/W	UPH3[0]	0

UPH3[7:0]:

This register contains the pattern to match in the third octet (H3) of the received cell in conjunction with the User-Programmable Match Mask for H3. The BLOCK bit, in the RXCP Configuration/Control register, determines whether to pass or discard cells matching this pattern.

Registers 07EH, 17EH, 27EH and 37EH: RXCP User-Programmable Match Pattern: H4 octet

Bit	Type	Function	Default
Bit 7	R/W	UPH4[7]	0
Bit 6	R/W	UPH4[6]	0
Bit 5	R/W	UPH4[5]	0
Bit 4	R/W	UPH4[4]	0
Bit 3	R/W	UPH4[3]	0
Bit 2	R/W	UPH4[2]	0
Bit 1	R/W	UPH4[1]	0
Bit 0	R/W	UPH4[0]	0

UPH4[7:0]:

This register contains the pattern to match in the fourth octet (H4) of the received cell in conjunction with the User-Programmable Match Mask for H4. The BLOCK bit, in the RXCP Configuration/Control register, determines whether to pass or discard cells matching this pattern.

Registers 07FH, 17FH, 27FH and 37FH: RXCP User-Programmable Match Mask: H1 octet

Bit	Type	Function	Default
Bit 7	R/W	UPMH1[7]	0
Bit 6	R/W	UPMH1[6]	0
Bit 5	R/W	UPMH1[5]	0
Bit 4	R/W	UPMH1[4]	0
Bit 3	R/W	UPMH1[3]	0
Bit 2	R/W	UPMH1[2]	0
Bit 1	R/W	UPMH1[1]	0
Bit 0	R/W	UPMH1[0]	0

UPMH1[7:0]:

This register contains the mask pattern for the first octet (H1) of a received cell. This mask is applied to User-Programmable Match Pattern for H1. A one in any UPMH1[n] bit enables the corresponding bit in the Match Pattern register to be compared. A zero causes the masking of the corresponding bit.

Registers 080H, 180H, 280H and 380H: RXCP User-Programmable Match Mask: H2 octet

Bit	Type	Function	Default
Bit 7	R/W	UPMH2[7]	0
Bit 6	R/W	UPMH2[6]	0
Bit 5	R/W	UPMH2[5]	0
Bit 4	R/W	UPMH2[4]	0
Bit 3	R/W	UPMH2[3]	0
Bit 2	R/W	UPMH2[2]	0
Bit 1	R/W	UPMH2[1]	0
Bit 0	R/W	UPMH2[0]	0

UPMH2[7:0]:

This register contains the mask pattern for the second octet (H2) of a received cell. This mask is applied to User-Programmable Match Pattern for H2. A one in any UPMH2[n] bit enables the corresponding bit in the Match Pattern register to be compared. A zero causes the masking of the corresponding bit.

Registers 081H, 181H, 281H and 381H: RXCP User-Programmable Match Mask: H3 octet

Bit	Type	Function	Default
Bit 7	R/W	UPMH3[7]	0
Bit 6	R/W	UPMH3[6]	0
Bit 5	R/W	UPMH3[5]	0
Bit 4	R/W	UPMH3[4]	0
Bit 3	R/W	UPMH3[3]	0
Bit 2	R/W	UPMH3[2]	0
Bit 1	R/W	UPMH3[1]	0
Bit 0	R/W	UPMH3[0]	0

UPMH3[7:0]:

This register contains the mask pattern for the third octet (H3) of a received cell. This mask is applied to User-Programmable Match Pattern for H3. A one in any UPMH3[n] bit enables the corresponding bit in the Match Pattern register to be compared. A zero causes the masking of the corresponding bit.

Registers 082H, 182H, 282H and 382H: RXCP User-Programmable Match Mask: H4 octet

Bit	Type	Function	Default
Bit 7	R/W	UPMH4[7]	0
Bit 6	R/W	UPMH4[6]	0
Bit 5	R/W	UPMH4[5]	0
Bit 4	R/W	UPMH4[4]	0
Bit 3	R/W	UPMH4[3]	0
Bit 2	R/W	UPMH4[2]	0
Bit 1	R/W	UPMH4[1]	0
Bit 0	R/W	UPMH4[0]	0

UPMH4[7:0]:

This register contains the mask pattern for the fourth octet (H4) of a received cell. This mask is applied to User-Programmable Match Pattern for H4. A one in any UPMH4[n] bit enables the corresponding bit in the Match Pattern register to be compared. A zero causes the masking of the corresponding bit.

Registers 083H, 183H, 283H and 383H: RXCP HCS Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CHCSI	X
Bit 0	R/W	HECEN	0

HECEN:

When logic 0, the HECEN bit disables the HCS error correction routine. When logic 1, the HCS error correction routine is run to correct HCS single-bit errors.

CHCSI:

When logic 1, the CHCSI bit indicates that an interrupt due to the reception of a correctable header check sequence (HCS). This bit is reset immediately after a read to this register.

Registers 084H, 184H, 284H and 384H: RXCP LCD Count Threshold

Bit	Type	Function	Default
Bit 7	R/W	LCDC[7]	1
Bit 6	R/W	LCDC[6]	0
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	1
Bit 3	R/W	LCDC[3]	0
Bit 2	R/W	LCDC[2]	1
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC [7:0]:

The LCDC[7:0] bits represent half the number of consecutive cell periods for which the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Similarly, LCD is not deasserted until the receive cell processor is in cell delineation for a number of cell periods equal to twice the contents of LCDC[7:0].

The LCDC[7:0] bits determine the LCD integration time. The default value of 180 sets the cell threshold to 360. This translates to the following LCD integration periods:

Format	Average cell period	Default LCD integration period
DS1 Direct Mapping	276 µs	99.4 ms
E1 Direct Mapping	213.7 µs	76.9 ms

Registers 088H, 188H, 288H and 388H: TXCP Control

Bit	Type	Function	Default
Bit 7	R/W	HCSINS	0
Bit 6	R/W	HCSDQDB	0
Bit 5	R/W	HCSADD	0
Bit 4	R/W	FIFODP[1]	0
Bit 3	R/W	FIFODP[0]	0
Bit 2	R/W	SCR	0
Bit 1	R/W	DHCS	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the transmit FIFO. When a logic 1 is written to FIFORST, the FIFO is immediately emptied, and idle/unassigned cells are transmitted. When a logic 0 is written to FIFORST, the transmit FIFO operates normally.

DHCS:

The DHCS bit controls the insertion of header check sequence (HCS) errors in the transmit stream. When a logic 1 is written to DHCS, a single HCS error is inserted in each transmitted cell. When a logic 0 is written to DHCS, the HCS is calculated and inserted normally.

SCR:

The SCR bit controls cell payload scrambling using the self synchronizing polynomial $x^{43} + 1$. When a logic 1 is written to SCR, payload scrambling is enabled. When a logic 0 is written to SCR, payloads are transmitted unscrambled.

FIFODP[1:0]:

The FIFODP[1:0] bits determine the transmit FIFO cell depth. FIFO depth control may be important in systems where the cell latency through the S/UNI-MPH must be minimized. When the FIFO is filled to the specified depth, the transmit FIFO full signal, TCA[x] is logic 0. TCA[x] is asserted only after a complete cell has been read out; therefore, the current cell being read is included in the count. The selectable FIFO cell depths are shown in the following table:

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

Note that FIFODP[1:0] only affects when TCA is asserted. All four cells of the FIFO may be filled before an overflow is declared.

It is not recommended that the FIFO depth be set to 1 cell. If a cell write is initiated only when TCA is asserted to logic 1, half the bandwidth is lost to idle/unassigned cells. For minimum latency and maximum throughput, set the FIFO depth to 2 cells.

HCSADD:

The HCSADD bit enables the addition of the coset polynomial $x^6 + x^4 + x^2 + 1$ to the HCS octet before transmission as required by the ATM Forum UNI specification. When a logic 1 is written to HCSADD, the coset polynomial is added to the HCS. When a logic 0 is written to HCSADD, the calculated HCS value is inserted, unmodified into the transmit cell. HCSINS must be set to logic 1 for HCSADD to have any effect.

HCSDQDB:

The HCSDQDB bit controls the cell header octets included in the HCS calculation. When a logic 1 is written to HCSDQDB, header octets two, three, and four are used in the HCS calculation as required by the IEEE-802.6 DQDB specification. When a logic 0 is written to HCSDQDB, all four header octets are used in the HCS calculation as required by the ATM Forum UNI specification, and the ITU-T Recommendation I.432.

HCSINS:

The HCSINS bit controls the insertion of the calculated header check sequence (HCS) in the transmit stream. When a logic 1 is written to HCSINS, the calculated HCS overwrites the HCS placeholder octet position in the cell that is read from the transmit FIFO. When a logic 0 is written to HCSINS, the value passed through the FIFO in the HCS placeholder octet position is inserted unmodified in the transmit cell. The HCS value is calculated and inserted externally when HCSINS is a logic 0.

Registers 089H, 189H, 289H and 389H: TXCP Interrupt Enable/Status and Control

Bit	Type	Function	Default
Bit 7	R/W	FIXPAT	0
Bit 6	R/W	HCKE	0
Bit 5	R/W	FIFOE	0
Bit 4	R/W	TFULL4	0
Bit 3	R	HCKI	X
Bit 2	R	COCAI	X
Bit 1	R	FOVRI	X
Bit 0		Unused	X

FOVRI:

The FOVRI bit is set to logic 1 when the transmit FIFO has overrun. The FOVRI bit position is set to logic 0 when this register is read.

COCAI:

The COCAI bit is set to logic 1 when a change of cell alignment (COCA) is detected. Start of cell indications are indicated by the TSOC input, and are expected during the first octet of the 53 octet data structure written to the transmit FIFO. If the FIFO's internal cell counter indicates that TSOC does not coincide with the first octet or is not present during the first octet, COCAI is set to logic 1. The COCAI bit position is set to logic 0 when this register is read.

HCKI:

The HCKI bit is set to logic 1 when a FIFO data path integrity error is detected. An external device must insert either an alternating AAH/55H or a fixed 55H pattern in the HCS octet placeholder location (the AAH/55H pattern alternates with each cell written to the transmit FIFO). The TXCP verifies that either the alternating or the fixed pattern is present in the data structure read from the transmit FIFO. Any pattern discrepancy indicates a failure in the transmit data path, and causes HCKI to be set to a logic 1. The HCKI bit position is set to logic 0 when this register is read.

TFULL4:

The TFULL4 bit selects the amount of advance indication given on the transmit cell available (TCA[x]) signal. When TFULL4 is logic 1, TCA[x] is removed when the transmit FIFO is almost full and can accept no more than four bytes before reaching the depth specified by the FIFODP[1:0] register bits. When TFULL4 is logic 0, TCA[x] is removed when the current FIFO access writes the last octet of a cell which fills the FIFO to the specified depth

FIFOE:

The FIFOE bit enables the generation of an interrupt when a transmit FIFO overrun, or a change of cell alignment (COCA) is detected. When a logic 1 is written to FIFOE, the interrupt generation is enabled.

HCKE:

The HCKE bit enables the generation of an interrupt when a FIFO datapath integrity error is detected. When a logic 1 is written to HCKE, the interrupt generation is enabled.

FIXPAT:

The FIXPAT bit selects the pattern used when FIFO data path integrity checking is enabled. When FIXPAT is logic 1, the HCS octet placeholder location is checked for the fixed 55H pattern. When FIXPAT is logic 0, the HCS octet placeholder location is checked for an alternating AAH/55H pattern which alternates with each cell written to the transmit FIFO.

Registers 08AH, 18AH, 28AH and 38AH: TXCP Idle/Unassigned Cell Pattern: H1 octet

Bit	Type	Function	Default
Bit 7	R/W	H1[7]	0
Bit 6	R/W	H1[6]	0
Bit 5	R/W	H1[5]	0
Bit 4	R/W	H1[4]	0
Bit 3	R/W	H1[3]	0
Bit 2	R/W	H1[2]	0
Bit 1	R/W	H1[1]	0
Bit 0	R/W	H1[0]	0

H1[7:0]:

The H1[7:0] bits contain the cell header pattern inserted in the first octet (H1) of the idle/unassigned cell. Idle/unassigned cells are inserted when the S/UNI-MPH detects that the transmit FIFO contains no outstanding cells. H1[7] is the most significant bit and is the first bit transmitted. H1[0] is the least significant bit. This register should be set to 00H when transmitting the standard idle/unassigned cell pattern.

Registers 08BH, 18BH, 28BH and 38BH: TXCP Idle/Unassigned Cell Pattern: H2 octet

Bit	Type	Function	Default
Bit 7	R/W	H2[7]	0
Bit 6	R/W	H2[6]	0
Bit 5	R/W	H2[5]	0
Bit 4	R/W	H2[4]	0
Bit 3	R/W	H2[3]	0
Bit 2	R/W	H2[2]	0
Bit 1	R/W	H2[1]	0
Bit 0	R/W	H2[0]	0

H2[7:0]:

The H2[7:0] bits contain the cell header pattern inserted in the second octet (H2) of the idle/unassigned cell. Idle/unassigned cells are inserted when the S/UNI-MPH detects that the transmit FIFO contains no outstanding cells. H2[7] is the most significant bit and is the first bit transmitted. H2[0] is the least significant bit. This register should be set to 00H when transmitting the standard idle/unassigned cell pattern.

Registers 08CH, 18CH, 28CH and 38CH: TXCP Idle/Unassigned Cell Pattern: H3 octet

Bit	Type	Function	Default
Bit 7	R/W	H3[7]	0
Bit 6	R/W	H3[6]	0
Bit 5	R/W	H3[5]	0
Bit 4	R/W	H3[4]	0
Bit 3	R/W	H3[3]	0
Bit 2	R/W	H3[2]	0
Bit 1	R/W	H3[1]	0
Bit 0	R/W	H3[0]	0

H3[7:0]:

The H3[7:0] bits contain the cell header pattern inserted in the third octet (H3) of the idle/unassigned cell. Idle/unassigned cells are inserted when the S/UNI-MPH detects that the transmit FIFO contains no outstanding cells. H3[7] is the most significant bit and is the first bit transmitted. H3[0] is the least significant bit. This register should be set to 00H when transmitting the standard idle/unassigned cell pattern.

Registers 08DH, 18DH, 28DH and 38DH: TXCP Idle/Unassigned Cell Pattern: H4 octet

Bit	Type	Function	Default
Bit 7	R/W	H4[7]	0
Bit 6	R/W	H4[6]	0
Bit 5	R/W	H4[5]	0
Bit 4	R/W	H4[4]	0
Bit 3	R/W	H4[3]	0
Bit 2	R/W	H4[2]	0
Bit 1	R/W	H4[1]	0
Bit 0	R/W	H4[0]	0

H4[7:0]:

The H4[7:0] bits contain the cell header pattern inserted in the fourth octet (H4) of the idle/unassigned cell. Idle/unassigned cells are inserted when the S/UNI-MPH detects that the transmit FIFO contains no outstanding cells. H4[7] is the most significant bit and is the first bit transmitted. H4[0] is the least significant bit. By default, unassigned cells are transmitted. This register should be set to 01H to transmit idle cells.

Registers 08EH, 18EH, 28EH and 38EH: TXCP Idle/Unassigned Cell Pattern: H5 octet

Bit	Type	Function	Default
Bit 7	R/W	H5[7]	0
Bit 6	R/W	H5[6]	0
Bit 5	R/W	H5[5]	0
Bit 4	R/W	H5[4]	0
Bit 3	R/W	H5[3]	0
Bit 2	R/W	H5[2]	0
Bit 1	R/W	H5[1]	0
Bit 0	R/W	H5[0]	0

H5[7:0]:

The H5[7:0] bits contain the cell header pattern inserted in the fifth octet (H5, the HCS octet) of the idle/unassigned cell. Idle/unassigned cells are inserted when the S/UNI-MPH detects that the transmit FIFO contains no outstanding cells. H5[7] is the most significant bit and is the first bit transmitted. H5[0] is the least significant bit. This register should be written with the correct header check sequence value corresponding to the patterns written to the H1 - H4 octet Idle/Unassigned Cell Pattern Registers.

Registers 08FH, 18FH, 28FH and 38FH: TXCP Idle/Unassigned Cell Payload

Bit	Type	Function	Default
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	0
Bit 5	R/W	PAYLD[5]	0
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	0
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	0
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]:

The PAYLD[7:0] bits contain the pattern inserted in the idle/unassigned cell payload. Idle/unassigned cells are inserted when the S/UNI-MPH detects that the transmit FIFO contains no outstanding cells. PAYLD[7] is the most significant bit and is the first bit transmitted. PAYLD[0] is the least significant bit.

12 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-MPH. Test mode registers (as opposed to normal mode registers) are mapped into addresses 400H-7FFH.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the S/UNI-MPH are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 00BH: Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	A_TM[9]	X
Bit 5	R/W	A_TM[8]	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select S/UNI-MPH test features. All bits, except for PMCTST and A_TM[9:8], are reset to zero by a hardware reset of the S/UNI-MPH. A software reset of the S/UNI-MPH does not affect the state of the bits in this register. Refer to the Test Features Description section for more information.

A_TM[9]:

The state of the A_TM[9] bit internally replaces the input address line A[9] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

A_TM[8]:

The state of the A_TM[8] bit internally replaces the input address line A[8] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

PMCTST:

The PMCTST bit is used to configure the S/UNI-MPH for PMC's manufacturing tests. When PMCTST is set to logic 1, the S/UNI-MPH microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin

high causes the S/UNI-MPH to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the S/UNI-MPH for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-MPH . While the HIZIO bit is a logic 1, all output pins of the S/UNI-MPH except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

12.1 Test Mode 0

In Test Mode 0, the S/UNI-MPH allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface (except for RDAT[7:0], RSOC, RXPRTY, and RCA).

To enable Test Mode 0, 00H should be written to every address in the Test Register Memory Map (400H to 7FFH) and then the IOTST bit in the Master Test Register (Register 00CH) should be set to logic 1. Some particular I/O require certain configuration bits to be set properly for Test Mode 0 operation to work. These configuration requirements are detailed in the notes accompanying the following address maps.

Reading the following address locations returns the values for the indicated inputs to the D[7:0] bits:

Table 2 - Reading S/UNI-MPH Inputs in Test Mode 0

Address	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
410H					RDP[1]	RDN[1]	RCLKI[1]	
418H					XCLK[1]			
434H							TDLSIG[1]	
440H	TCLKI[2]		TFPI					
473H							RRDENB[1][3]	RFCLK
488H			TXPRTY		TSOC	MPHEN	TFCLK	
489H	TDAT[7]	TDAT[6]	TDAT[5]	TDAT[4]	TDAT[3]	TDAT[2]	TDAT[1]	TDAT[0]
48AH								TWRENB[1]
510H					RDP[2]	RDN[2]	RCLKI[2]	
518H					XCLK[1]			
534H							TDLSIG[2]	
540H	TCLKI[2]		TFPI					
573H							RRDENB[2][3]	RFCLK
588H			TXPRTY		TSOC	MPHEN	TFCLK	
589H	TDAT[7]	TDAT[6]	TDAT[5]	TDAT[4]	TDAT[3]	TDAT[2]	TDAT[1]	TDAT[0]
58AH								TWRENB[2]
610H					RDP[3]	RDN[3]	RCLKI[3]	
618H					XCLK[1]			
634H							TDLSIG[3]	
640H	TCLKI[2]		TFPI					
673H							RRDENB[3][3]	RFCLK
688H			TXPRTY		TSOC	MPHEN	TFCLK	
689H	TDAT[7]	TDAT[6]	TDAT[5]	TDAT[4]	TDAT[3]	TDAT[2]	TDAT[1]	TDAT[0]
68AH								TWRENB[3]
710H					RDP[4]	RDN[4]	RCLKI[4]	
718H					XCLK[1]			

Address	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
734H							TDLSIG[4]	
740H	TCLKI[2]		TFPI					
773H							RRDENB[4][3]	RFCLK
788H			TXPRTY		TSOC	MPHEN	TFCLK	
789H	TDAT[7]	TDAT[6]	TDAT[5]	TDAT[4]	TDAT[3]	TDAT[2]	TDAT[1]	TDAT[0]
78AH								TWRENB[4]

Notes:

1. The MODE[1] in the Transmit Configuration Register and the FIFOBYP register bit must not be set.

2. So long as the PAYLB register bit is not set.

3. Only one of RRDENB[4:1] can be set low at any time for the proper value to be read.

Writing the following address locations forces the outputs to the state of the corresponding D[7:0] bits.

Table 3 - Controlling Outputs in Test Mode 0

Address	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
410H		INT[1]						RCLKO[2]
418H	INT[1]					TCLKO[1][3]	TDN[1]	TDP[1]
434H						TDLCLK[1][4]	TDLSIG[1]	
438H							RDLCLK[1]	RDLSIG[1]
440H	TDLCLK[1][5]							
444H								TDLCLK[1][6]
488H					TCA[1], TCAMPH[7]			
510H		INT[1]						
518H	INT[1]					TCLKO[2][3]	TDN[2]	TDP[2]
534H						TDLCLK[2][4]	TDLSIG[2]	
538H							RDLCLK[2]	RDLSIG[2]
540H	TDLCLK[2][5]							
544H								TDLCLK[2][6]

Address	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
588H					TCA[2]			
610H		INT[1]						
618H	INT[1]					TCLKO[3][3]	TDN[3]	TDP[3]
634H						TDLCLK[3][4]	TDLSIG[3]	
638H							RDLCLK[3]	RDLSIG[3]
640H	TDLCLK[3][5]							
644H								TDLCLK[3][6]
688H					TCA[3]			
710H		INT[1]						
718H	INT[1]					TCLKO[4][3]	TDN[4]	TDP[4]
734H						TDLCLK[4][4]	TDLSIG[4]	
738H							RDLCLK[4]	RDLSIG[4]
740H	TDLCLK[4][5]							
744H								TDLCLK[4][6]
788H					TCA[4]			

Notes:

1. Setting any of the INT bits high will force INTB low.
2. So long as MODE[1] in the Recieve Configuration Register is not set.
3. So long as OCLKSEL=0, FIFOBYP=0, and MODE[1]=0 in the Transmit Configuration. (this is the default)
4. So long as TXDMASIG is set.
5. If TXDMASIG is cleared and MODE[1:0] = 00 in the Transmit Configuration Register (this is the default)
6. If TXDMASIG is cleared, MODE[1:0] = 01 in the Transmit Configuration Register, and SIGEN = 0 and DLEN =1 in the E1-TRAN Configuration Register.
7. If MPHEN = 1, the value written to this bit will appear on TCAMPH.

12.2 JTAG Test Port

The Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port and on the boundary scan cells, refer to the Operations section.

Identification Register

Length - 32 bits

Version number - 0H

Part Number - 7344H

Manufacturer's identification code - 0CDH

Device identification - 073440CDH

Table 4 - Boundary Scan Register

Length - 127 bits

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
TFPI[7]	126	IN_CELL	0	tdn[2]	73	OUT_CELL	-
TCLKI	125	IN_CELL	0	tdlclk[1]	72	OUT_CELL	-
XCLK	124	IN_CELL	0	TDLCLK[2]	71	OUT_CELL	-
MPHEN	123	IN_CELL	0	tdlclk[3]	70	OUT_CELL	-
RSTB	122	IN_CELL	0	TDLCLK[4]	69	OUT_CELL	-
WRB	121	IN_CELL	1	INTB	68	OUT_CELL	-
RDB	120	IN_CELL	1	TSOC	67	IN_CELL	-
CSB	119	IN_CELL	1	TXPRTY	66	IN_CELL	-
ALE	118	IN_CELL	0	TFCLK	65	IN_CELL	-
A[0:5]	117:112	IN_CELL	011010	TDLSIG[1]	64	IO_CELL	-
A[6:10]	111:107	IN_CELL	00100	TDLSIG1_OEN[1]	63	OUT_CELL	-
RDP[1]	106	IN_CELL	0	TDLSIG[2]	62	IO_CELL	-
RDN[1]	105	IN_CELL	0	TDLSIG2_OEN[1]	61	OUT_CELL	-

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
RCLKI[1]	104	IN_CELL	0	TDLSIG[3]	60	IO_CELL	-
RDP[2]	103	IN_CELL	0	TDLSIG3_OEN[1]	59	OUT_CELL	-
RDN[2]	102	IN_CELL	1	TDLSIG[4]	58	IO_CELL	-
RCLKI[2]	101	IN_CELL	1	TDLSIG4_OEN[1]	57	OUT_CELL	-
RDP[3]	100	IN_CELL	0	TDP[3]	56	OUT_CELL	-
RDN[3]	99	IN_CELL	0	TDN[3]	55	OUT_CELL	-
RCLKI[3]	98	IN_CELL	1	TCLKO[3]	54	OUT_CELL	-
RDP[4]	97	IN_CELL	1	TDP[4]	53	OUT_CELL	-
RDN[4]	96	IN_CELL	0	TDN[4]	52	OUT_CELL	-
RCLKI[4]	95	IN_CELL	1	TCLKO[4]	51	OUT_CELL	-
D[0]	94	IO_CELL	-	RCLKO	50	OUT_CELL	-
D0_OEN[1]	93	OUT_CELL	-	TCA[1:4]]	49:46	OUT_CELL	-
D[1]	92	IO_CELL	-	RCA[1:4]	45:42	OUT_CELL	-
D1_OEN[1]	91	OUT_CELL	-	TWRENB[4]	41	IO_CELL	-
D[2]	90	IO_CELL	-	TCAMPH_OEN[1]	40	OUT_CELL	-
D2_OEN[1]	89	OUT_CELL	-	TWRENB[3:1]	39:37	IN_CELL	-
D[3]	88	IO_CELL	-	TDAT[0:7]	36:29	IN_CELL	-
D3_OEN[1]	87	OUT_CELL	-	RFCLK	28	IN_CELL	-
D[4]	86	IO_CELL	-	RDLCLK[1:4]	27:24	OUT_CELL	-
D4_oen[1]	85	OUT_CELL	-	RRDENB[1:3]	23:21	IN_CELL	-
d[5]	84	IO_CELL	-	RRDENB[4]	20	IO_CELL	-
d5_oen[1]	83	OUT_CELL	-	RCAMPH_OEN[1]	19	OUT_CELL	-
d[6]	82	IO_CELL	-	RSOC	18	OUT_CELL	-
d6_oen[1]	81	OUT_CELL	-	RXPRTY	17	OUT_CELL	-
d[7]	80	IO_CELL	-	RDAT[0:7]	16:9	OUT_CELL	-
d7_oen[1]	79	OUT_CELL	-	RDLSIG[1:4]	8:5	OUT_CELL	-
tclko[1]	78	OUT_CELL	-	HIZ[4][2]	4	OUT_CELL	-
tdp[1]	77	OUT_CELL	-	HIZ[3][3]	3	OUT_CELL	-
tdn[1]	76	OUT_CELL	-	HIZ[2][4]	2	OUT_CELL	-
tclko[2]	75	OUT_CELL	-	HIZ[1][5]	1	OUT_CELL	-
tdp[2]	74	OUT_CELL	-	RFIFO_HIZ[6]	0	OUT_CELL	-

Notes:

1. All OEN signals will set the corresponding bidirectional signal (the one preceding the OEN in the boundary scan chain, see note 7 also) to an output when set low.

2. Unused.

3. When set high, RDLCLK[4:1], RCA[4:1], TCA[4:1], and RCLKO will be set to high-impedance.

4. When set high, TDP[4:1], TDN[4:1], TCLKO[4:1], TDLCLK[4:1] will be set to high impedance.

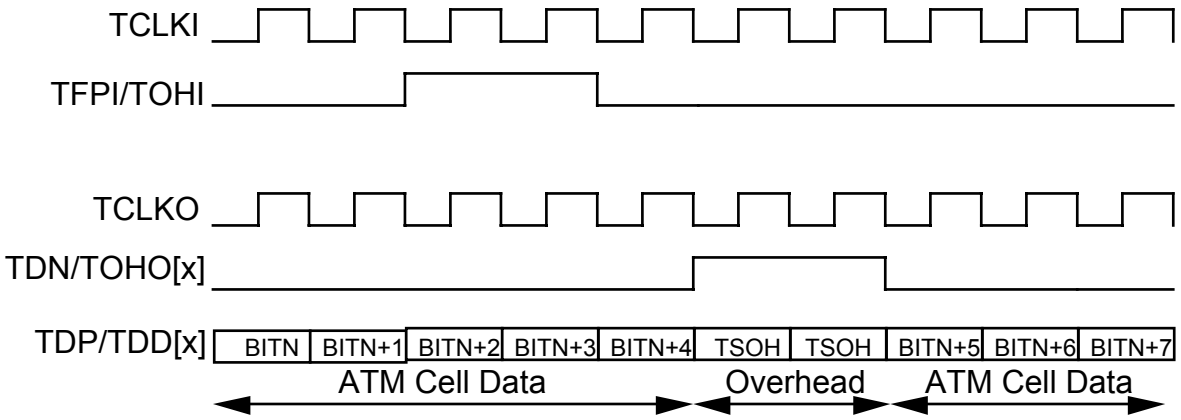
5. When set high, RDLSIG[4:1] will be set to high impedance.

6. When set high, RDAT[7:0], RSOC, and RXPRTY will be set to high impedance.

7. TFPI is the first bit of the boundary scan chain.

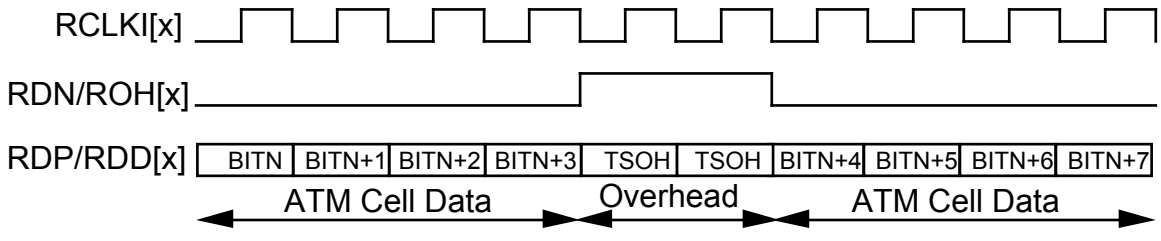
13 FUNCTIONAL TIMING

Figure 18 - Arbitrary Rate Transmit Interface



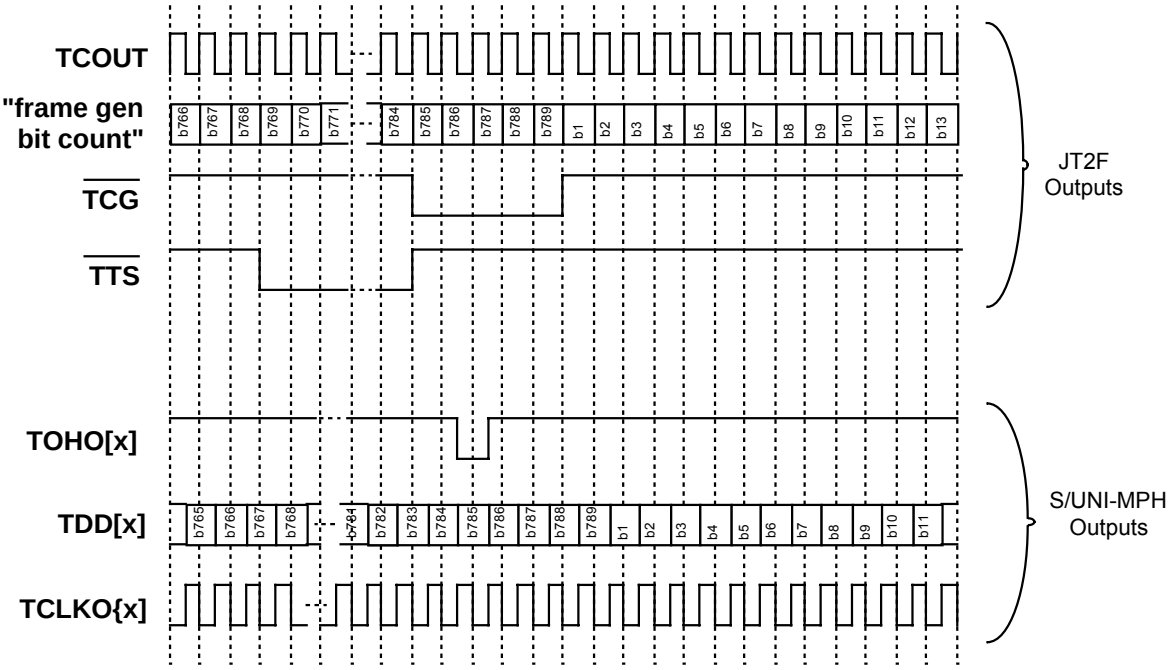
The S/UNI-MPH is configured to select the arbitrary transmit interface. TOHO marks the location of the transmission system overhead placeholder bits (TSOH) in the TDD stream. The delay between TOHI and TOHO is fixed to be 2.5 clock periods starting at the rising TCLKI edge where TOHI is sampled and finishing at the falling TCLKO[x] edge where TOHO[x] is generated. It should be noted that the outputs are clocked out on TCLKO[x] which is a flow-through version of TCLKI and which could be significantly delayed from TCLKI. The active polarity (here shown as active high) of the TOHI and TOHO signals can be inverted using the TOHINV and TDNINV bits in the Transmit Interface Configuration register. The active edge that is used to sample TFPI (here shown as the rising edge) as well as update TOHO[x] and TDD[x] can be inverted using the TFALL and TRISE bits in the Transmit Interface Configuration register. The octet alignment of the bit position labeled "BITM+1" in the timing diagram is controlled by the TOCTA bit in the Transmit Interface Configuration register.

Figure 19 - Arbitrary Rate Receive Interface



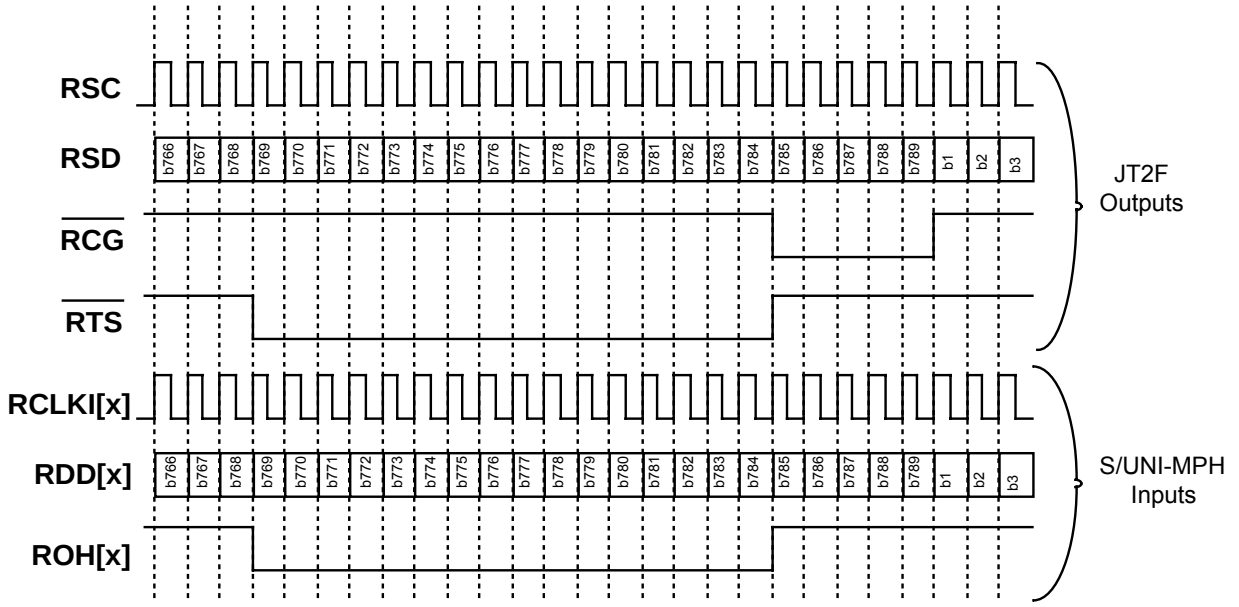
The S/UNI-MPH is configured to select the arbitrary receive interface. ROHI marks the location of the transmission system overhead bits (TSOH) in the RDD stream. The active polarity (here shown as active high) of the ROHI signal can be inverted using the RDNINV bit in the Receive Interface Configuration register. The active edge that is used to sample RDD and ROHI (here shown as the rising edge) can be inverted using the RFALL bit in the Receive Interface Configuration register.

Figure 20 - J2 (6.312 Mbit/s) Transmit Interface



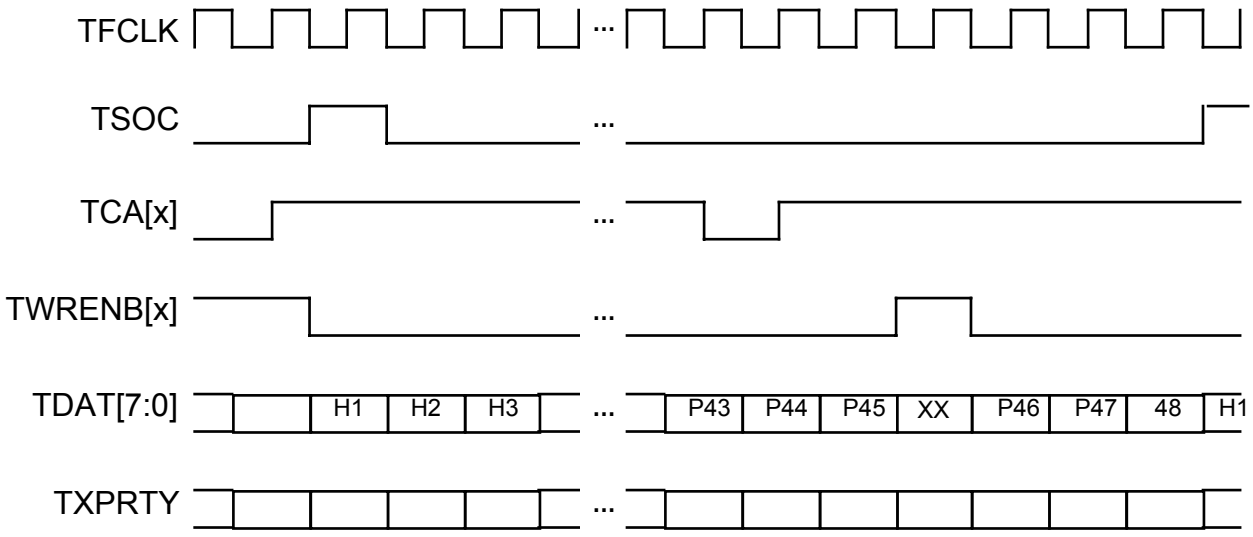
The S/UNI-MPH is configured to select the J2 transmit interface. The connections between the S/UNI-MPH and the JT2F J2 framer should be made as shown in the "OPERATIONS - Using the JT2F" section. The register bits TFALL, TOHINV, TRISE, and TDNINV are all set to logic 1 so that TOHI is sampled on the falling TCLKI edge, TOHI is active low, TDD[x] and TOHO[x] are updated on the rising edge of TCLKO[x], and TOHO[x] is active low. TOHO[x] goes low during the first frame alignment bit position in the transmitted data once every J2 multiframe. The falling edge of TOHO[x] occurs approximately 1 clock period after TTS gets sampled high (starting at the falling edge of TCOUT where TTS is sampled high by the S/UNI-MPH and ending at the rising edge of TCLKO[x] where TOHO[x] is generated). Note that with this configuration, TCLKO[x] is a flow-through and inverted version of TCOUT whose phase delay from TCOUT will be less than half a TCOUT period.

Figure 21 - J2 (6.312 Mbit/s) Receive Interface



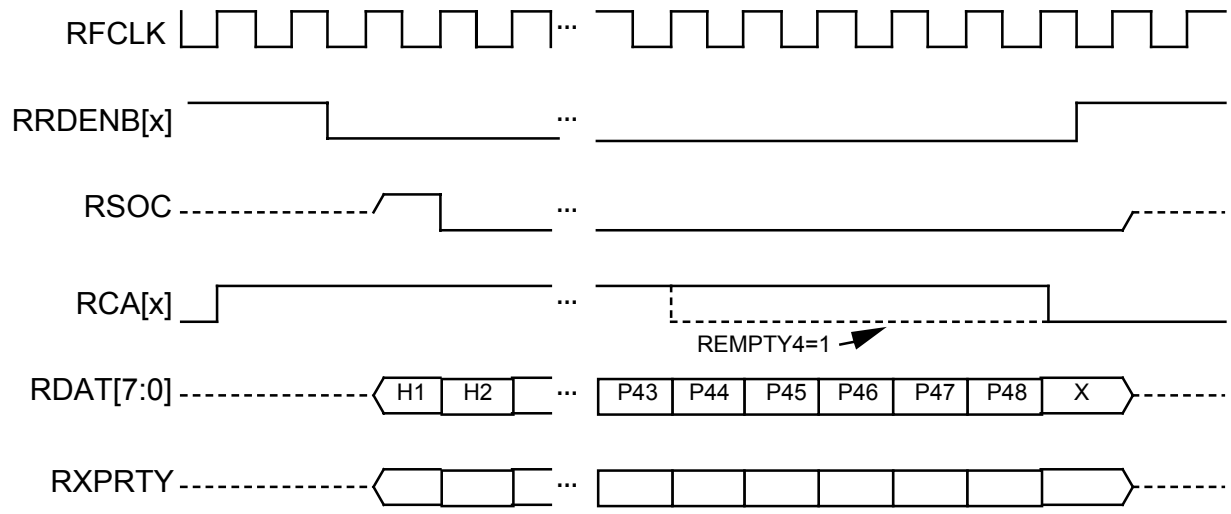
The S/UNI-MPH is configured to select the J2 receive interface. The connections between the two devices should be made as shown in the "OPERATIONS - Using the JT2F" section. The register bits RDNINV and RFALL are set to logic 1 so that ROH[x] is active low and so RDD[x] and ROH[x] are sampled on the falling edge of RCLKI[x].

Figure 22 - Direct-PHY Selection Transmit Cell Interface (MPHEN = 0)



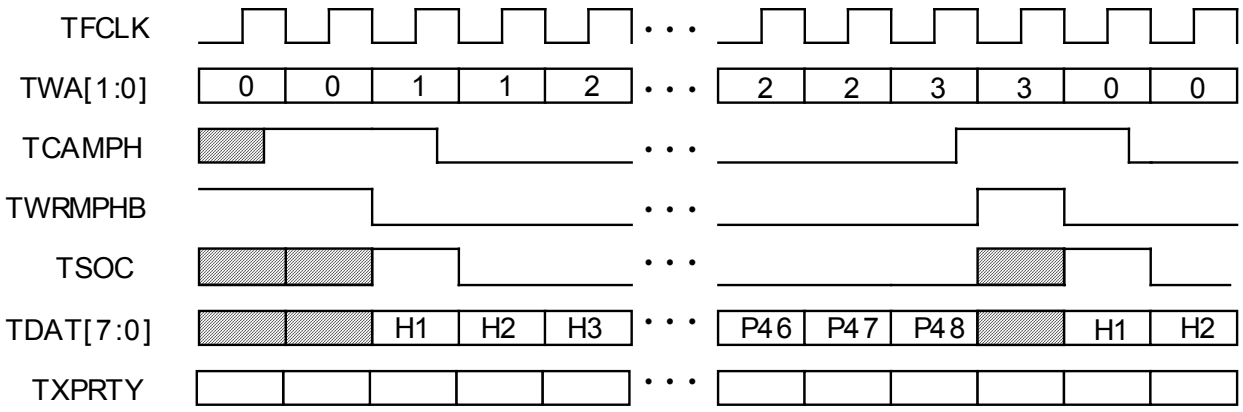
The S/UNI-MPH is configured for direct PHY selection (MPHEN = 0). The TCA[x] cell available indicators signal when a cell is available in the corresponding PHY's transmit FIFO (shown with TFULL4 in the TXCP Interrupt Enable / Status and Control Register set to logic 1). The TWRENB[x] input is brought low to begin the cell transfer. Only one TWRENB[x] should be active during a cell transfer.

Figure 23 - Direct-PHY Selection Receive Cell Interface (MPHEN = 0)



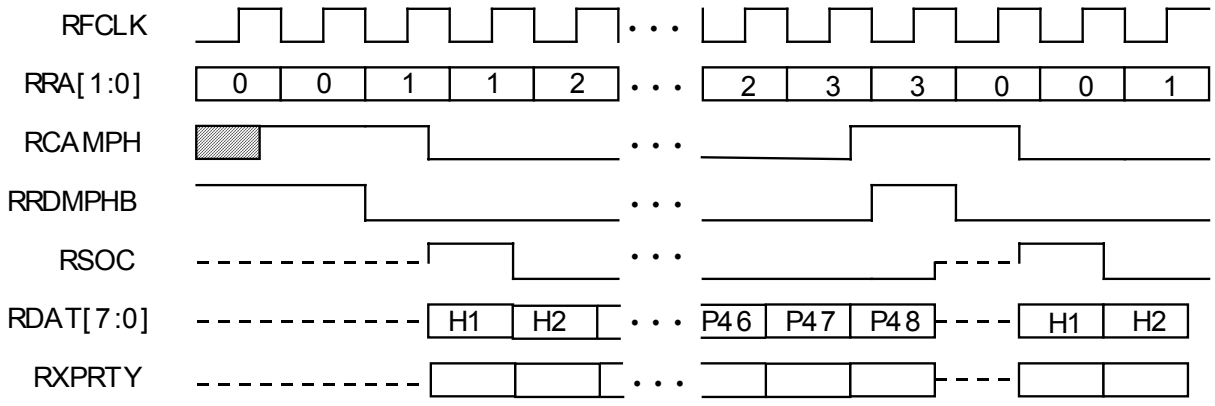
The S/UNI-MPH is configured for direct PHY selection (MPHEN = 0). The RCA[x] cell available indicators signal when a cell is available in the corresponding PHY's receive FIFO. The RRDENB[x] input is brought low to begin the cell transfer. Only one RRDENB[x] should be active during a cell transfer.

Figure 24 - Multi-PHY Addressing Transmit Cell Interface (MPHEN = 1)



The S/UNI-MPH is configured for multi-PHY addressing (MPHEN = 1). The TCAMPH output is updated with the transmit cell available status of the PHY selected by the TWA[1:0] inputs in the previous cycle. TWA[1:0] is latched while TWRMPHB is high. On the high to low transition of TWRMPHB, the PHY selected by the latched address (in this case PHY #1, TWA[1:0] = 0H) begins to accept its 53 octet cell. During this transfer, the three remaining cell available signals (from PHY #2, #3, and #4) can be polled as required. The cell available status of PHY #1 indicates that a cell is available while the cell transfer is in progress. In the diagram above, at the end of the cell transfer from PHY #1, PHY #4 (TWA[1:0] = 3H) has a cell available. TWRMPHB is brought high for one clock cycle to latch the new address. TWRMPHB is then brought low and the cell transfer to PHY #4 proceeds.

Figure 25 - Multi-PHY Addressing Receive Cell Interface (MPHEN = 1)



The S/UNI-MPH is configured for multi-PHY addressing (MPHEN = 1). The RCAMPH output is updated with the receive cell available status of the PHY selected by the RRA[1:0] inputs in the previous cycle. RRA[1:0] is latched while RRDMPHB is high. On the high to low transition of RRDMPHB, the PHY selected by the latched address (in this case PHY #1, RRA[1:0] = 0H) begins outputting its 53 octet cell. During this transfer, the three remaining cell available signals (from PHY #2, #3, and #4) can be polled as required. The cell available status of PHY #1 indicates that a cell is available while the cell transfer is in progress. In the diagram above, at the end of the cell transfer from PHY #1, PHY #4 (RRA[1:0] = 3H) has a cell available. RRDMPHB is brought high for one clock cycle to latch the new address and to avoid contention on the tristateable signals. RRDMPHB is then brought low and the cell transfer from PHY #4 proceeds.

14 OPERATION

Using the Internal FDL Transmitter

Upon reset of the S/UNI-MPH, the XFDL should be disabled by setting the EN bit in the XFDL Configuration Register to logic 0. If data is not ready to be transmitted, the TDLINT[x] output should also be masked by setting the INTE bit to logic 0.

When initializing the XFDL, the XFDL Configuration Register should be set for transmission: if the FCS is desired, the CRC bit should be set to logic 1; if the block is to be used in interrupt driven mode, interrupts should be enabled by setting the INTE bit to logic 1. Finally, the XFDL can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The XFDL can be used in a polled, interrupt driven, or DMA-controlled mode for the transfer of frame data. In the polled mode, the TDLINT[x] and TDLUDR[x] outputs of the XFDL are not used, and the processor controlling the XFDL must periodically read the XFDL Interrupt Status Register to determine when to write to the XFDL Transmit Data Register. In the interrupt driven mode, the processor controlling the XFDL uses either the TDLINT[x] output, or the main processor INTB output and the interrupt source registers, to determine when to write to the XFDL Transmit Data Register. In the DMA controlled mode, the TDLINT[x] output of the XFDL is used as a DMA request input to the DMA controller, and the TDLUDR[x] output is used as an interrupt to the processor to allow handling of exceptions. The TDLUDR[x] output can also be enabled to generate a processor interrupt through the common INTB output via the TDLUDRE bit in the Datalink Options register.

Polled Mode

If the XFDL data transfer is operating in the polled mode (TXDMASIG, TDLINTE, and TDLUDRE bits in the Datalink Options Register are set to logic 0), then a timer periodically starts up a service routine, which should process data as follows:

1. Read the XFDL Interrupt Status Register and poll the UDR and INT bits.

2. If UDR=1, then clear the UDR bit in the XFDL Interrupt Status Register to logic 0, and restart the current frame. Go to step 1.

3. If INT=1, then:

a) If there is still data to send, then write the next data byte to the XFDL Transmit Data Register;

b) If all bytes in the frame have been sent, then set the EOM bit in the XFDL Configuration Register to logic 1.

4. If EOM bit was set to logic 1 in step 3b, then:

   a) Read the XFDL Interrupt Status Register and check the UDR bit.

   b) If UDR=1 then reset the UDR bit in the XFDL Interrupt Status Register and the EOM bit in the XFDL Configuration Register to logic 0, and retransmit the last frame.

5. Go to step 1.

Interrupt Mode

In the case of interrupt driven data transfer, the TDLINT[x] output is connected to the interrupt input of the processor, and the interrupt service routine should process the data exactly as described above for the polled mode. The INTE bit in the XFDL Configuration Register must be set to logic 1. Alternately, the INTB output can be connected to the interrupt input of the processor if the TDLINTE bit of the Datalink Options Register is set to logic 1. If this mode is used, additional polling of the Source Selection/Interrupt ID, Interrupt Source #1 and Interrupt Source #2 registers must be performed to identify the cause of the interrupt before initiating the interrupt service routine.

DMA-Controlled Mode

The XFDL can also be used with a DMA controller to process the frame data. In this case, the TDLUDR[x] output is connected to the processor interrupt input. The TDLINT[x] output of the XFDL is connected to the DMA request input of the DMA controller. The INTE bit in the XFDL Configuration Register must be set to logic 1 before enabling the XFDL. The DMA controller writes a data byte to the XFDL whenever the TDLINT[x] output is high. If there is a problem during transmission and an underrun condition occurs, then the TDLUDR[x] output goes high and the processor is interrupted. The processor can then halt the DMA controller, reset the UDR bit in the XFDL Interrupt Status Register, reset the frame data pointers, and restart the DMA controller to resend the data frame. After the message transmission is completed, the DMA controller must initiate a write to set the EOM bit in the XFDL Configuration Register and then verify that TDLUDR[x] is not set prior to setting EOM.

Using the Internal FDL Receiver

On power up of the S/UNI-MPH, the RFDL should be disabled by setting the EN bit in the RFDL Configuration Register to logic 0. The RFDL Interrupt Control/Status Register should then be initialized to select the FIFO buffer fill level at which an interrupt will be generated.

After the Interrupt Control/Status Register has been written to, the RFDL can be enabled at any time by setting the EN bit in the RFDL Configuration Register to logic 1. When the RFDL is enabled, it will assume that the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated (if enabled), and the byte received before the first flag was detected will be written into the FIFO buffer. Because the FLG and EOM bits are passed through the buffer, this dummy write allows the RFDL Status Register to accurately reflect the current state of the data link. A RFDL Status Register read after a RFDL Data Register read of the dummy byte will return EOM as logic 1 and FLG as logic 1. The first interrupt and data byte read after the RFDL is enabled (or TR bit set to logic 1) is an indication of the link status, and the data byte should therefore be discarded. It is up to the controlling processor to keep track of the link state as idle (all ones or bit-oriented messages active) or active (flags received).

The RFDL can be used in a polled, interrupt driven, or DMA controlled mode for the transfer of frame data.

Polled Mode

In the polled mode, the RDLINT[x] and RDLEOM[x] outputs of the RFDL are not used, and the processor controlling the RFDL must periodically read the RFDL Interrupt/Status to determine when to read the RFDL Receive Data Register. If the RFDL data transfer is operating in the polled mode, entry to the service routine is from a timer. The processor service routine should process the data in the following order:

1. Poll the INT bit in the RFDL Interrupt/Status Register until it is set to logic 1. Once INT is set to logic 1, then proceed to step 2.

2. Read the RFDL Receive Data Register.

3. Read the RFDL Status Register to check for the following:

   a) If OVR=1, then discard the current frame and go to step 1.

   ELSE

b) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the current frame, and go to step 1.

c) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and go to step 1.

ELSE

d) Save the last data byte read.

e) If EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register to process the frame properly.

f) If FE=0, then go to step 2, else go to step 1.

The link state is typically a local software variable. The link state is inactive if the RFDL is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RFDL is receiving flags or data.

Interrupt Mode

In the interrupt driven mode, the processor controlling the RFDL uses either the RDLINT[x] output, or the main processor INTB output (RDLINTE bit of the Datalink Options Register is set to logic 1) and the Source Selection/Interrupt ID, Interrupt Source #1 and Interrupt Source #2 Registers, to determine when to read the RFDL Receive Data Register. The RXDMASIG bit in the Datalink Options Register should be set to logic 1. RDLINTE of the same register should be set to logic 1 if the INTB output is used as the interrupt source. The processor interrupt service routine should process the data in the following order:

1. Wait for an interrupt originating from the RFDL. Once the interrupt is set, then proceed to step 2.

2. Read the RFDL Receive Data Register.

3. Read the RFDL Status Register to check for the following:

   a) If OVR=1, then discard the current frame and go to step 1.

   ELSE

   b) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the current frame, and go to step 1.

c) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and go to step 1.

ELSE

d) Save the last data byte read.

e) If EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register to process the frame properly.

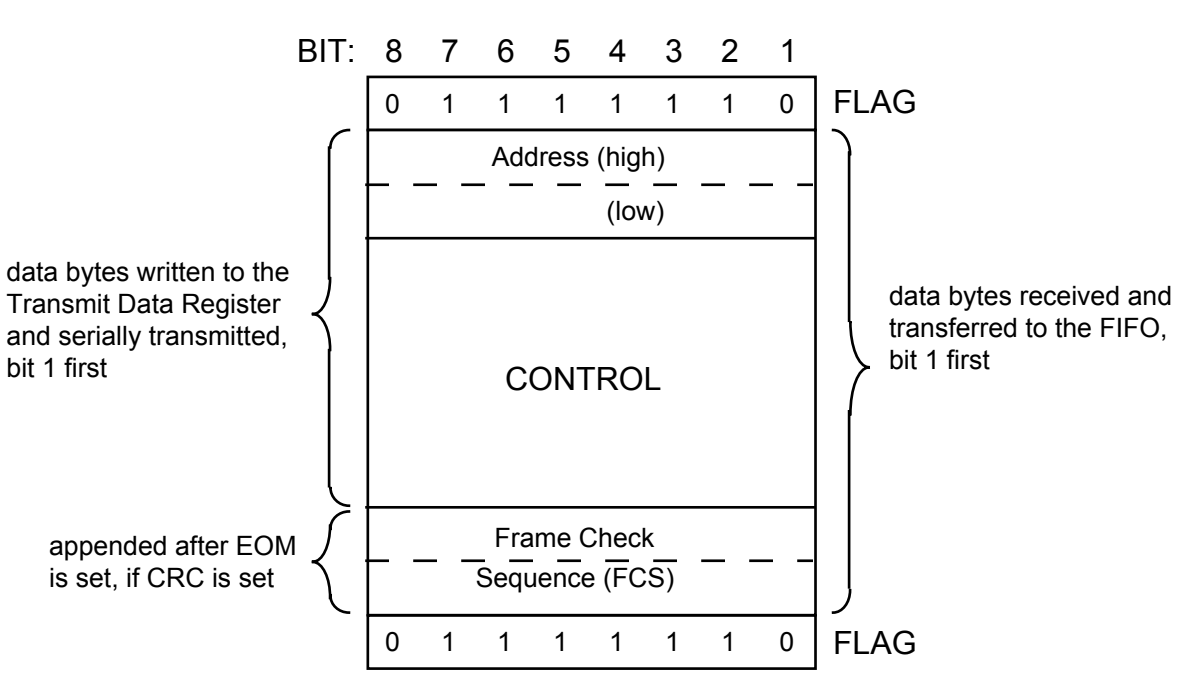
f) If FE=0, then go to step 2, else go to step 1.

DMA-Controlled Mode

The RFDL can also be used with a DMA controller to process the frame data. In the DMA controlled mode, the RDLINT[x] output of the RFDL is used as a DMA request input to the DMA controller, and the RDLEOM[x] output is used as an interrupt to the processor to allow handling of exceptions and as an indication of when to process a frame. The RXDMASIG bit of the Datalink Options Register should be set to logic 1.

The RDLINT[x] output of the RFDL is connected through a gate to the DMA request input of the DMA controller to optionally inhibit the DMA request if the RDLEOM[x] output is high. The DMA controller reads the data bytes from the RFDL whenever the RDLINT[x] output is high. When the current byte read from the RFDL Receive Data Register is the last byte in a frame (due to an end-of-message or an abort), or an overrun condition occurs, then the RDLEOM[x] output goes high. The DMA controller is inhibited from reading any more bytes, and the processor is interrupted. The processor can then halt the DMA controller, read the RFDL Status Register, process the frame, and finally reset the DMA controller to process the data for the next frame. The RDLEOM[x] output can optionally be enabled to generate a processor interrupt through the common INTB output via the RDLEOME bit in the Datalink Options register, rather than tying the RDLEOM[x] output directly to the microprocessor. This allows a central microprocessor controlling the S/UNI-MPH operation to also respond to conditions affecting the DMA servicing of RFDL. When using the INTB output, the central processor must poll the Source Selection/Interrupt ID, Interrupt Source #1 and Interrupt Source #2 Registers to identify the source of the interrupt before beginning any interrupt service routine.

Figure 26 - Typical Data Frame



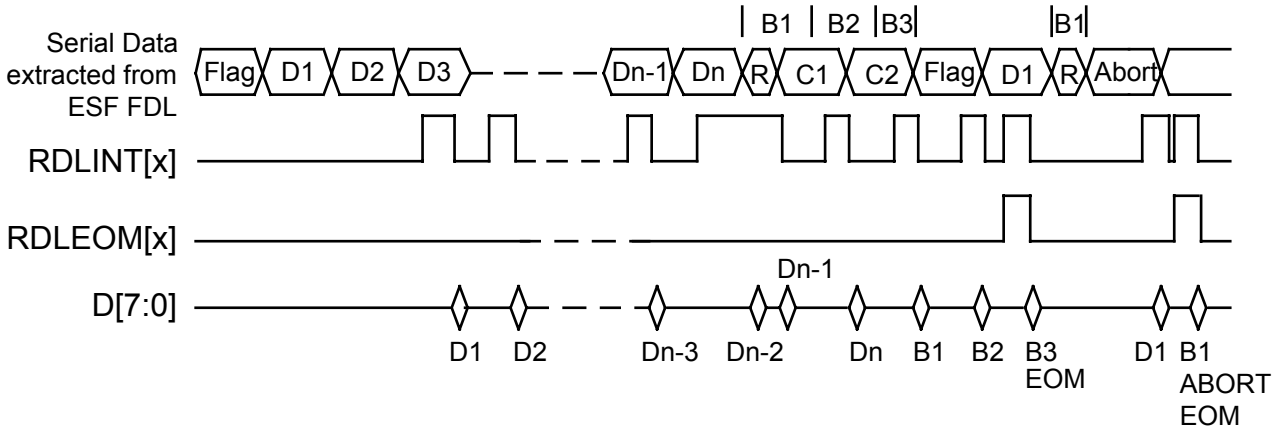
Bit 1 is the first serial bit to be transmitted or received.

Both the address and control bytes must be supplied by an external processor and are shown for reference purposes only.

Key used on subsequent diagrams:

Flag	- flag sequence (01111110)
Abort	- abort sequence (01111111)
D1 - Dn	- n frame data bytes
R	- remainder bits (less than 8)
C1, C2	- CRC-CCITT information
B1, B2, B3	- groupings of 8 bits

Figure 27 - RFDL Normal Data and Abort Sequence



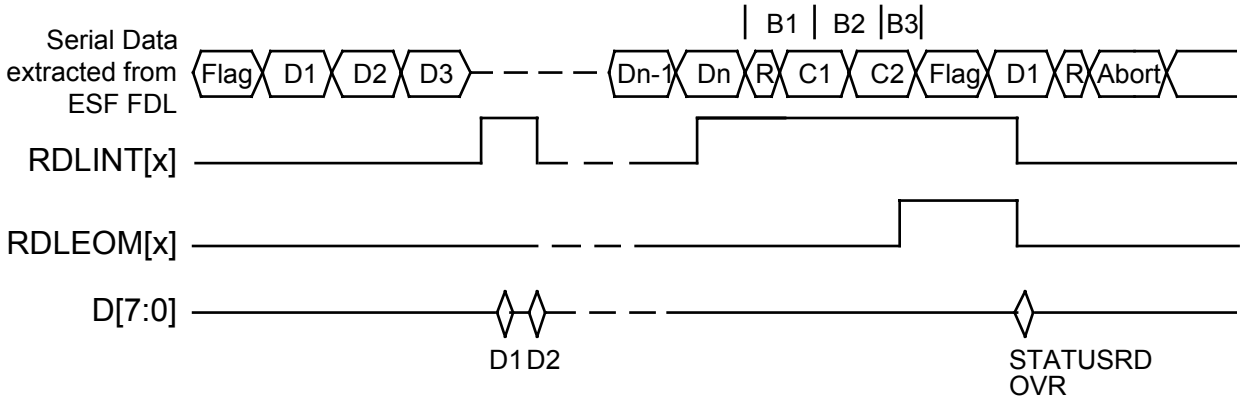
This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when one byte is present in the FIFO buffer. The RFDL is assumed to be operating in the interrupt driven mode. Each read shown is composed of two register reads: first a read of the Data Register, followed by a read of the Status Register. A read of the Data Register sets the RDLINT[x] output to low if no more data exists in the FIFO buffer. The status of the FE bit returned in the Status Register read will indicate the FIFO buffer fill status as well. The Data Register read Dn-2 is shown to occur after two bytes have been written into the buffer. The RDLINT[x] output does not go low after the first Data Register read because a data byte still remains to be read. The RDLINT[x] output goes low after Data Register read Dn-1. The FE bit will be logic 0 in Status Register read Dn-2 and logic 1 in Status Register read Dn-1.

The RDLEOM[x] output goes high as soon as the last byte in the frame is read from the Data Register. The RDLINT[x] output will go low if the FIFO buffer is empty. The next Status Register read will return a value of logic 1 for the EOMR and FLG bits, and cause the RDLEOM[x] output of the RFDL to return low.

In the next frame, the first data byte is received, and after a delay of ten bit periods, it is written to the FIFO buffer, and read by the processor after the interrupt. When the abort sequence is detected, the data received up to the abort is written to the FIFO buffer and an interrupt generated. The processor then reads the partial byte from the Data Register and the RDLEOM[x] output is set high. The processor then reads the Status Register which will return a value of logic 1 for the EOMR and FLG bits, and set the RDLEOM[x] output low. The FIFO buffer is not cleared when an abort is detected. All bytes received up to the abort are available to be read.

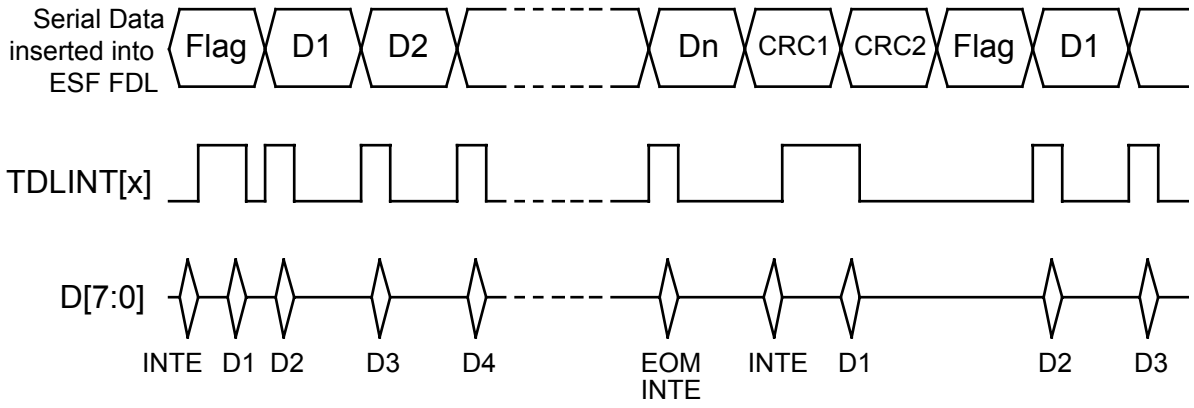
After an abort, the RFDL state machine will be in the receiving all ones state, and the data link status will be idle. When the first flag is detected, a new interrupt will be generated, with a dummy data byte loaded into the FIFO buffer, to indicate that the data link is now active.

Figure 28 - RFDL FIFO Overrun



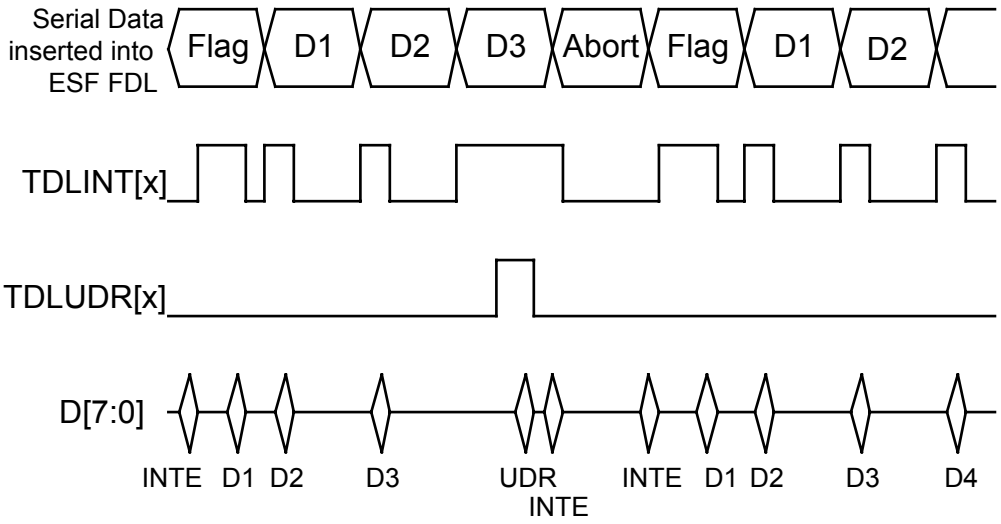
This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when two data bytes are present in the FIFO buffer. Each read is composed of two register reads, as described above. In this example, data is not read by the end of B2. An overrun occurs since unread data (Dn-3) has been overwritten by B1. This sets the RDLEOM[x] output high, and resets both the RFDL and the FIFO buffer. The RFDL is held disabled until the Status Register is read. The start flag sequence is not detected since the RFDL is still held disabled when it occurs. Consequently, the RFDL will ignore the entire frame including the abort sequence (since it has not occurred in a valid frame or during flag reception, according to the RFDL).

Figure 29 - XFDL Normal Data Sequence



This diagram shows the relationship between XFDL inputs and outputs for the case where interrupts and CRC are enabled for regular data transmission. The process is started by setting the INTE bit in the Configuration/Control Register to logic 1, thus enabling the TDLINT[x] signal. When TDLINT[x] goes high, the interrupt service routine is started, which writes the first byte (D1) of the data frame to the Transmit Data Register. When this byte begins to be shifted out on the data link, TDLINT[x] goes high. This restarts the interrupt service routine, and the next data byte (D2) is written to the Transmit Data Register. When D2 begins to be shifted out on the data link, TDLINT[x] goes high again. This cycle continues until the last data byte (Dn) of the frame is written to the Transmit Data Register. When Dn begins to be shifted out on the data link, TDLINT[x] again goes high. Since all the data has been sent, the interrupt service routine sets the EOM bit in the Configuration/Control Register to logic 1. The TDLINT[x] interrupt should also be disabled at this time by setting the INTE bit to logic 0. The XFDL will then shift out the two-byte CRC word and closing flag, which ends the frame. Whenever new data is ready, the TDLINT[x] signal can be re-enabled by setting the INTE bit in the Configuration/Control Register to logic 1, and the cycle starts again.

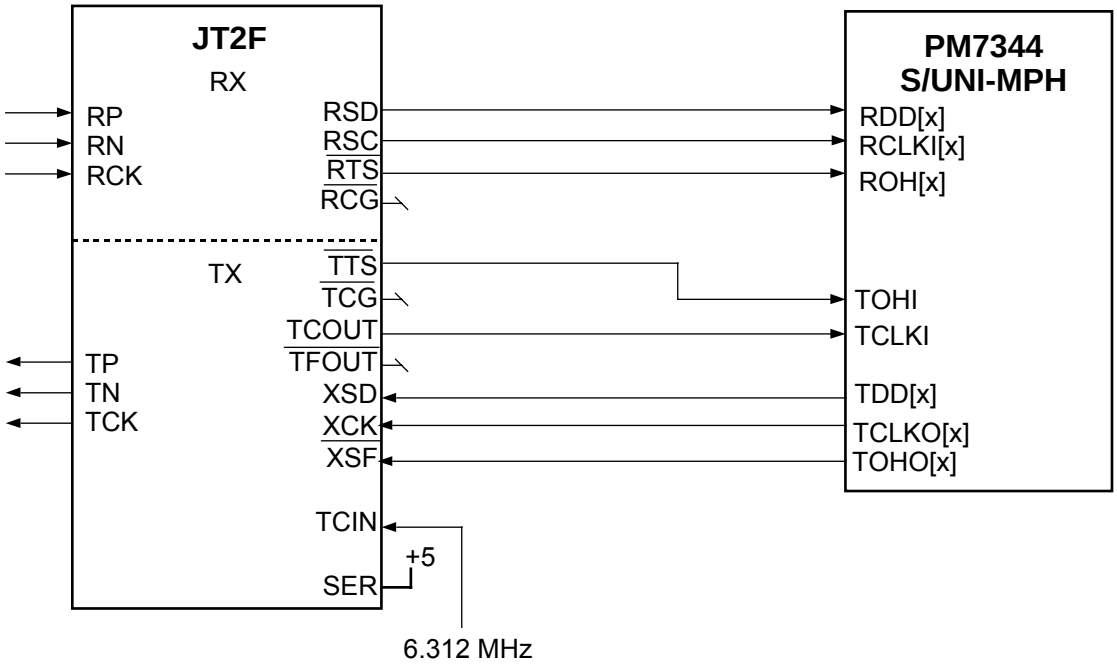
Figure 30 - XFDL Underrun Sequence



This diagram shows the relationship between XFDL inputs and outputs in the case of an underrun error. An underrun error occurs if the XFDL finishes transmitting the current message byte before the processor writes the next byte into the Transmit Data Register; that is, the processor fails to write data to the XFDL in time. In this example, data is not written to the XFDL within five rising clock edges after TDLINT[x] goes high at the beginning of the transmission of byte D3. The TDLUDR[x] interrupt becomes active at this point, and an abort, followed by a flag, is sent out on the data link. Meanwhile, the processor must clear the TDLUDR[x] interrupt by setting the UDR bit in the Status Register to logic 0. The TDLINT[x] interrupt should also be disabled at this time by setting the INTE bit in the Configuration/Control Register to logic 0. The data frame can then be restarted as usual, by setting the INTE bit logic to 1. Transmission of the frame then proceeds normally.

14.1 Using the JT2F

Figure 31 - J2 Framer Example



The JT2F J2 framer can be connected to the S/UNI-MPH as shown above. The S/UNI-MPH is configured to select the J2 interface by setting the register bits MODE[1] to logic 1 and MODE[0] to logic 0. The register bits TFALL, TOHINV, TRISE, and TDNINV are all set to logic 1 so that TOHI is sampled on the falling TCLKI edge, TOHI is active low, TDD[x] and TOHO[x] are updated on the rising edge of TCLKO[x], and TOHO[x] is active low. The register bits RDNINV and RFALL are set to logic 1 so that ROH[x] is active low and so RDD[x] and ROH[x] are sampled on the falling edge of RCLKI[x].

Using the ROH and TOHI inputs from the JT2F, the S/UNI-MPH internally generates additional J2 overhead signals which identify the J2 signalling and framing bit positions. The S/UNI-MPH also generates the J2 multiframe output on TOHO. Additional information on the J2 Transmit and Receive timing is provided in the S/UNI-MPH Functional Timing section.

14.2 Using the Digital Jitter Attenuator

The key to using DJAT lies in selecting the appropriate divisors for the phase comparison between the selected reference clock and the generated smooth TCLKO[x].

14.2.1 Default Application

Upon reset, the S/UNI-MPH default condition provides jitter attenuation with TCLKO[x] referenced to the transmit clock TCLKI. The DJAT SYNC bit is also logic 1 by default. DJAT is configured to divide its input clock rate, TCLKI, and its output clock rate, TCLKO[x], both by 48, which is the maximum length of the FIFO. These divided down clock rates are then used by the phase comparator to update the DJAT DPLL. The phase delay between TCLKI and TCLKO[x] is synchronized to the physical data delay through the FIFO. For example, if the phase delay between TCLKI and TCLKO[x] is 12UI, the FIFO will be forced to lag its output data 12 bits from its input data.

The default mode works well with TCLKI at 1.544MHz for T1 operation format or at 2.048MHz for E1 operation format.

14.2.2 Data Burst Application

In applications where TCLKI works at a higher than nominal instantaneous rate (but with gapping to provide the same nominal rate over time), a few factors must be considered to adequately filter the resultant TCLKO[x] into a smooth 1.544MHz or 2.048MHz clock. The magnitude of the phase shifts in the incoming bursty data are too large to be properly attenuated by the PLL alone. However, the magnitudes, and the frequency components of these phase shifts are known, and are most often multiples of 8 kHz.

In this situation, the input clock to DJAT is a gapped bursty clock. The phase shifts of the input clock with respect to the generated TCLKO[x] in this case are large, but when viewed over a longer period, such as a frame, there is little net phase shift. Therefore, by choosing the divisors appropriately, the large phase shifts can be filtered out, leaving a stable reference for the DPLL to lock onto. In this application, the N1 and N2 divisors should be changed to C0H (i.e. divisors of 193 for T1 applications) or FFH (i.e. divisors of 256 for E1 applications). Consequently, the frequency of the clock inputs to the phase discriminator in the PLL is 8 kHz. The DJAT SYNC option must be disabled since the divisor magnitude of 193 or 256 is not an integer multiple of the FIFO length 48.

The self-centering circuitry of the FIFO should be enabled by setting the CENT register bit. This sets up the FIFO read pointer to be at least 4 UI away from the end of the FIFO registers, and then disengages. Should variations in the frequency of input clock or the output clock cause the read pointer to drift to within one unit interval of FIFO overflow or underflow, the pointer will be incrementally pushed away by the LIMIT control without any loss of data.

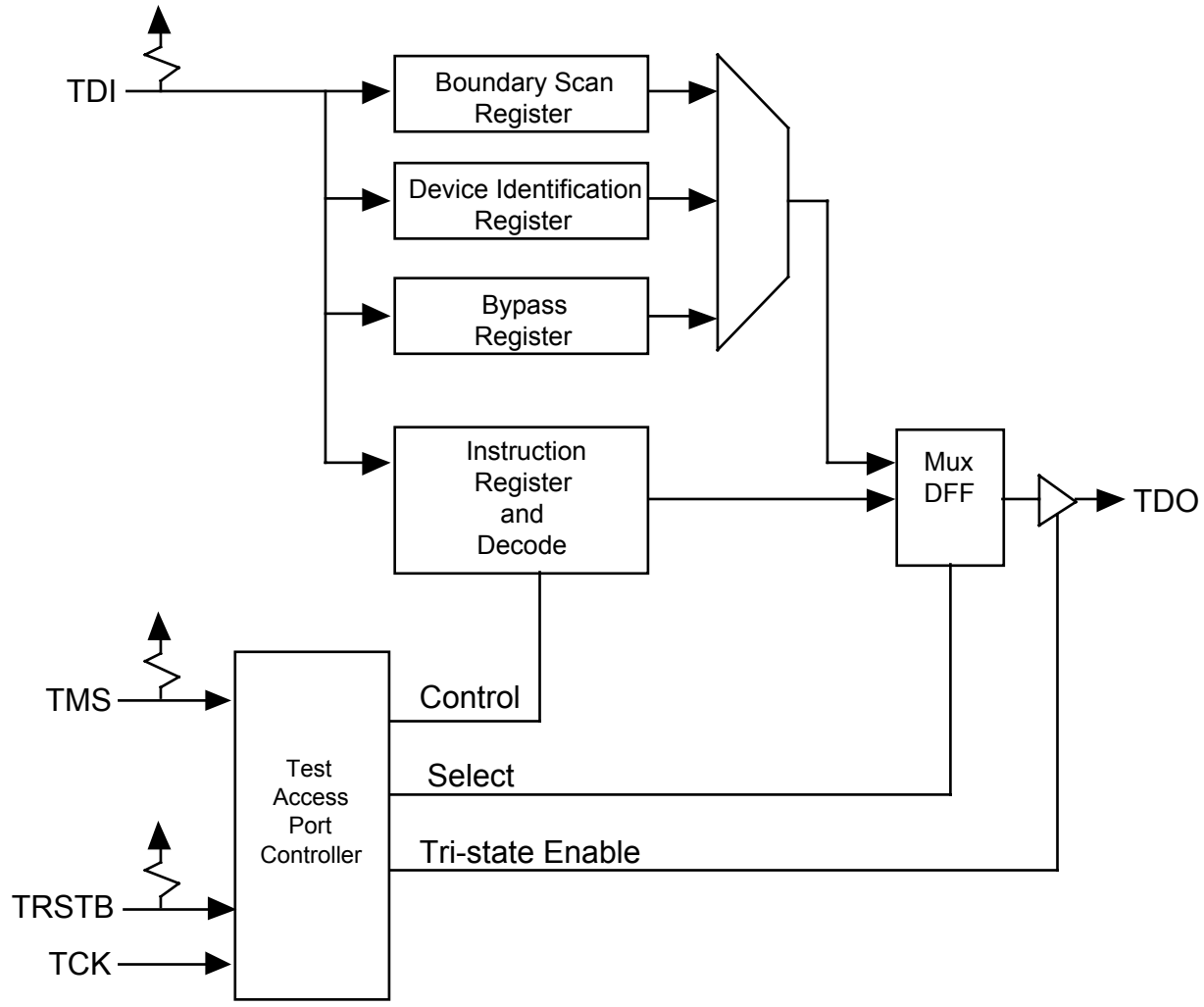
With SYNC disabled, and CENT and LIMIT enabled, the maximum tolerable phase difference between the bursty input clock and the smooth TCLKO[x] is

40UI. Phase wander between the two clock signals is compensated for by the LIMIT control.

14.3 JTAG Support

The S/UNI-MPH supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 32 - Boundary Scan Architecture



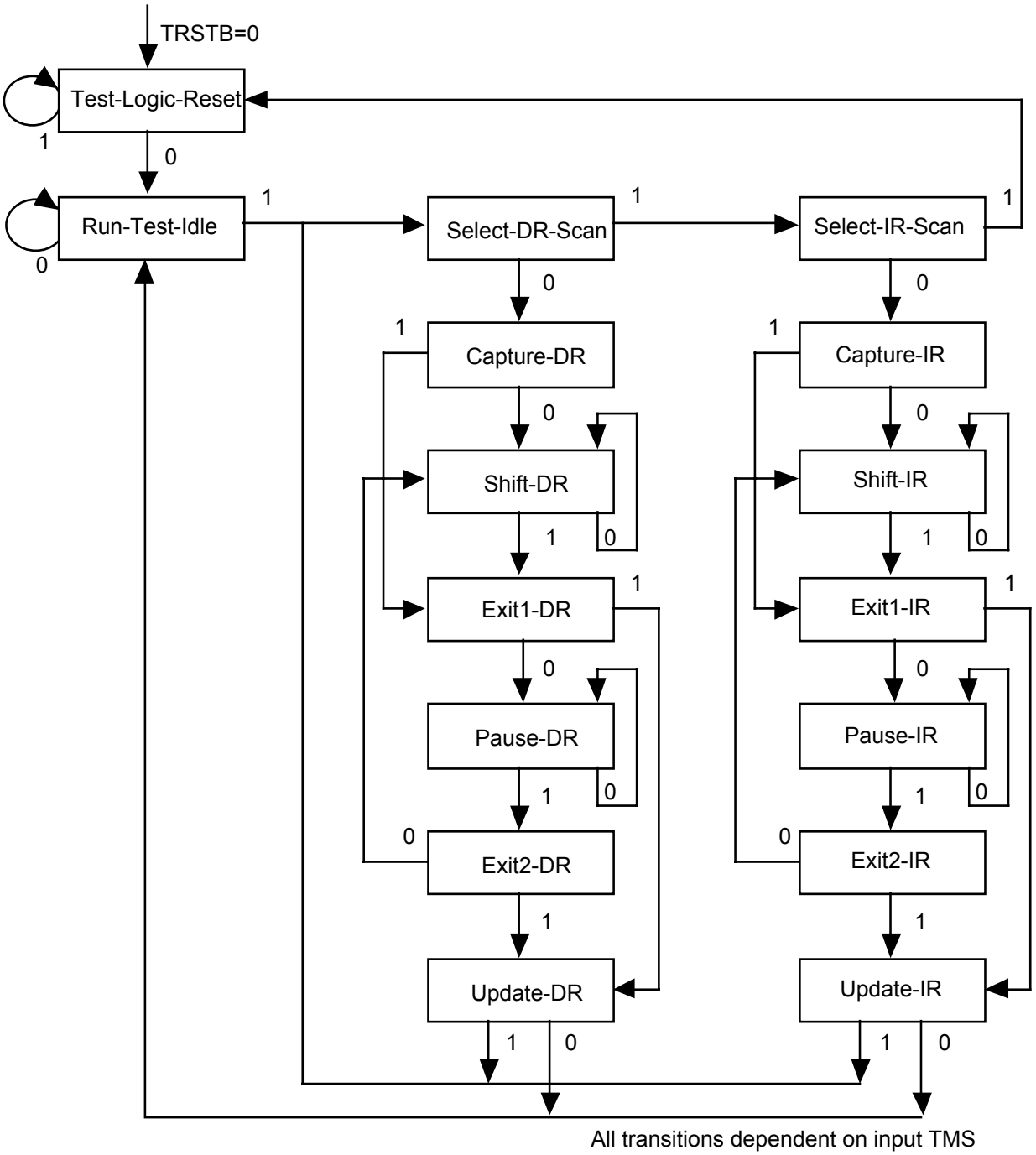
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. A description of the finite state machine follows:

Figure 33 - TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

Table 5 - Instruction Register

Length - 3 bits

Instructions	Selected Register Boundary Scan	Instruction Codes (IR[2:0])
EXTEST		000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device

inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

14.3.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located in the TEST FEATURES DESCRIPTION - JTAG Test Port section.

Figure 34 - Input Observation Cell (IN_CELL)

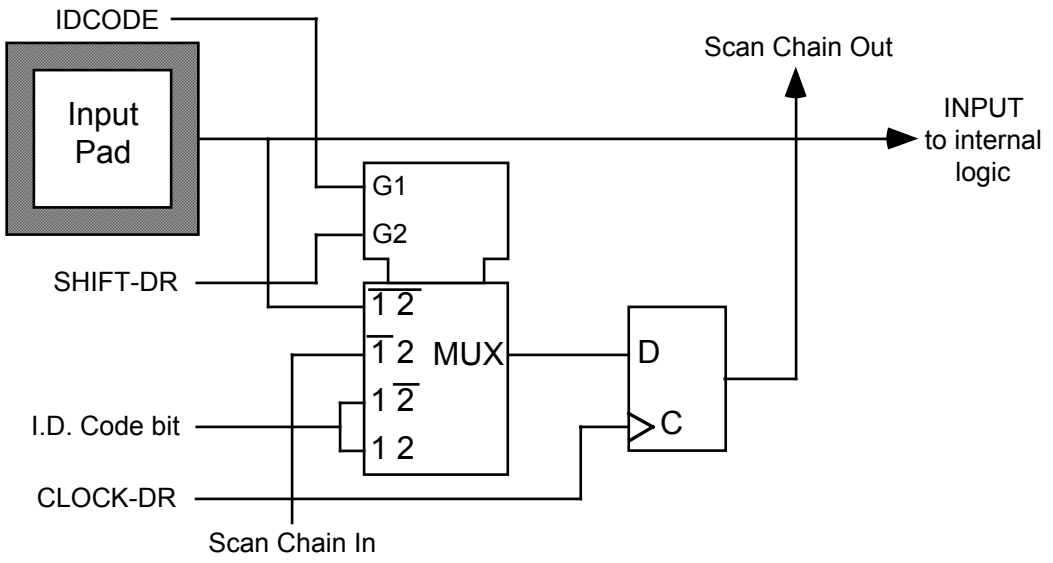


Figure 35 - Output Cell (OUT_CELL)

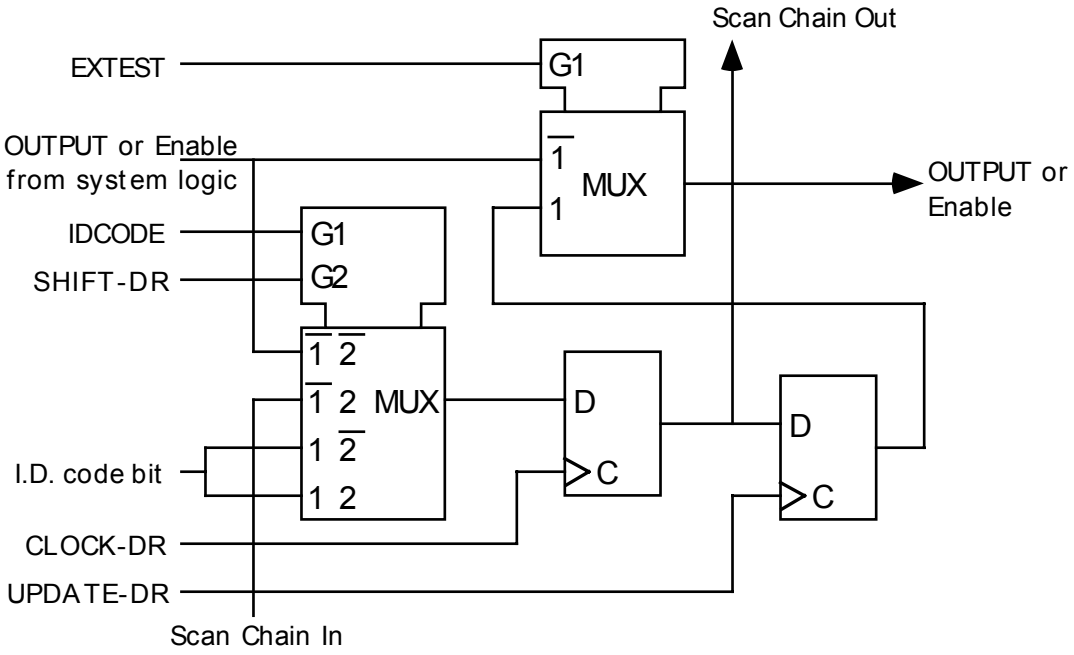


Figure 36 - Bidirectional Cell (IO_CELL)

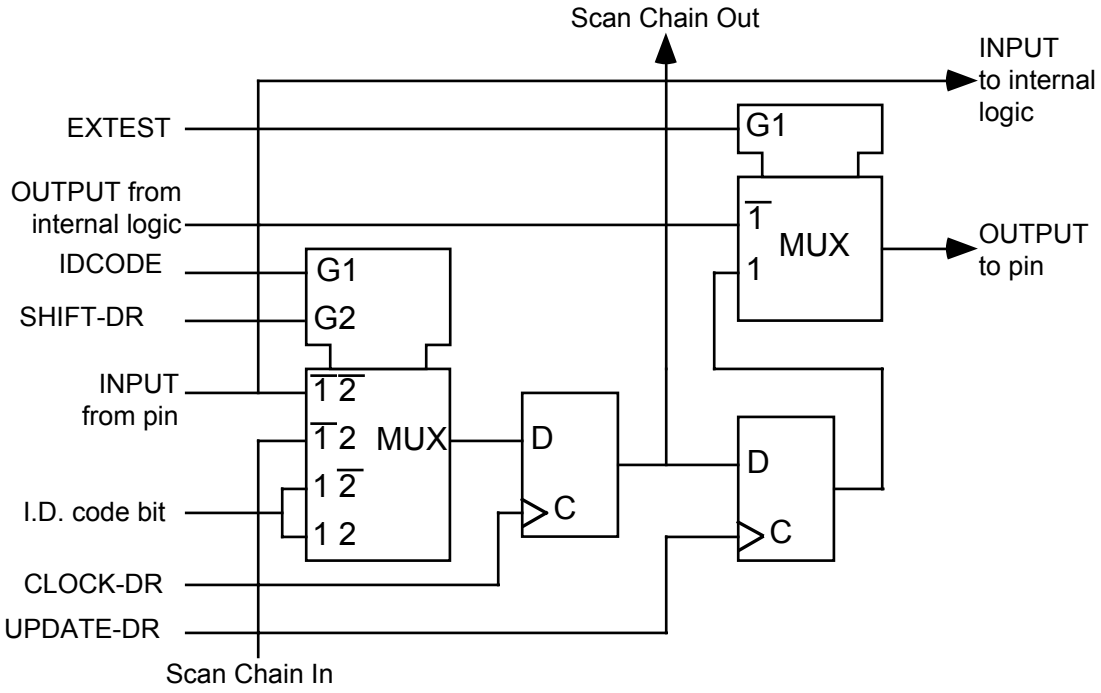
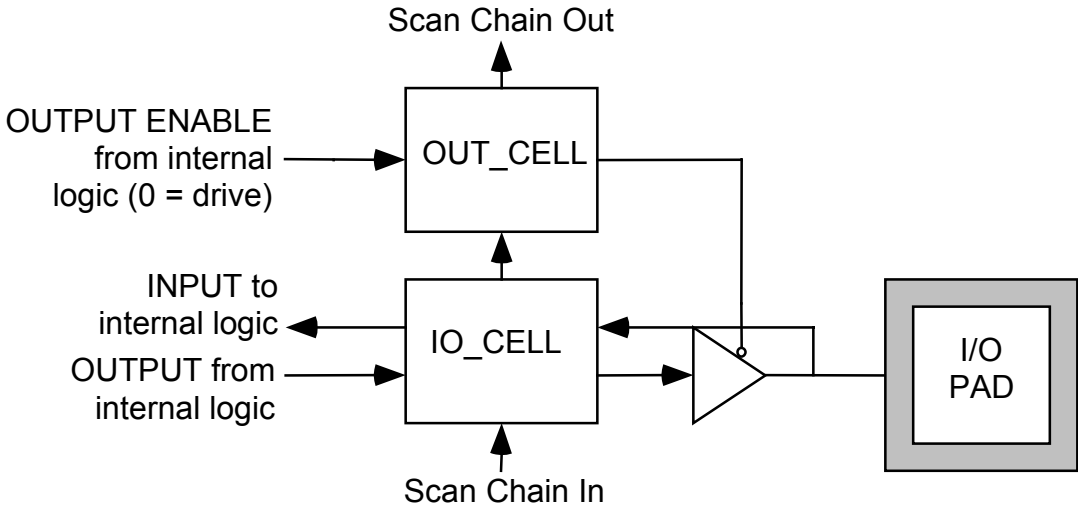


Figure 37 - Layout of Output Enable and Bidirectional Cells



15 ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on VDD with Respect to GND	-0.5V to +7.0V
Voltage on Any Pin	VSS-0.5V to VDD+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current (T_A = -40°C to +85°C)	±100 mA

16 CAPACITANCE

Symbol	Parameter	Typical	Units	Conditions
Cin	Input Capacitance	5	pF	T_A = 25°C, f = 1 MHz
Cout	Output Capacitance	5	pF	T_A = 25°C, f = 1 MHz
Cbidir	Bidirectional Capacitance	5	pF	T_A = 25°C, f = 1 MHz

17 D.C. CHARACTERISTICS

TA= -40° to +85°C, VDD=5V ±10%

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	4.5	5	5.5	Volts	
V_{IL}	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0		V_{DD} +0.5	Volts	Guaranteed Input HIGH Voltage
V_{OL} (TTL)	Output or Bidirectional Low Voltage		0.1	0.4	Volts	V_{DD} = min, I_{OL} = -4 mA for D[7:0], all FIFO outputs, TCLKO[4:1], and RCLKO and -2 mA for others. Note 3, 4
V_{OH} (TTL)	Output or Bidirectional High Voltage	3.5	4.5		Volts	V_{DD} = min, I_{OL} = 4 mA for D[7:0], all FIFO outputs, TCLKO[4:1], and RCLKO and 2 mA for others. Note 3, 4
V_{T+}	Reset Input High Voltage	3.5			Volts	Applies to RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage			0.6	Volts	Applies to RSTB and TRSTB only.
V_{TH}	Reset Input Hysteresis Voltage		0.8		Volts	Applies to RSTB and TRSTB only.
I_{ILPU}	Input Low Current	+100	+340	+525	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}, Notes 1, 3

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}, Notes 2, 3
I_{DDOP1}	Operating Current (T1 format)		29	50	mA	V_{DD} = 5.5 V, Outputs Unloaded, XCLK = 37.056 MHz, TCLKI = 1.544 MHz, RDP[4:1]/RDN[4:1] = 1.544 Mbit/s, RFCLK = 25 MHz, TFCLK = 25 MHz
I_{DDOP2}	Operating Current (E1 format)		33	55	mA	V_{DD} = 5.5 V, Outputs Unloaded, XCLK = 49.152 MHz, TCLKI = 2.048 MHz, RDP[4:1]/RDN[4:1] = 2.048 Mbit/s, RFCLK = 25 MHz, TFCLK = 25 MHz
I_{DDOP3}	Operating Current (J2 format)		24	45	mA	V_{DD} = 5.5 V, Outputs Unloaded, TCLKI = 6.312 MHz RCLKI[4:1] = 6.312 MHz, RFCLK = 25 MHz, TFCLK = 25 MHz
I_{DDOP4}	Operating Current (Arbitrary format)		48	75	mA	V_{DD} = 5.5 V, Outputs Unloaded, TCLKI = 25 MHz, RCLKI[4:1] = 25 MHz, RFCLK = 25 MHz, TFCLK = 25 MHz

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. FIFO output pins include: RDAT[7:0], RXPRTY, RSOC, RCAMPH, RCA[4:1], TCAMPH, and TCA[4:1]

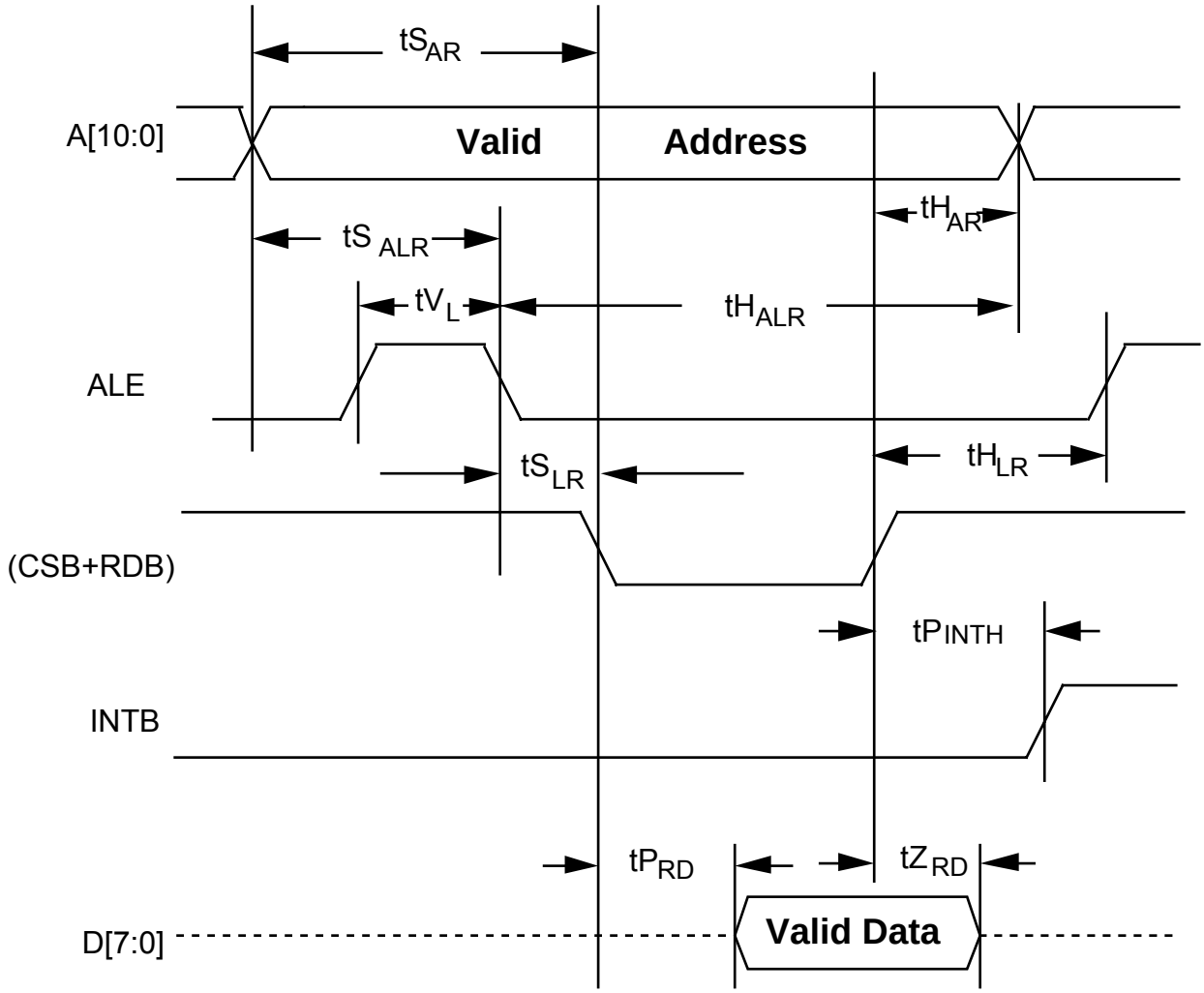
18 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

TA= -40° to +85°C, VDD=5V ±10%

Table 6 - Microprocessor Read Access (Figure 38)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to INTB high		50	ns

Figure 38 - Microprocessor Read Access Timing



Notes on Microprocessor Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. Microprocessor Interface timing applies to normal mode register accesses only.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

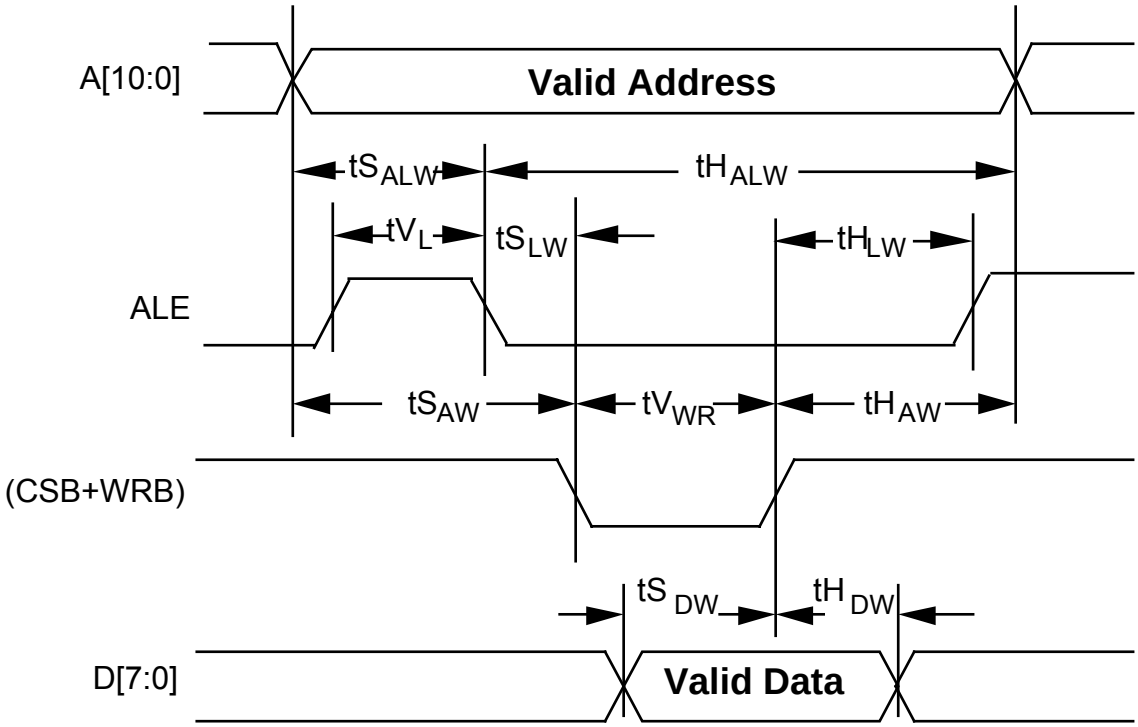
7. In non-multiplexed address/data bus architectures ALE can be held high; parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.

8. Parameter tH_{AR} is not applicable when address latching is used.

Table 7 - Microprocessor Write Access (Figure 39)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 39 - Microprocessor Write Access Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. Microprocessor Interface timing applies to normal mode register accesses only.

3. In non-multiplexed address/data bus architectures, ALE can be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW}, and tH_{LW} are not applicable.

4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.

5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

19 S/UNI-MPH I/O TIMING CHARACTERISTICS

TA= -40° to +85°C, VDD=5V ±10%

Table 8 - XCLK Input for Jitter Attenuation (Figure 40)

Symbol	Description	Min	Max	Units
t_{XCLK}	XCLK Frequency (typically 37.056 MHz ± 100 ppm for T1 format or 49.152 MHz ± 50 ppm for E1 format)[3]		50	MHz
tD_{XCLK}	XCLK Duty Cycle (at XCLK = 37.056 MHz for T1, 49.152 MHz for E1)[5]	40	60	%

Figure 40 - XCLK Input Timing for Jitter Attenuation

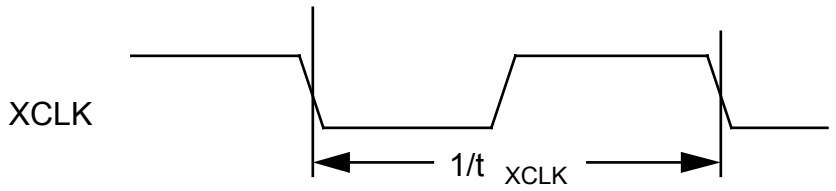


Table 9 - TCLKI Input (Figure 41)

Symbol	Description	Min	Max	Units
$t_{T1TCLKI}$	TCLKI Frequency for T1[3,4] (nominally 1.544 MHz ± 130 ppm)		1.545	MHz
$t_{E1TCLKI}$	TCLKI Frequency for E1[3,4] (nominally 2.048 MHz ± 50 ppm)		2.049	MHz
$t_{J2TCLKI}$	TCLKI Frequency for J2 bit rate format		7	MHz
$t_{ARTCLKI}$	TCLKI Frequency for arbitrary bit rate format		25	MHz
tH_{TTCLKI}	TCLKI High Duration (for T1 formats)[6]	165		ns

Symbol	Description	Min	Max	Units
$t_{LTTCLKI}$	TCLKI Low Duration (for T1 formats)[6]	165		ns
$t_{HETCLKI}$	TCLKI High Duration (for E1 formats)[6]	125		ns
$t_{LETCLKI}$	TCLKI Low Duration (for E1 formats)[6]	125		ns
$t_{HJTCLKI}$	TCLKI High Duration (for J2 formats)	50		ns
$t_{LJTCLKI}$	TCLKI Low Duration (for J2 formats)	50		ns
$t_{HATCLKI}$	TCLKI High Duration (for arbitrary formats)	16		ns
$t_{LATCLKI}$	TCLKI Low Duration (for arbitrary formats)	16		ns
t_{STCLKI}	TCLKI to TFPI Input Set-up Time[1]	5		ns
t_{HTCLKI}	TCLKI to TFPI Input Hold-up Time[2]	10		ns

Figure 41 - TCLKI Input Timing

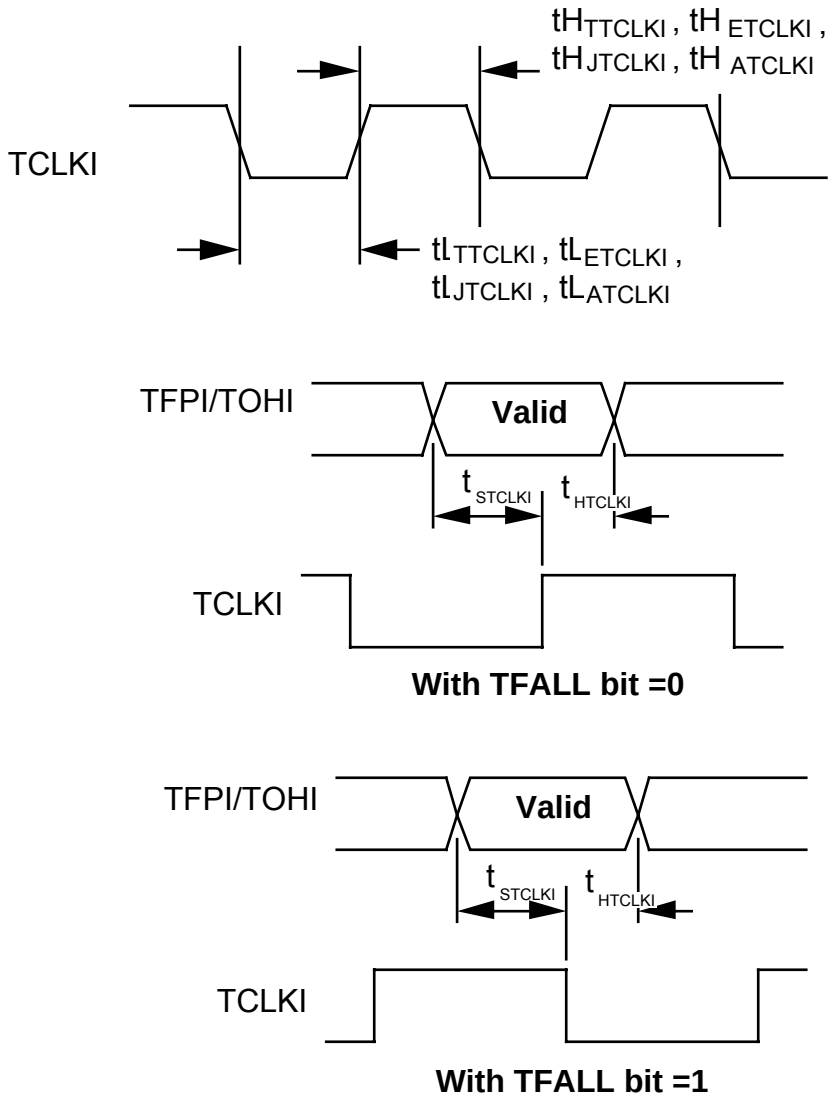
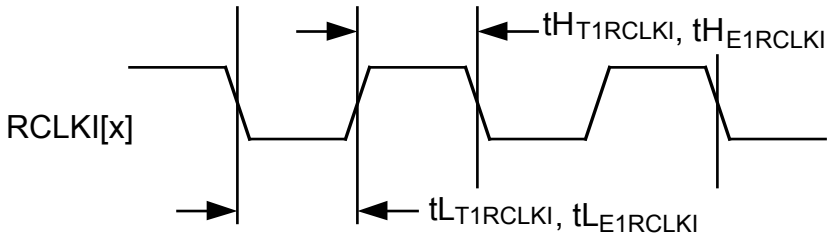


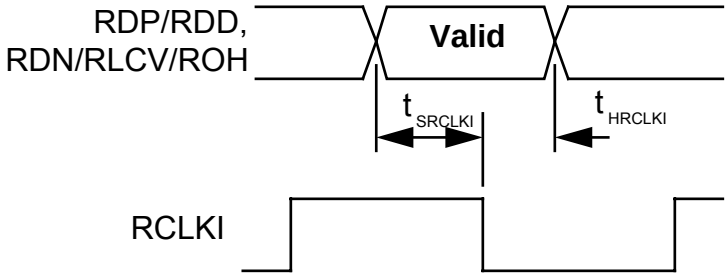
Table 10 - Digital Receive Interface Input Timing (Figure 42)

Symbol	Description	Min	Max	Units
$t_{T1RCLKI}$	RCLKI[x] Frequency for T1 format[3,6] (nominally 1.544 MHz ± 130 ppm)		1.6	MHz
$t_{LT1RCLKI}$	RCLKI[x] Low Duration (T1 format)[6]	250		ns

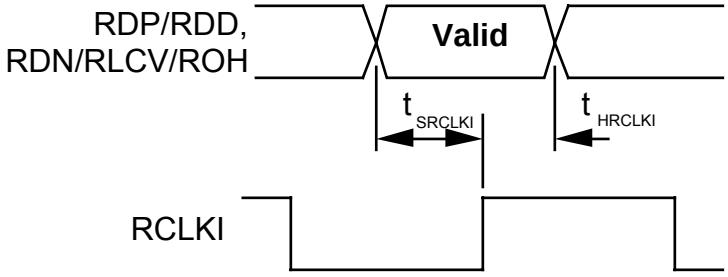
Symbol	Description	Min	Max	Units
$t_{HT1RCLKI}$	RCLKI[x] High Duration (T1 format)[6]	250		ns
$t_{E1RCLKI}$	RCLKI[x] Frequency for E1 format[3,6] (nominally 2.048 MHz ± 50 ppm)		2.2	MHz
$t_{LE1RCLKI}$	RCLKI[x] Low Duration (E1 format)[6]	190		ns
$t_{HE1RCLKI}$	RCLKI[x] High Duration (E1 format)[6]	190		ns
$t_{J2RCLKI}$	RCLKI[x] Frequency for J2 format (nominally 6.312 MHz)		7	MHz
$t_{ARRCLKI}$	RCLKI[x] Frequency for other bit rate formats		25	MHz
t_{DRCLKI}	Digital Receive Clock Duty Cycle (J2 and Arbitrary formats)	40	60	%
t_{SRCLKI}	RCLKI to NRZ Digital Receive Input Set-up Time[1]	5		ns
t_{HRCLKI}	RCLKI to NRZ Digital Receive Input Hold Time[2]	5		ns
t_{WTRDPN}	RZ Digital Receive Input Pulse Width (T1 format)[6]	100	540	ns
t_{WERDPN}	RZ Digital Receive Input Pulse Width (E1 format)[6]	100	380	ns

Figure 42 - Digital Receive Interface Input Timing Diagram

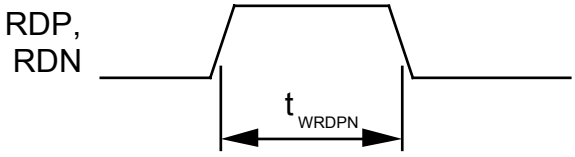




With RFALL bit = 1



With RFALL bit = 0



With Clock Recovery Enabled

Table 11 - Transmit Data Link Input Timing (Figure 43)

Symbol	Description	Min	Max	Units
tS_{DIN}	TDLCLK[x] to TDLSIG[x] Input Set-up Time[1]	80		ns
tH_{DIN}	TDLCLK[x] to TDLSIG[x] Input Hold Time[2]	20		ns

Figure 43 - Transmit Data Link Input Timing Diagram

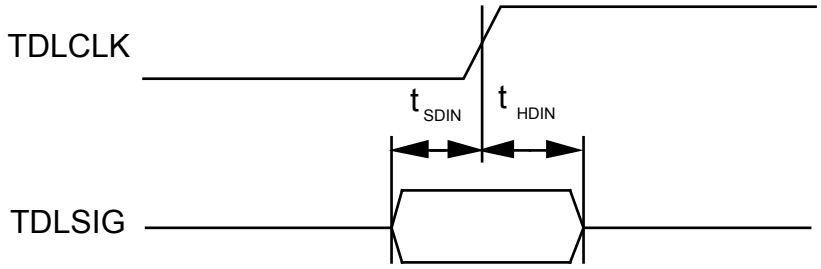


Table 12 - Receive Data Link Output Timing (Figure 44)

Symbol	Description	Min	Max	Units
tP_{RDLCLK}	RDLCLK[x] to RDLSIG[x] Propagation Delay[7,8]		50	ns

Figure 44 - Receive Data Link Output Timing Diagram

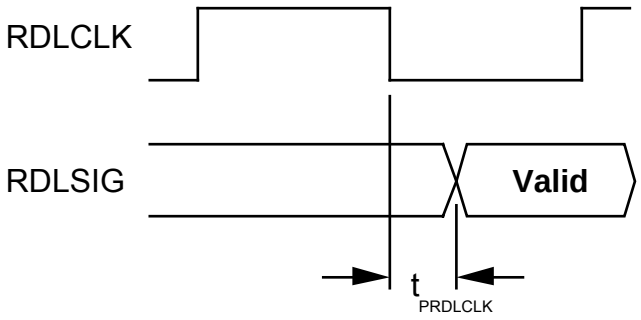


Table 13 - Transmit Interface Output Timing (Figure 45)

Symbol	Description	Min	Max	Units
t_{PTCLKO}	TCLKO to Digital Transmit Data Output Signals Propagation Delay[7,8]		15	ns
t_{PTCLKI}	TCLKI to TDP[4:1] and TDN[4:1] Propagation Delay[7,8] *Valid only if LINELB=0, PAYLB=0, TREF[1:0]=00, with J2 format or Arbitrary format or T1/E1 format with FIFOBYP=1		33	ns

Figure 45 - Transmit Interface Output Timing Diagram

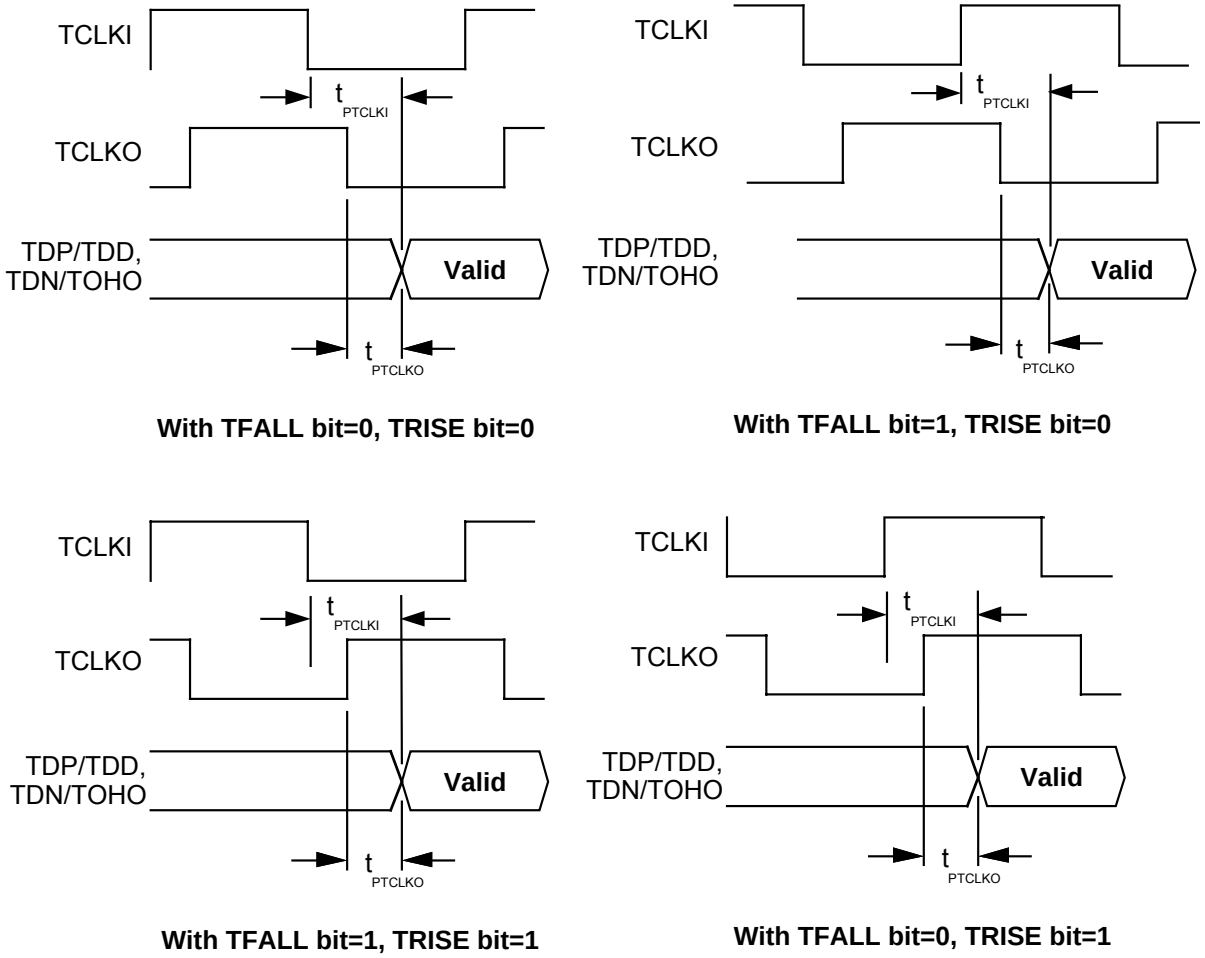


Table 14 - Transmit Data Link DMA Interface Output Timing (Figure 46)

Symbol	Description	Min	Max	Units
tP_{TINT}	Transmit Data Register Serviced (WRB low) to TDLINT[x] Low Propagation Delay[7,8]		50	ns
tP_{TUDR}	Transmit Data Register Serviced (WRB high) to TDLUDR[x] Low Propagation Delay[7,8]		50	ns

Figure 46 - Transmit Data Link DMA Interface Output Timing Diagram

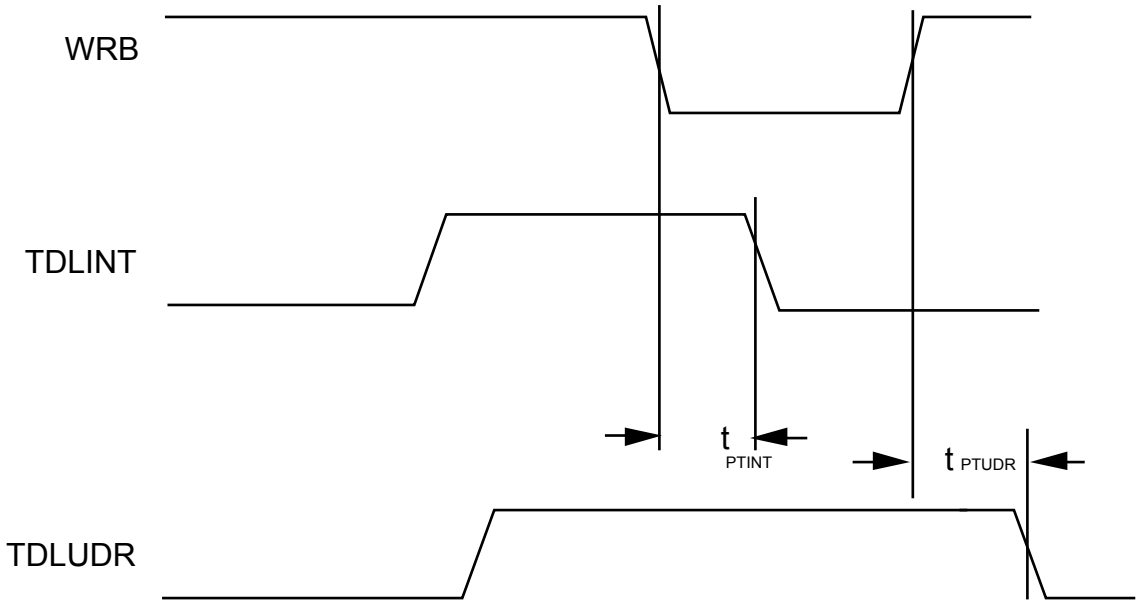


Table 15 - Receive Data Link DMA Interface Output Timing (Figure 47)

Symbol	Description	Min	Max	Units
tP_{RINT}	Receive Data Register Serviced (RDB low) to RDLINT[x] Low Propagation Delay[7,8]		70	ns
tP_{R1EOM}	Receive Data Register Serviced (RDB low) to RDLEOM[x] High Propagation Delay[7,8]		80	ns
tP_{R2EOM}	Receive Status Register Serviced (RDB high) to RDLEOM[x] Low Propagation Delay[7,8]		50	ns

Figure 47 - Receive Data Link DMA Interface Output Timing Diagram

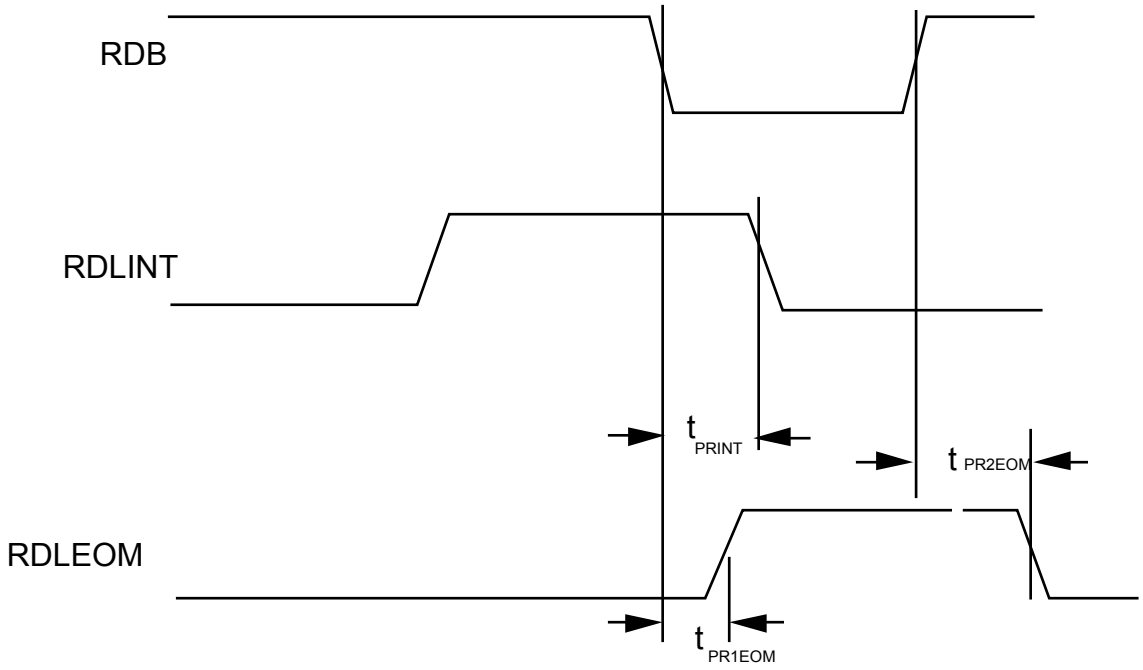


Table 16 - Transmit Cell Interface Timing (Figure 48)

Symbol	Description	Min	Max	Units
tD_{TFCLK}	TFCLK Duty Cycle[5]	40	60	%
tS_{TWRENB}	TWRENB[x] Set-up time to TFCLK (or TWA[1:0], TWRMPHB if MPHEN = 1)[1]	10		ns
tH_{TWRENB}	TWRENB Hold time to TFCLK (or TWA[1:0], TWRMPHB if MPHEN = 1)[2]	1		ns
tS_{TDAT}	TDAT[7:0] Set-up time to TFCLK[1]	10		ns
tH_{TDAT}	TDAT[7:0] Hold time to TFCLK[2]	1		ns
tS_{TXPRTY}	TXPRTY Set-up time to TFCLK[1]	10		ns
tH_{TXPRTY}	TXPRTY Hold time to TFCLK[2]	1		ns
tS_{TSOC}	TSOC Set-up time to TFCLK[1]	10		ns
tH_{TSOC}	TSOC Hold time to TFCLK[2]	1		ns
tP_{TCA}	TFCLK High to TCA Valid (and TCAMPH if MPHEN=1)[7,8]	4	25	ns

Figure 48 - Transmit Cell Interface Timing Diagram

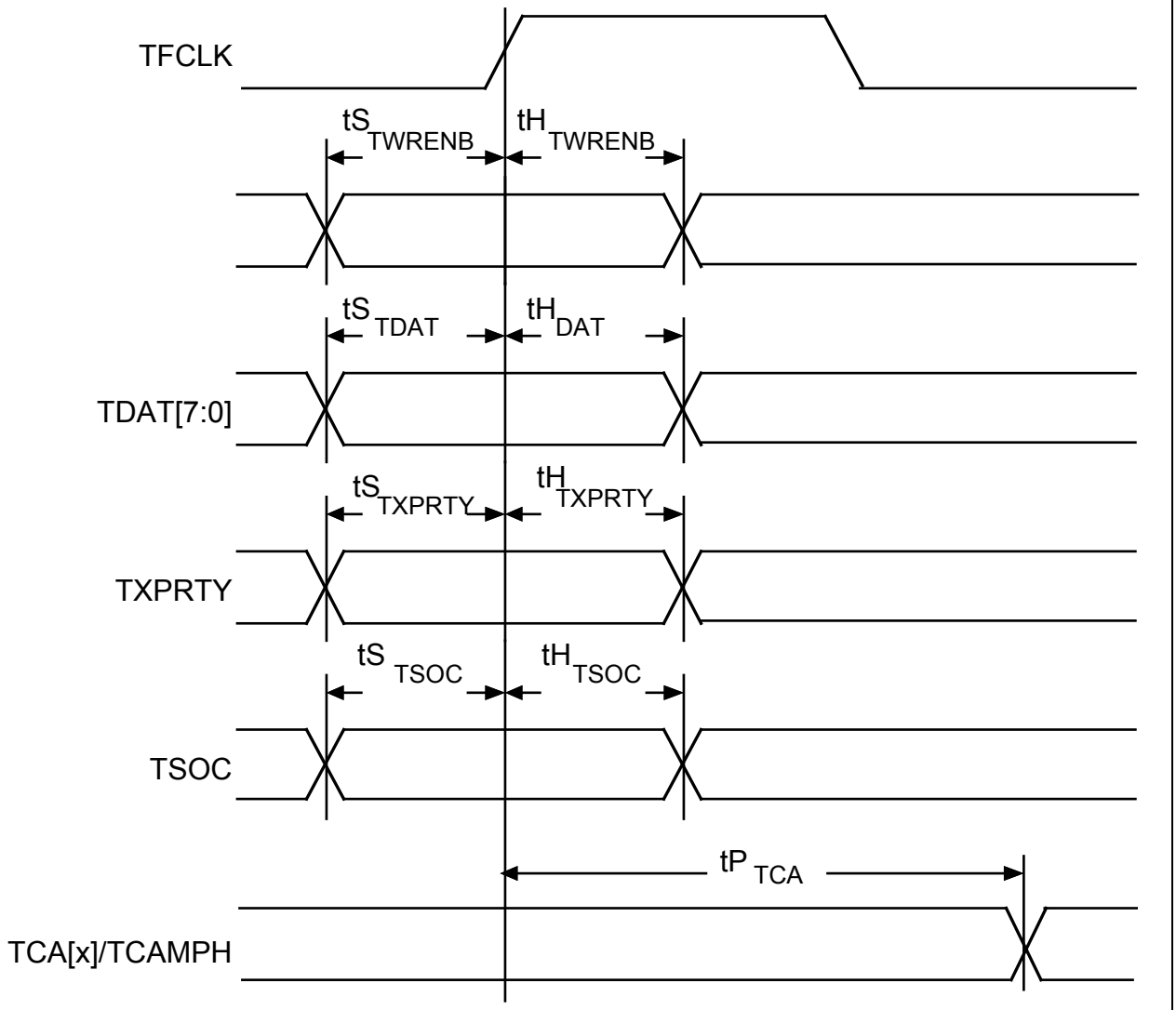
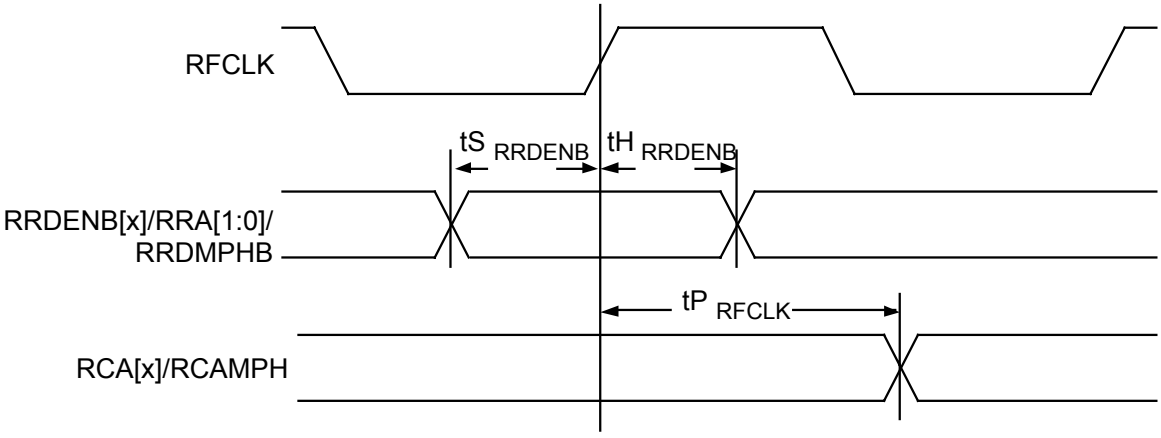


Table 17 - Receive Cell Interface Timing (Figure 49)

Symbol	Description	Min	Max	Units
t_{RFCLK}	RFCLK Frequency		25	MHz
tD_{RFCLK}	RFCLK Duty Cycle[5]	40	60	%
tS_{RRDENB}	RRDENB[x] Set-up time to RFCLK (or RRA[1:0], RRDMPHB if MPHEN = 1)[1]	10		ns

Symbol	Description	Min	Max	Units
tH_{RRDENB}	RRDENB[x] Hold time to RFCLK (or RRA[1:0], RRDMPHB if MPHEN = 1)[2]	1		ns
tP_{RFCLK}	RFCLK High to Output Valid[7,8]	4	25	ns
tZ_{RFCLK}	RFCLK High to Output Tristate	4	20	ns
tZB_{RFCLK}	RFCLK High to Output Driven[6]	0		ns

Figure 49 - Receive Cell Interface Timing Diagram



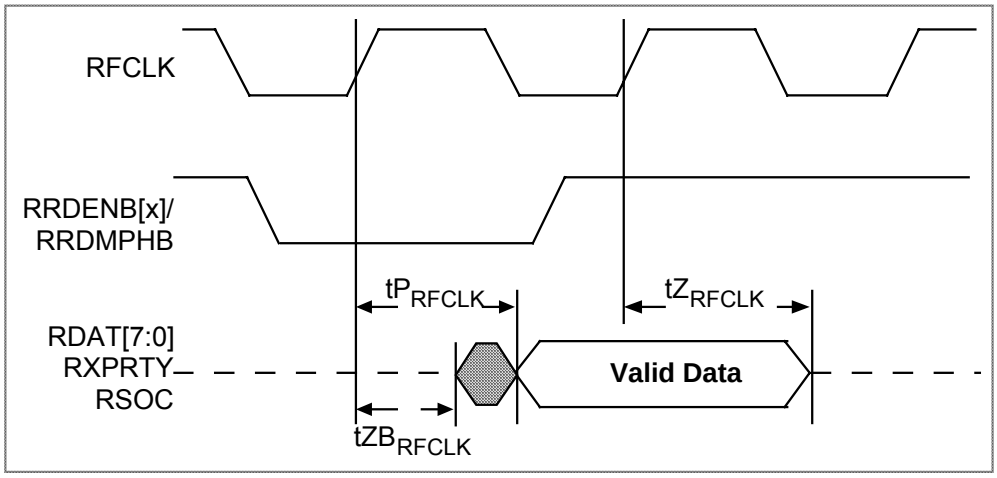
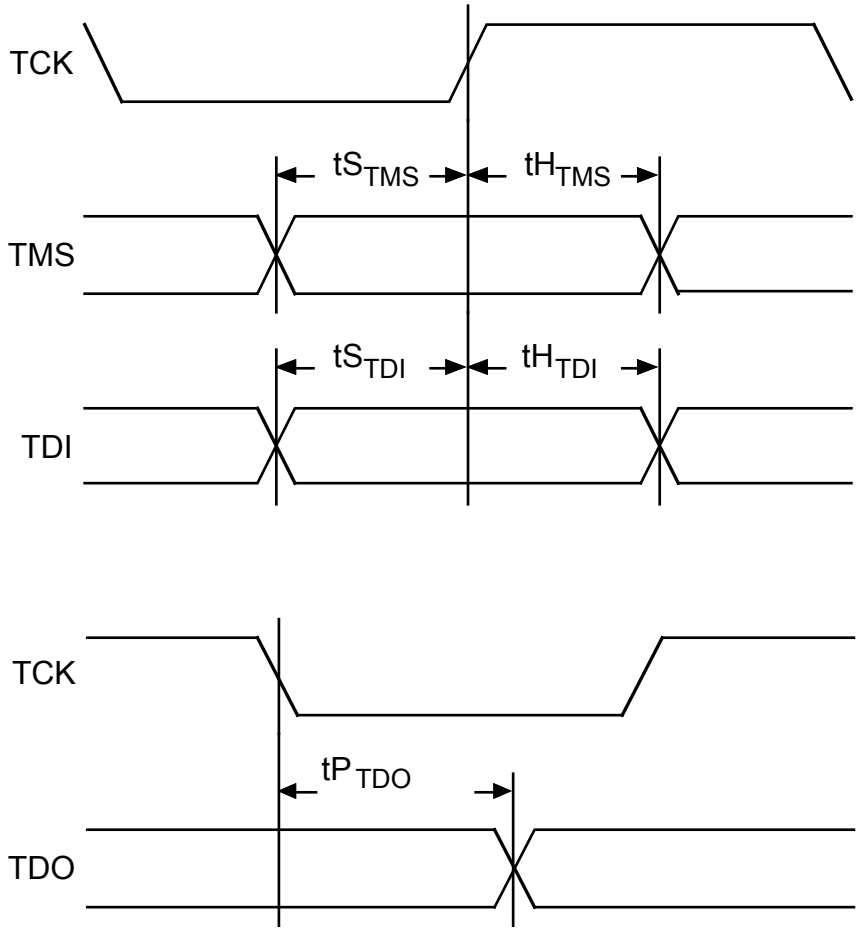


Table 18 - JTAG Port Interface Timing (Figure 50)

Symbol	Description	Min	Max	Units
t_{TCK}	TCK Frequency		1	MHz
t_{DTCK}	TCK Duty Cycle[5]	40	60	%
t_{STMS}	TMS Set-up time to TCK[1]	50		ns
t_{HTMS}	TMS Hold time to TCK[2]	50		ns
t_{STDI}	TDI Set-up time to TCK[1]	50		ns
t_{HTDI}	TDI Hold time to TCK[2]	50		ns
t_{PTDO}	TCK Low to TDO Valid[7,8]	2	50	ns

Figure 50 - JTAG Port Interface Timing Diagram



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. These clock tolerances assume that the line clock tolerance is ±130ppm for T1 and ±50ppm for E1.

4. TCLKI can be a jittered clock signal subject to the instantaneous frequencies corresponding to the minimum and maximum high and low TCLKI pulse widths shown.

5. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

6. Guaranteed by design for nominal XCLK frequencies. May not be production tested.

Notes on Output Timing:

7. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

8. Output propagation delays are measured with a 50 pF load on the outputs except on D[7:0] where the load is 100 pF.

20 ORDERING AND THERMAL INFORMATION

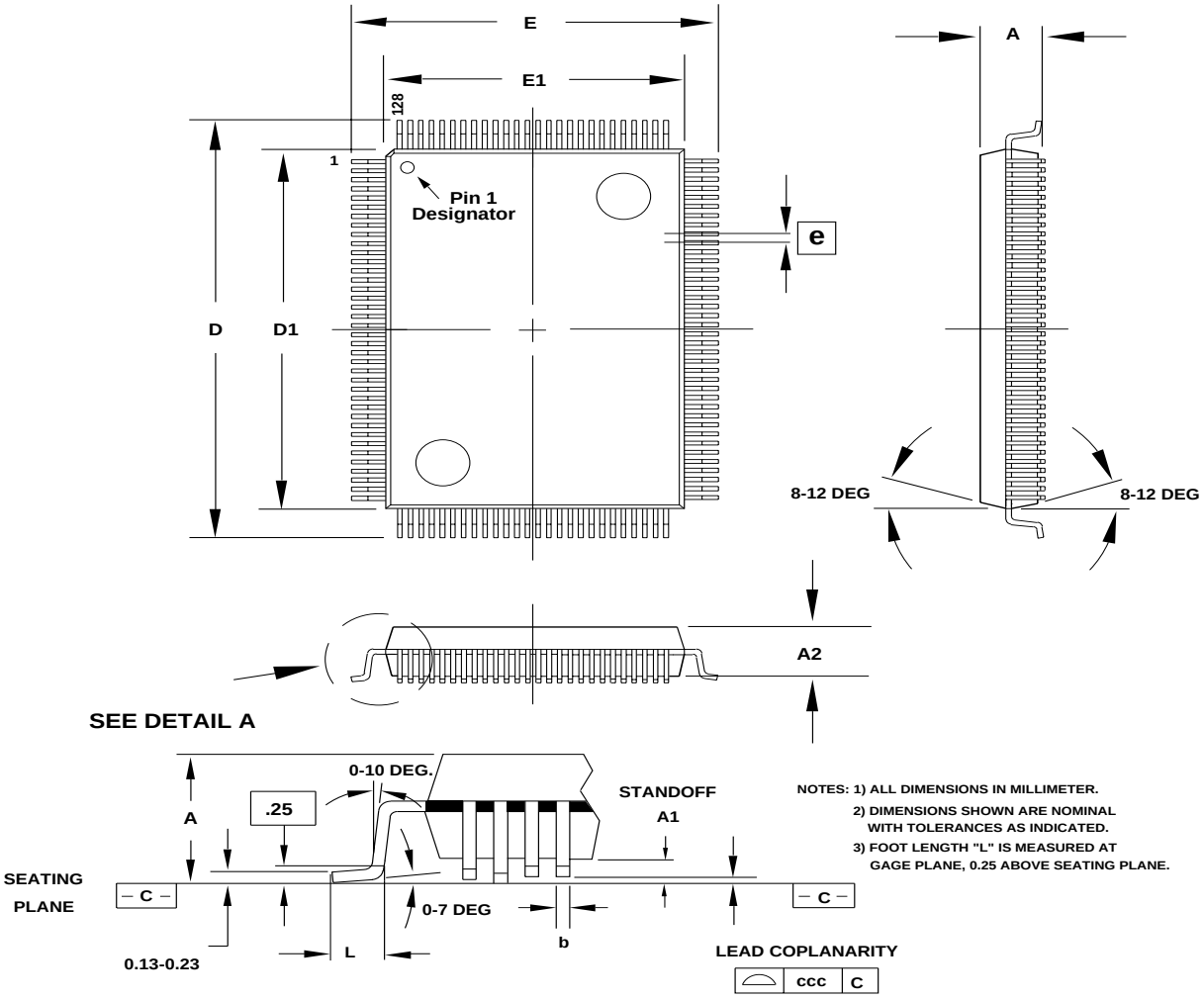
Table 19 - S/UNI-MPH Ordering Information

PART NO.	DESCRIPTION
PM7344	128 Plastic Quad Flat Pack (PQFP)

Table 20 - S/UNI-MPH Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM7344	-40°C to 85°C	41 °C/W	19 °C/W

21 MECHANICAL INFORMATION



PACKAGE TYPE: 128 PIN METRIC RECTANGULAR PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 14 x 20 x 2.7 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	2.82	0.25	2.57	22.95	19.90	16.95	13.90	0.73		0.17	
Nom.			2.70	23.20	20.00	17.20	14.00	0.88	0.50	0.22	
Max.	3.40	0.53	2.87	23.45	20.10	17.45	14.10	1.03		0.27	0.10

NOTES

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