PM4314

QDSX

QUAD T1/E1 LINE INTERFACE DEVICE

DATA SHEET

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CONTENTS

1 FEATURES 1

2 APPLICATIONS 5

3 REFERENCES 6

4 APPLICATION EXAMPLES 8

5 BLOCK DIAGRAM 13

6 DESCRIPTION 15

7 PIN DIAGRAM 18

8 PIN DESCRIPTION 19

9 FUNCTIONAL DESCRIPTION 32

9.1 ANALOG PULSE SLICER (RSLC) 32

9.2 CLOCK AND DATA RECOVERY (CDRC) 35

9.3 LINE CODE VIOLATION PERFORMANCE MONITOR (LCV_PMON) 39

9.4 INBAND LOOPBACK CODE DETECTOR (IBCD) 40

9.5 PSEUDO-RANDOM BIT SEQUENCE MONITOR (PRSM) 40

9.6 TIMING OPTIONS (TOPS) 42

9.7 PSEUDO-RANDOM BIT SEQUENCE GENERATOR (PRSG) 42

9.8 INBAND LOOPBACK CODE GENERATOR (XIBC) 43

9.9 B8ZS/HDB3/AMI LINE ENCODER (LCODE) 43

9.10 DIGITAL JITTER ATTENUATOR (DJAT) 43

9.11 ANALOG PULSE GENERATOR (XPLS) 49

9.12 IEEE P1149.1 JTAG TEST ACCESS PORT 52
9.13 MICROPROCESSOR INTERFACE 52
9.14 REGISTER MEMORY MAP 53
10 NORMAL MODE REGISTER DESCRIPTION 56
11 TEST FEATURES DESCRIPTION 113
11.1 TEST MODE 0 DETAILS 114
11.2 JTAG TEST PORT 116
12 OPERATIONS 119
12.1 PROGRAMMING THE XPLS WAVEFORM TEMPLATE 122
12.2 USING THE DIGITAL JITTER ATTENUATOR 127
12.3 USING XPLS WITHOUT DJAT 128
12.3.1 FIFO NOT IN TX PATH, XSEL[1] = 0 129
12.3.2 FIFO NOT IN TX PATH, XSEL[1] = 1, XSEL[0] = 0 129
12.3.3 FIFO IS IN TX PATH, XSEL[1] = 1, XSEL[0] = 0. 129
12.3.4 FIFO NOT IN TX PATH, XSEL[1] = 1, XSEL[0] = 1 129
12.3.5 FIFO IS IN TX PATH, XSEL[1] = 1, XSEL[0] = 1 130
12.4 JTAG SUPPORT 130
13 FUNCTIONAL TIMING 141
13.1 LINE CODE VIOLATION INSERTION 141
14 ABSOLUTE MAXIMUM RATINGS 144
15 CAPACITANCE 145
16 D.C. CHARACTERISTICS 146
17 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS 149

18 A.C. TIMING CHARACTERISTICS 153

19 ORDERING AND THERMAL INFORMATION 163

20 MECHANICAL INFORMATION 164

LIST OF REGISTERS

REGISTER 000H, 040H, 080H, AND 0C0H: RECEIVE CONFIGURATION.....57

REGISTER 001H, 041H, 081H, AND 0C1H: TRANSMIT CONFIGURATION ...60

REGISTER 002H, 042H, 082H, AND 0C2H: TX/RX BLOCK PLACEMENT.....62

REGISTER 003H, 043H, 083H, AND 0C3H: INTERRUPT SOURCE 64

REGISTER 005H, 045H, 085H, AND 0C5H: DIAGNOSTICS 65

REGISTER 006H OR 106H: MASTER TEST.....67

REGISTER 007H: REVISION/CHIP ID/GLOBAL MONITORING UPDATE 70

REGISTER 008H: INTERRUPT QUADRANT ID.....71

REGISTER 009H: TOPS MASTER CLOCK CONFIGURATION/CLOCK ACTIVITY MONITOR.....72

REGISTER 00AH, 04AH, 08AH, AND 0CAH: TOPS CLOCK TIMING OPTIONS 74

REGISTER 00BH, 04BH, 08BH, AND 0CBH: LCODE TRANSMIT LINE CODE CONFIGURATION.....76

REGISTER 010H, 050H, 090H, AND 0D0H: CDRC CONFIGURATION.....77

REGISTERS 011H, 051H, 091H AND 0D1H: CDRC INTERRUPT ENABLE....79

REGISTERS 012H, 052H, 092H AND 0D2H: CDRC INTERRUPT STATUS.....80

REGISTER 014H, 054H, 094H, AND 0D4H: LCV_PMON INTERRUPT ENABLE/STATUS 81

REGISTERS 01AH-01BH, 05AH-05BH, 09AH-09BH, 0DAH-0DBH: LATCHING LCV PERFORMANCE DATA 82

REGISTERS 01AH, 05AH, 09AH AND 0DAH: LCV_PMON LINE CODE VIOLATION COUNT LSB 83

REGISTERS 01BH, 05BH, 09BH AND 0DBH: LCV_PMON LINE CODE VIOLATION COUNT MSB 84

REGISTERS 01CH, 05CH, 09CH AND 0DCH: DJAT INTERRUPT STATUS 85

REGISTER 01DH, 05DH, 09DH AND 0DDH: DJAT REFERENCE CLOCK DIVISOR (N1) CONTROL 86

REGISTERS 01EH, 05EH, 09EH AND 0DEH: DJAT OUTPUT CLOCK DIVISOR (N2) CONTROL 87

REGISTERS 01FH, 05FH, 09FH AND 0DFH: DJAT CONFIGURATION 88

REGISTERS 020H, 060H, 0A0H AND 0E0H: IBCD CONFIGURATION 90

REGISTERS 021H, 061H, 0A1H AND 0E1H: IBCD INTERRUPT ENABLE/STATUS 91

REGISTERS 022H, 062H, 0A2H AND 0E2H: IBCD ACTIVATE CODE 93

REGISTERS 023H, 063H, 0A3H AND 0E3H: IBCD DEACTIVATE CODE 94

REGISTERS 024H, 064H, 0A4H AND 0E4H: XIBC CONTROL 95

REGISTERS 025H, 065H, 0A5H AND 0E5H: XIBC LOOPBACK CODE 97

REGISTER 027H, 067H, 0A7H, 0E7H: PRSG CONFIGURATION 98

REGISTER 029H, 069H, 0A9H, 0E9H: PRSM CONTROL/STATUS 99

REGISTER 02AH, 06AH, 0AAH, 0EAH: PRSM BIT ERROR EVENT COUNT LSB 102

REGISTER 02BH, 06BH, 0ABH, 0EBH: PRSM BIT ERROR EVENT COUNT MSB 103

REGISTER 02CH, 06CH, 0ACH, 0ECH: XPLS LINE LENGTH CONFIGURATION 104

REGISTER 02DH, 06DH, 0ADH, 0EDH: XPLS CONTROL/STATUS 106

REGISTER 02EH, 06EH, 0AEH, 0EEH: XPLS CODE INDIRECT ADDRESS 108

REGISTER 02FH, 06FH, 0AFH, 0EFH: XPLS CODE INDIRECT DATA 110

REGISTER 030H, 070H, 0B0H, 0F0H: RSLC CONFIGURATION 111

REGISTER 031H, 071H, 0B1H, 0F1H: RSLC INTERRUPT ENABLE/STATUS112

LIST OF FIGURES

FIGURE 1 - EXAMPLE 1. T1 OR E1 ATM INTERFACES 8

FIGURE 2 - EXAMPLE 2. DSX-1 DIGITAL ACCESS CROSS CONNECTS (DACS) 10

FIGURE 3 - EXAMPLE 3. MULTIPLEXERS (M13) 12

FIGURE 4 - NORMAL OPERATING MODE 13

FIGURE 5 - LOOPBACK MODES 14

FIGURE 6 - EXTERNAL ANALOG RECEIVE INTERFACE CIRCUIT 34

FIGURE 7 - DSX-1 JITTER TOLERANCE 37

FIGURE 8 - E1 JITTER TOLERANCE WITH ALGSEL = 1 38

FIGURE 9 - E1 JITTER TOLERANCE WITH ALGSEL = 0 39

FIGURE 10 - DSX-1 JITTER TOLERANCE 45

FIGURE 11 - E1 JITTER TOLERANCE 46

FIGURE 12 - DJAT MINIMUM JITTER TOLERANCE VS. XCLK ACCURACY (DSX-1 CASE) 47

FIGURE 13 - DJAT MINIMUM JITTER TOLERANCE VS. XCLK ACCURACY (E1 CASE) 47

FIGURE 14 - DSX-1 JITTER TRANSFER 48

FIGURE 15 - E1 JITTER TRANSFER 49

FIGURE 16 - EXTERNAL ANALOG TRANSMIT INTERFACE CIRCUIT 51

FIGURE 17 - TIMING OPTIONS 75

FIGURE 18 - CODE REGISTER SEQUENCE DURING PULSE GENERATION 125

FIGURE 19 - CODE REGISTER SEQUENCE FOR 0-110 FEET BUILD-OUT 126

FIGURE 20 - BOUNDARY SCAN ARCHITECTURE 131

FIGURE 21 - TAP CONTROLLER FINITE STATE MACHINE 133

FIGURE 22 - INPUT OBSERVATION CELL (IN_CELL) 138

FIGURE 23 - OUTPUT CELL (OUT_CELL) 139

FIGURE 24 - BIDIRECTIONAL CELL (IO_CELL) 140

FIGURE 25 - LAYOUT OF OUTPUT ENABLE AND BIDIRECTIONAL CELLS 140

FIGURE 26 - B8ZS LINE CODE VIOLATION INSERTION 141

FIGURE 27 - HDB3 LINE CODE VIOLATION INSERTION 142

FIGURE 28 - AMI LINE CODE VIOLATION INSERTION 143

FIGURE 29 - MICROPROCESSOR INTERFACE READ TIMING 150

FIGURE 30 - MICROPROCESSOR INTERFACE WRITE TIMING 152

FIGURE 31 - XCLK INPUT TIMING FOR JITTER ATTENUATION 153

FIGURE 32 - TCLKI INPUT TIMING 154

FIGURE 33 - CLKO8X INPUT TIMING DIAGRAM (FIFO NOT IN TX PATH) ... 156

FIGURE 34 - XCLK INPUT TIMING DIAGRAM (FIFO NOT IN TX PATH) 157

FIGURE 35 - RCLKO OUTPUT TIMING DIAGRAM 158

FIGURE 36 - JTAG PORT INTERFACE TIMING 160

FIGURE 37 - ANALOG RECEIVE DATA INPUT TIMING DIAGRAM 161

LIST OF TABLES

TABLE 1 - 33

TABLE 2 - 35

TABLE 3 - 51

TABLE 4 - 90

TABLE 5 - TEST MODE REGISTER MEMORY MAP 113

TABLE 6 - 115

TABLE 7 - 115

TABLE 8 - INSTRUCTION REGISTER 116

TABLE 9 - BOUNDARY SCAN REGISTER 117

TABLE 10 - 122

TABLE 11 - 123

TABLE 12 - 124

TABLE 13 - 136

TABLE 14 -.QDSX ABSOLUTE MAXIMUM RATINGS 144

TABLE 15 - QDSX CAPACITANCE 145

TABLE 16 - QDSX D.C. CHARACTERISTICS 146

TABLE 17 - MICROPROCESSOR INTERFACE READ ACCESS (FIGURE 29) 149

TABLE 18 - MICROPROCESSOR INTERFACE WRITE ACCESS (FIGURE 30) 151

TABLE 19 - XCLK INPUT FOR JITTER ATTENUATION (FIGURE 31) 153

TABLE 20 - TCLKI INPUT TIMING (FIGURE 32) 154

TABLE 21 - CLKO8X INPUT TIMING (FIFO NOT IN TX PATH) (FIGURE 33) 156

TABLE 22 - XCLK INPUT TIMING (FIFO NOT IN TX PATH) (FIGURE 34) 157

TABLE 23 - RCLKO OUTPUT TIMING (FIGURE 35) 158

TABLE 24 - JTAG PORT INTERFACE TIMING (FIGURE 36) 159

TABLE 25 - ANALOG RECEIVE DATA INPUT TIMING (FIGURE 37) 161

TABLE 26 - QDSX ORDERING INFORMATION 163

TABLE 27 - QDSX THERMAL INFORMATION 163

1 FEATURES

- Integrates four duplex DSX-1 or CEPT E1 compatible line interface circuits in a single monolithic device. Line format is selected on a per-device basis.
- Provides clock recovery and line performance monitoring in the receivers.
- Provides jitter attenuation and programmable line build out in the transmitters.
- Utilizes digital phase-locked loops for receive and transmit clock derivation without the use of tuned circuits.
- Provides an integrated 8X clock multiplier for generation of required high-speed clocks in applications not requiring jitter attenuation.
- Optionally inserts Alarm Indication Signal (AIS) when loopback modes are enabled. AIS insertion may also be directly controlled via the microprocessor interface.
- Provides a generic microprocessor interface for initial configuration, ongoing control, and status monitoring.
- Generates an interrupt upon detection of any of various alarms, events, or changes in status. Identification of interrupt sources, masking of interrupt sources, and acknowledgment of interrupts is provided via internal registers.
- Provides optional hardware programmed mode which provides external configuration pins when microprocessor access is not available to the device.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Provides seamless interface to PM4344 TQUAD, PM6344 EQUAD, PM8313 D3MX, and PM7344 S/UNI-MPH.
- Low power CMOS technology, 1500 mW power dissipation processing all ones signals on all four quadrants.
- 128-pin (14mm x 20mm) PQFP package.

Each receiver section

- Slices incoming G.703 DSX-1 and CEPT E1 bipolar line signals into digital return-to-zero (RZ) pulses.
- Selectable slicer levels (DSX-1/CEPT E1) to provide improved SNR.

- Squelches RZ signals with pulse amplitudes below 140mV and 105mV for CEPT and T1, respectively.
- Typical minimum sensitivity of 50 mV at transformer primary with a 1:2 turns ratio transformer allows for terminating or bridged performance monitoring applications.
- Recovers a 1.544 MHz clock and DS-1 data or a 2.048 MHz clock and E1 data using a digital phase-locked loop to achieve high jitter accommodation.
- Accommodates up to 0.4 UI peak-to-peak, high frequency jitter to satisfy AT&T TR 62411 and ITU-T G.823.
- Optionally outputs either dual rail recovered line pulses or a single rail DS-1/E1 signal.
- Performs B8ZS or AMI decoding when processing a bipolar DS-1 signal and HDB3 or AMI decoding when processing a bipolar E1 signal.
- Detects line code violations (LCVs), B8ZS/HDB3 line code signatures, and 16, 8, or 4 successive zeros.
- Accumulates up to 4095 line code violations (LCVs), for performance monitoring purposes, over accumulation intervals defined by the period between software write accesses to the LCV register.
- Detects loss of signal (LOS), which is defined as 10, 15, 31, 63, or 175 successive zeros.
- Detects both programmable inband loopback activate and deactivate code sequences received in the DS-1 data stream when they are present for 5 seconds. Optionally, enters loopback mode automatically on detection of an inband loopback code.
- Detects any pair of arbitrary inband codes from three to eight bits in length.
- The inband code detection algorithm operates in the presence of a 10^{-2} bit error rate.
- Programmable to detect CSU (Channel Service Unit), network, and far-end loopback codes.
- Optionally allows jitter attenuation of recovered clock and data, using a 2 X 48 bit FIFO.
- Optionally inserts unframed inband code sequences in place of recovered data.

- Detects unframed 2^{15}-1 test sequences as defined in ITU-T O.151 and accumulates bit errors detected using this pseudo-random pattern.
- Optionally inserts unframed 2^{15}-1 test sequences in place of recovered data.

Each transmitter section

- Generates DSX-1 and CEPT E1 compatible pulses with programmable pulse shape using an external 1:1.36 turns ratio transformer.
- Accommodates standard cable types such as ABAM, PIC, and Coaxial.
- Provides an integrated analog pulse driver performance monitor which can provide an interrupt upon detection of failure.
- Allows bipolar violation (BPV) transparent operation for error restoring regenerator applications.
- Allows bipolar violation (BPV) insertion for diagnostic testing purposes.
- Supports all ones transmission for alarm indication signal (AIS) generation.
- Provides a digital phase-locked loop for generation of jitter reduced transmit output timing. The DPLL utilizes a 37.056 MHz master clock for DSX-1 or a 49.152 MHz master clock for CEPT E1 applications.
- Digital phase-locked loop locks 1.544 MHz or 2.048 MHz output timing to the average frequency of the 1.544 MHz or 2.048 MHz jittered transmit input clock.
- Provides a 2 x 48 bit FIFO for jitter attenuation in the transmit path.
- Provides up to 55 dB of jitter attenuation to satisfy AT&T TR 62411, ITU-T G.737, G.738, G.739, and G.742.
- Provides FIFO overrun and underrun indicators.
- Inhibits FIFO overrun and underrun for excessive jitter amplitudes.
- Supports transmission of a programmable unframed inband loopback code sequence.
- Programmable to transmit repetitions of any arbitrary code from three to eight bits in length.
- Accepts either dual rail or single rail DS-1/E1 signals.
- Performs B8ZS or AMI encoding when processing a single rail DS-1 signal and HDB3 or AMI encoding when processing a single rail E1 signal.

- Optionally detects inband code sequences in DS-1 transmit streams.
- Optionally inserts unframed 2^{15}-1 test sequences in place of input transmit data.
- Optionally detects unframed 2^{15}-1 test sequences in the input transmit data.

2 APPLICATIONS

- T1 or E1 ATM interfaces
- Electronic DSX-1/CEPT E1 Cross-connects
- Digital Access and Cross-connect Systems (DACS)
- Multiplexers
- Channel Service Units (CSUs)
- DSX-1/CEPT E1 Repeaters
- Test Equipment

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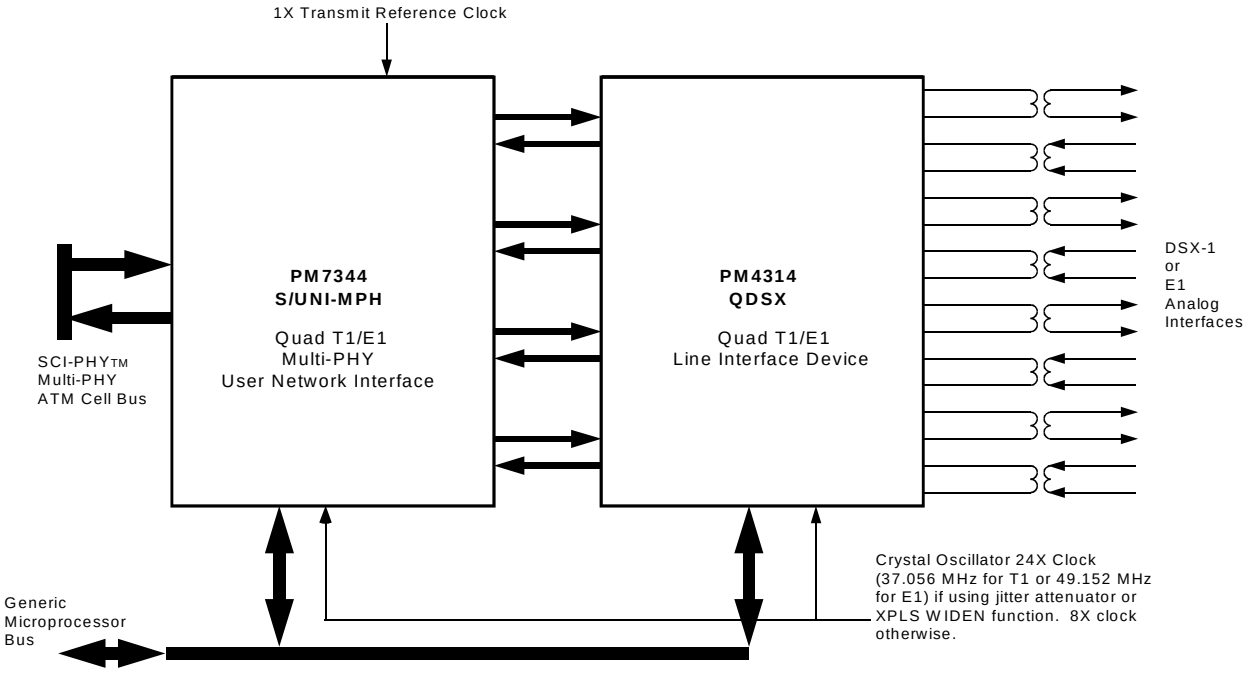
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4 APPLICATION EXAMPLES

Figure 1 - Example 1. T1 or E1 ATM Interfaces



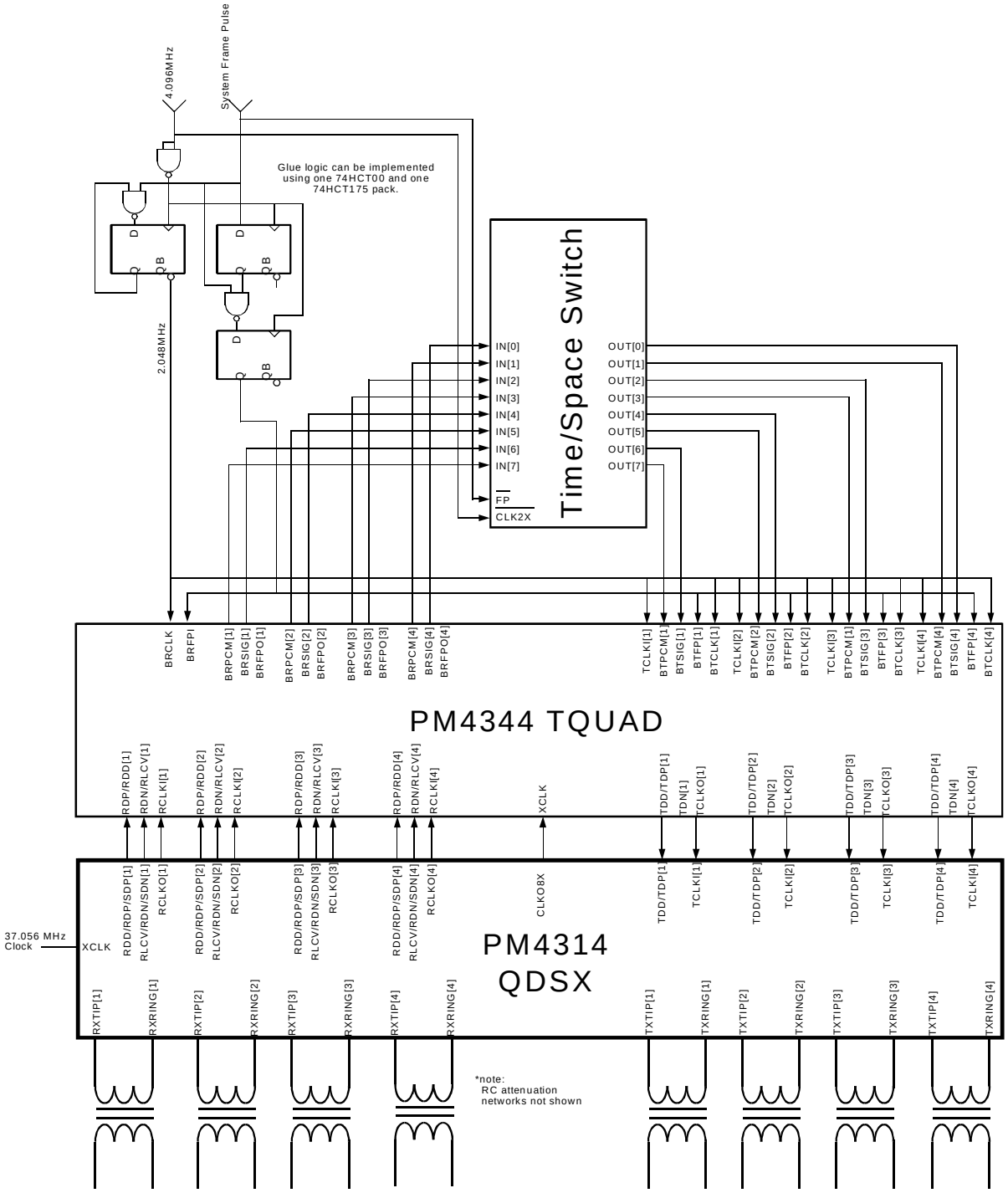
Example 1 shows the PM4314 QDSX used with the PM7344 S/UNI-MPH to implement a quad T1/E1 UNI where the DS1 or E1 signals are presented on DSX-1 or E1 electrical interfaces.

In this example, the DSX-1 or E1 line interface functions are provided by the QDSX and the DS-1 or E1 framing functions are provided by the S/UNI-MPH. The S/UNI-MPH also provides the ATM cell processing functions associated with the PHY layer, including the implementation of a SCI-PHY multi-PHY interface to the ATM layer device(s). The combination of the QDSX device with the S/UNI-MPH allows both ANSI/ITU compliant DSX-1/E1 analog signals and ATM Forum UNI 3.1 and ITU G.804 compliant DS1/E1 digital signals to be processed.

Jitter attenuation by both the QDSX and the S/UNI-MPH can be performed by supplying a 24X reference clock to the devices. If jitter attenuation is to be executed by the S/UNI-MPH only, then an 8X reference clock is required by the QDSX and a 24X reference clock is required by the S/UNI-MPH. If jitter attenuation is to be executed by the QDSX, then a 24X reference clock must be

supplied to it and an 8X reference clock may be supplied to the S/UNI-MPH. If jitter attenuation is not required by either device, then an 8X reference clock may be supplied to both devices.

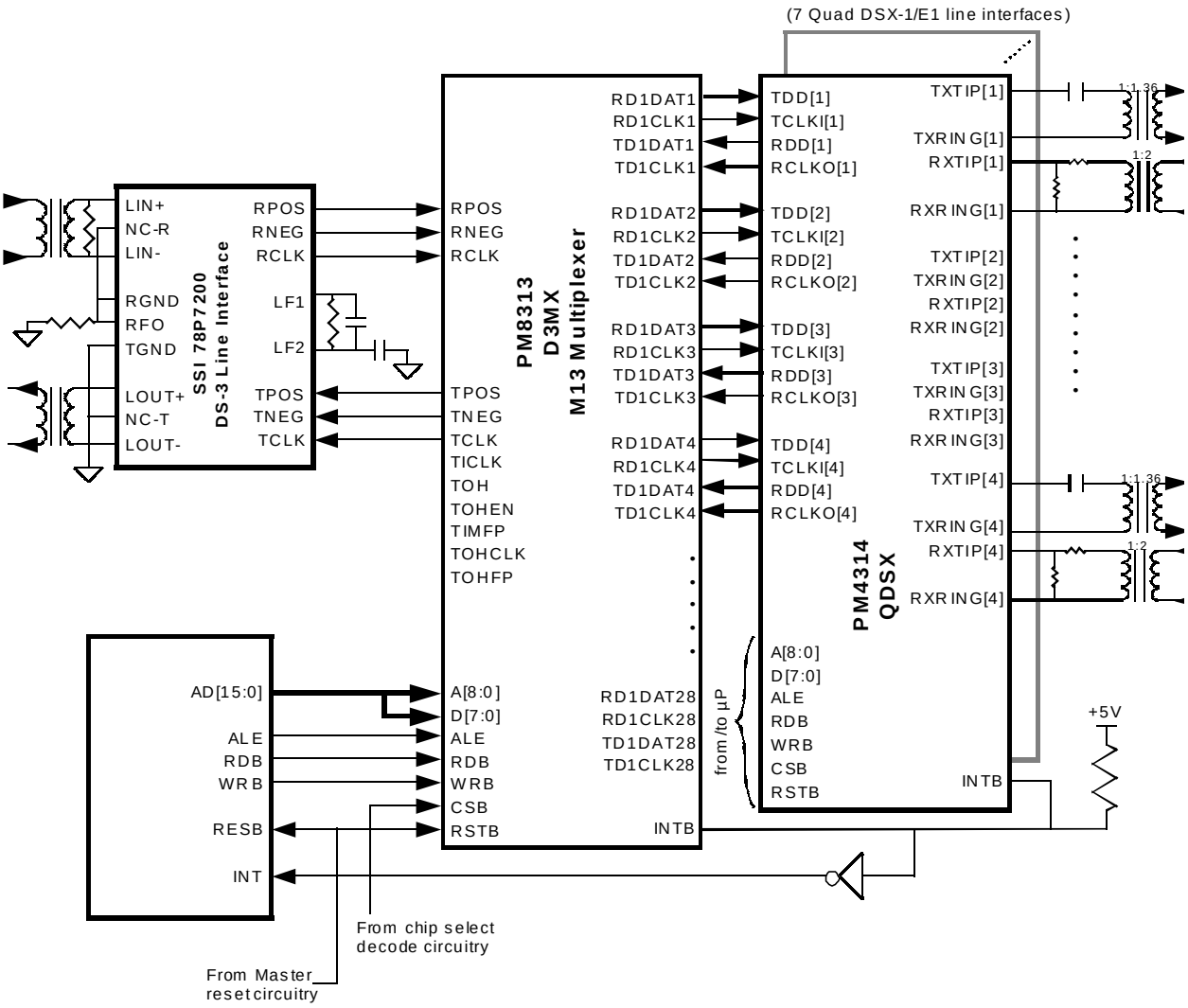
Figure 2 - Example 2. DSX-1 Digital Access Cross Connects (DACs)



Example 2 shows a DSX 1/0 Cross-Connect using a PM4314 QDSX, a PM4344 TQUAD, and a Digital Time/Space Switch to implement a simple 1/0 cross-connect. An alternate architecture could use two Digital Time/Space Switches, one as a voice switch and the other as a signaling switch, and 2 TQUADs to cross-connect eight T1s. (Note: a true implementation would require redundancy in the switch core.)

In this example, the TQUAD is programmed to receive and generate the same framing format, using the 2.048 MHz backplane data rate. The "system frame pulse" signal is stretched through the two D-FF into a pulse of 488ns duration, which is used to frame align the data out of each framer through the elastic store and to provide frame alignment indication to the transmitters. The raw system frame pulse signal is used to indicate frame alignment synchronization to the Digital Time/Space Switch. Another D-FF is configured as a toggle to generate a 2.048MHz clock from the system 4.096MHz clock source, synchronized to the system frame pulse. The TQUAD is configured to accept and source unipolar signal from and to the QDSX. As shown, the jitter attenuation is performed in the QDSX and is disabled in the TQUAD.

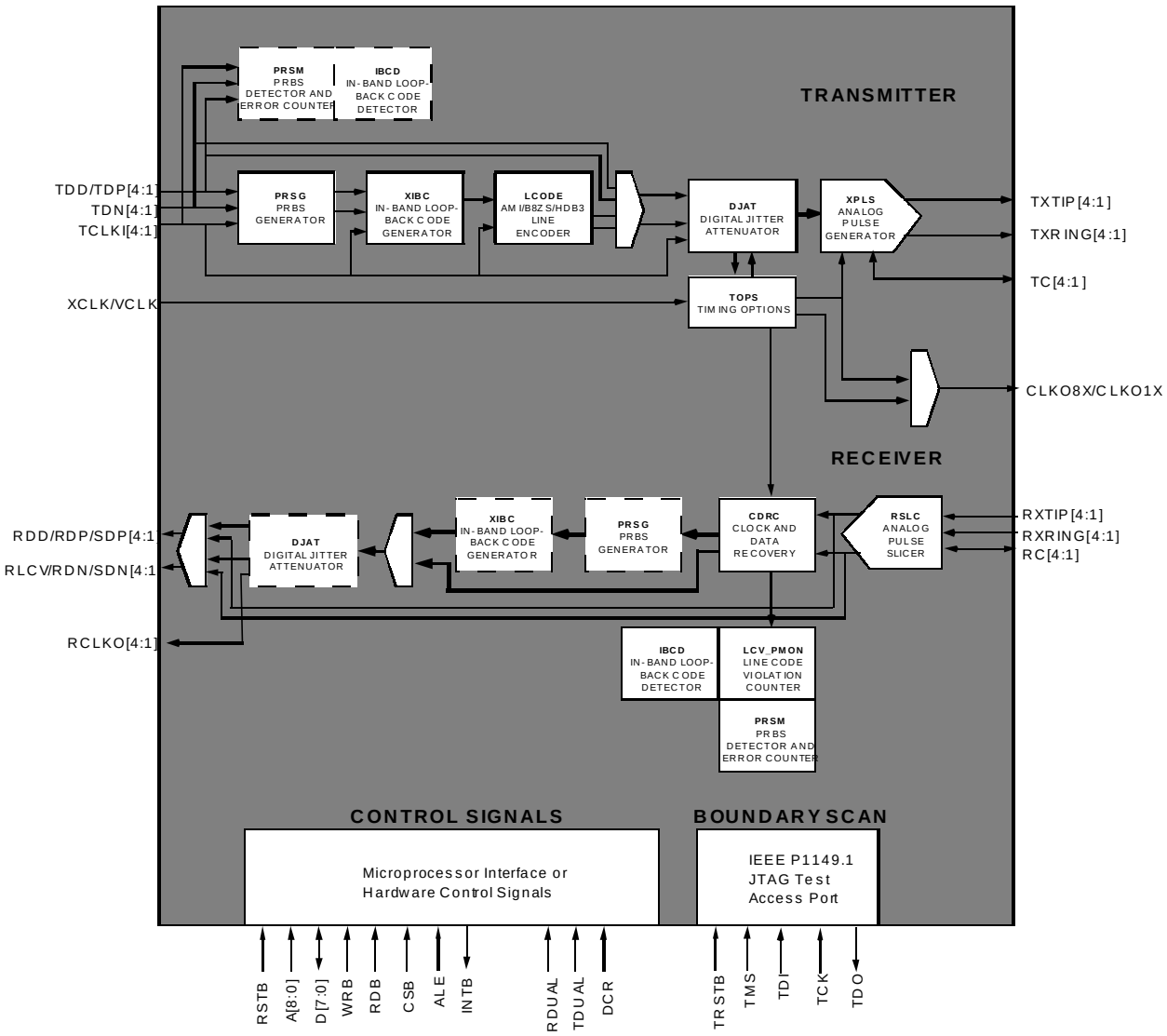
Figure 3 - Example 3. Multiplexers (M13)



Example 3 shows the use of the PM4314 QDSX with the PM8313 D3MX in an M13 Multiplexer/Demultiplexer application. Use of the SSI LIU as illustrated requires that TICLK of the D3MX has a duty cycle of 45% min., 55% max. or better (e.g.. using a Connor Winfield S65T3 reference oscillator).

5 BLOCK DIAGRAM

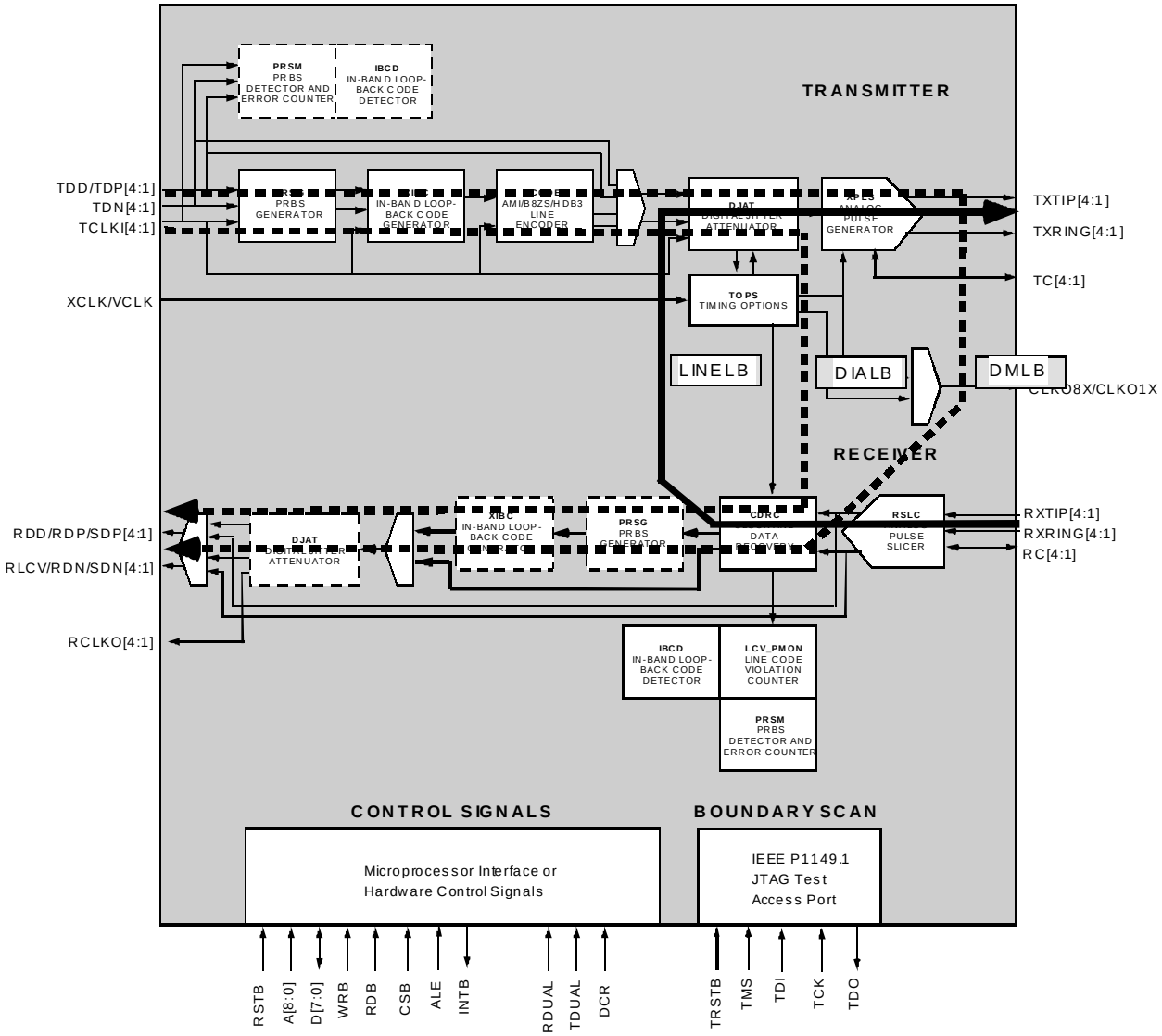
Figure 4 - Normal Operating Mode



Note:

Dashed boxes show optional placement of blocks. Default placement of the block is shown in solid boxes.

Figure 5 - Loopback Modes



Note:

Dashed boxes show optional placement of blocks. Default placement of the block is shown in solid boxes.

6 DESCRIPTION

The PM4314 QDSX Quad T1/E1 Line Interface Device is a monolithic integrated circuit that supports DSX-1 and CEPT E1 compatible transmit and receive interfaces for four 1.544 Mbit/s or 2.048 Mbit/s data streams.

In the incoming direction, the DSX-1/E1 signals for each quadrant of the QDSX are first processed by a receive data slicer. The receive data slicer converts the line signal received via a coupling transformer to dual rail RZ digital pulses. Adaptation for attenuation is achieved using an integral peak detector that sets the slicing levels. Through use of passive external attenuation circuitry, either terminated or bridge monitored DSX-1/E1 signal levels can be accommodated. The low signal level condition or signal squelch may be enabled to generate interrupts. Clock and data are recovered from the dual rail RZ digital pulses using a digital phase-locked loop that provides excellent high frequency jitter accommodation. The recovered data is decoded using B8ZS, HDB3, or AMI line code rules and is presented either as a DS-1/E1 stream or presented in an undecoded dual rail NRZ format. Loss of signal and line code violations are detected as well as 8 successive zeros/4 successive zeros, and the B8ZS/HDB3 signature. The presence of programmable inband loopback codes is also detected. These various events or changes in status may be enabled to generate interrupts. Additionally, line code violations are indicated on outputs.

In the outgoing direction, each quadrant of the QDSX may accept either a DS-1/E1 stream to be encoded using B8ZS, HDB3, or AMI line code rules, or it may accept pre-encoded data in dual rail NRZ format. Jitter attenuation is provided by passing outgoing data through a FIFO. A low jitter clock is generated by an integral digital phase-locked loop and is used to read data from the FIFO. FIFO overrun or underrun may be enabled to generate interrupts. Alarm indication signal (all ones) may be substituted for the FIFO data. The digital data is converted to high drive, dual rail RZ pulses that drive the DSX-1/E1 interface through a coupling transformer. The shape of the pulses is user programmable to ensure that the DSX-1/E1 pulse template is met after the signal is passed through different cable lengths or types. Driver performance monitoring is provided and may be enabled to generate interrupts upon driver failure.

The jitter attenuation function can optionally be moved to the receive side. The recovered clock and data is passed through the jitter attenuator before being presented at the digital receive outputs.

Internal high speed timing for all quadrants of the QDSX is provided by a common 37.056 MHz or 49.152 MHz master clock. This master clock rate is required for applications where QDSX provides jitter attenuation. For applications where QDSX is not required to attenuate jitter, a 12.352 MHz or 16.384 MHz clock may be used as the master clock and used directly as the internal 8X high speed clock.

Diagnostic loopback is provided and the loopback may be invoked past the analog transmit outputs using the driver performance monitors or invoked prior to the conversion to analog. Line loopback with jitter attenuation is provided and may be enabled for automatic operation based on detected inband loopback codes.

The QDSX detects framed or unframed inband loopback code sequences from the received input pulses. Any arbitrary code from three to eight bits in length can be declared to be the activate and deactivate codes by writing to configuration registers. The inband loopback code detector can optionally be moved to the transmit side where it detects inband loopback codes in the unipolar input transmit data stream. For framed inband loopback code sequences, it is expected that the framing bit overwrites the inband loopback code bit.

The QDSX may insert unframed inband loopback code sequences into the transmitted PCM data stream. These codes consist of continuous repetitions of specific bit sequences. Any arbitrary code from three to eight bits in length is programmable by writing to configuration registers. This unframed inband loopback code insertion may optionally be switched to the receive side where it overwrites the data from the slicer.

The QDSX may insert an unframed 2^{15}-1 O.151 compatible pseudo-random bit sequence into the transmitted PCM data stream. Optionally, the PRBS insertion may be switched to the receive side where it overwrites the data from the slicer.

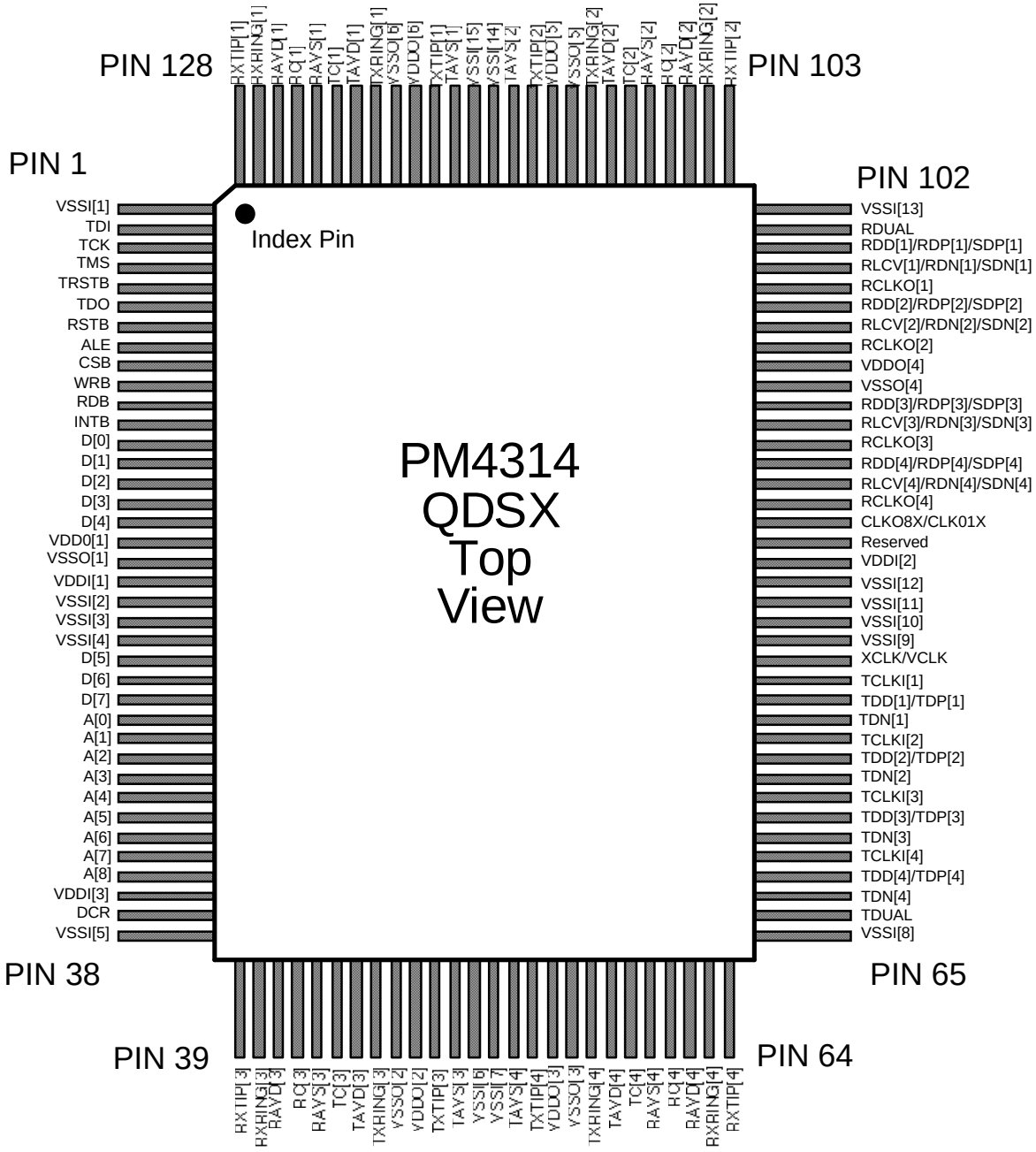
The QDSX detects an unframed 2^{15}-1 O.151 compatible pseudo-random bit sequence input to the receive slicer. This PRBS detector can operate in the presence of a 10^{-2} bit error rate. Bit errors are detected and recorded. The PRBS detector can optionally be switched to the transmit side where it can detect unframed PRBS data from the unipolar input transmit data stream.

The QDSX operates in conjunction with external line coupling transformers, resistors, and capacitors. An external crystal may be used for high speed timing

generation. The QDSX is configured, controlled, and monitored using registers that are accessed via a generic microprocessor interface.

7 PIN DIAGRAM

The QDSX is packaged in a 128-pin plastic QFP package having a body size of 1mm by 20mm and a pin pitch of 0.5 mm.



8 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
TXTIP[4] TXTIP[3] TXTIP[2] TXTIP[1]	Output	54 49 113 118	Transmit Bipolar Tip (TXTIP[4:1]). The TXTIP[4:1] outputs are the transmit analog positive pulses. These analog outputs drive an AC signal through an external matching transformer. They must be connected to the positive lead of the transformer primary. An analog Transmit Monitor Positive point is internally bonded to each of these outputs and is used to monitor the positive pulses on each transmit line.
TXRING[4] TXRING[3] TXRING[2] TXRING[1]	Output	57 46 110 121	Transmit Bipolar Ring (TXRING[4:1]). The TXRING[4:1] outputs are the transmit analog negative pulses. These analog outputs drive an AC signal through an external matching transformer. They must be connected to the negative lead of the transformer primary. An analog Transmit Monitor Negative point is internally bonded to each of these outputs and is used to monitor the negative pulses on each transmit line.
TC[4] TC[3] TC[2] TC[1]	I/O	59 44 108 123	Transmit Reference Decoupling Capacitor (TC[4:1]). These analog bidirectionals provide decoupling for an internal reference generator. They must be connected to an external decoupling capacitor to the corresponding TAVD[4:1].

Pin Name	Type	Pin No.	Function
TDD[4] TDD[3] TDD[2] TDD[1]	Input	68 71 74 77	Transmit Data (TDD[4:1]). When in single-rail mode, these inputs are the NRZ data signals to be transmitted. These inputs can be configured to be active high or active low. These inputs can be sampled on either the rising or falling edges of the corresponding TCLKI[4:1].
TDP[4] TDP[3] TDP[2] TDP[1]	Input		Transmit Positive Data (TDP[4:1]). When in dual-rail mode, these inputs are the NRZ positive data signals to be transmitted. These inputs can be sampled on either the rising or falling edges of the corresponding TCLKI[4:1].
TDN[4] TDN[3] TDN[2] TDN[1]	Input	67 70 73 76	Transmit Negative Data (TDN[4:1]). When in dual-rail mode, these inputs are the NRZ negative data signals to be transmitted. These inputs can be sampled on either the rising or falling edges of the corresponding TCLKI[4:1]. These input pins are ignored if the device is configured for single-rail (unipolar) transmit mode.
TCLKI[4] TCLKI[3] TCLKI[2] TCLKI[1]	Input	69 72 75 78	Transmit Clock (TCLKI[4:1]). This clock should be 1.544 MHz for DS1 or 2.048 MHz for E1 data streams and is used to sample the corresponding TDP/TDD[4:1] and TDN[4:1] signals.
RXTIP[4] RXTIP[3] RXTIP[2] RXTIP[1]	Input	64 39 103 128	Receive Bipolar Tip (RXTIP[4:1]). The RXTIP[4:1] inputs are the receive analog positive pulses. They must be connected to the positive lead of the transformer secondary through a passive attenuation network.
RXRING[4] RXRING[3] RXRING[2] RXRING[1]	I/O	63 40 104 127	Receive Bipolar Ring (RXRING[4:1]). The RXRING[4:1] bidirectional pins provide DC bias to an external isolation transformer. They must be connected to the negative lead of the transformer secondary and to a decoupling capacitor to RAVS[4:1].

Pin Name	Type	Pin No.	Function
RC[4] RC[3] RC[2] RC[1]	I/O	61 42 106 125	Receive Peak Hold R-C Network (RC[4:1]). The RC[4:1] analog bidirectional pins must be connected to an external parallel resistor/capacitor network to RAVS[4:1]. This network is necessary to the operation of the internal peak detector that tracks the incoming signal level.
RDD[4] RDD[3] RDD[2] RDD[1]	Output	89 92 97 100	Receive Digital Data (RDD[4:1]). When configured for unipolar outputs, the RDD[4:1] NRZ outputs contain the sampled DS-1 or E1 data which has been decoded by AMI, B8ZS, or HDB3 line code rules. RDD[4:1] outputs can be updated on either the falling or rising RCLKO[4:1] edge.
RDP[4] RDP[3] RDP[2] RDP[1]	Output		Receive Digital Positive Pulse (RDP[4:1]). When configured for bipolar outputs, the RDP[4:1] NRZ outputs contain sampled bipolar positive pulses. RDP[4:1] outputs can be updated on either the falling or rising RCLKO[4:1] edge.
SDP[4] SDP[3] SDP[2] SDP[1]	Output		Sliced Positive Line Pulse (SDP[4:1]). A positive pulse on the SDP[4:1] outputs corresponds to the sampled positive pulse excursion on the RXTIP[4:1] input.

Pin Name	Type	Pin No.	Function
RLCV[4] RLCV[3] RLCV[2] RLCV[1]	Output	88 91 96 99	Receive Line Code Violation Indication (RLCV[4:1]). When configured for unipolar outputs, the RLCV[4:1] NRZ outputs pulse whenever a line code violation or excess zeroes condition is detected. RDP[4:1] outputs can be updated on either the falling or rising RCLKO[4:1] edge.
RDN[4] RDN[3] RDN[2] RDN[1]	Output		Receive Digital Positive Pulse (RDN[4:1]). When configured for bipolar outputs, the RDN[4:1] NRZ outputs contain sampled bipolar negative pulses. RDN[4:1] outputs can be updated on either the falling or rising RCLKO[4:1] edge.
SDN[4] SDN[3] SDN[2] SDN[1]	Output		Sliced Negative Line Pulse (SDN[4:1]). A positive pulse on the SDN[4:1] outputs corresponds to the sampled negative pulse excursion on the RXTIP[4:1] input.
RCLKO[4] RCLKO[3] RCLKO[2] RCLKO[1]	Output	87 90 95 98	Recovered Clock Output (RCLKO[4:1]). RCLKO[4:1] is the clock recovered from the RXTIP[4:1] and RXRING[4:1] input signals. RCLKO[4:1] are 2mA output pads. Care must be taken in board layouts to guarantee the integrity of the clock signals.
XCLK/	Input	79	Crystal Clock Input (XCLK). This signal supplies the timing reference for the high-speed clocks required by many portions of the QDSX. When jitter attenuation is required, XCLK is nominally a 24X clock (37.056 MHz for T1, 49.152 MHz for E1). When jitter attenuation is not required, XCLK can be driven by an 8X clock (12.352 MHz for T1, 16.384 MHz for E1).
VCLK			Vector Clock (VCLK). The VCLK signal is used during QDSX production test to verify internal functionality.

Pin Name	Type	Pin No.	Function
CLKO8X/	Output	86	8X Clock Output (CLKO8X). This output is the internal 8X high-speed clock derived from the digital jitter attenuator, or derived by dividing down the 24X XCLK input. It is used as the reference clock to generate the transmit analog pulse template. The CLKO8X signal is generated from Quadrant 1.
CLKO1X	Output		1X Clock Output (CLKO1X). When an 8X clock is provided on XCLK, this is the internal 8X clock divided by 8. This output can be used to synchronously clock in data on TDP[4:1]/TDD[4:1] and TDN[4:1] by connecting it to TCLKI[4:1].
DCR	Input	37	Disable Clock Recovery Input (DCR). When set high, the DCR input will disable clock recovery in the QDSX and enable the SDP[4:1] and SDN[4:1] sliced line pulse outputs. This input is logically "ORed" with the DCR register bits.
TDUAL	Input	66	Transmit Dual-Rail Input Select (TDUAL). This input selects whether the QDSX expects single-rail or dual-rail input transmit data. The TDUAL input is logically "ORed" with the TDUAL register bits. When TDUAL is set high, the TDP[4:1] and TDN[4:1] inputs are enabled. When both the TDUAL input pin and register bits are set low, then the TDD[4:1] inputs are enabled and the TDN[4:1] inputs are ignored.

Pin Name	Type	Pin No.	Function
RDUAL	Input	101	Receive Dual-Rail Output Select (RDUAL). This input selects whether the QDSX generates single-rail or dual-rail outputs from its receiver section. The RDUAL input is logically "ORed" with the RDUAL register bits. When RDUAL is set high, the RDP[4:1] and RDN[4:1] outputs are enabled. When both the RDUAL input pin and register bits are set low, then line decoding is performed on the receive slicer outputs and the RDD[4:1] and RLCV[4:1] outputs are enabled. The state of the DCR input pin or the DCR register bits takes precedence over the RDUAL state.
CSB	Input	9	Active low Chip Select (CSB). This signal must be low to enable QDSX register accesses. CSB must go high at least once after a powerup to clear internal test modes. If CSB is not used, then it should be tied to an inverted version of RSTB, in which case RDB and WRB determine register access.
WRB	Input	10	Active low Write Strobe (WRB). This signal is pulsed low to enable a QDSX register write access. The D[7:0] bus is clocked into the addressed register on the rising edge of WRB while CSB is low.
RDB	Input		Active low Read Enable (RDB). This signal is pulsed low to enable a QDSX register read access. The QDSX drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.

Pin Name	Type	Pin No.	Function
A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	35 34 33 32 31 30 29 28 27	Address Bus (A[8:0]). This bus selects specific registers during QDSX register accesses.
ALE	Input	8	Address Latch Enable (ALE). This signal latches the address bus contents, A[8:0], when low, allowing the QDSX to be interfaced to a multiplexed address/data bus. When ALE is high, the address latches are transparent. ALE has an integral pull-up resistor.
INTB	Output	12	Active low Open-Drain Interrupt (INTB). This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active unmasked interrupt sources are acknowledged at their source.

Pin Name	Type	Pin No.	Function
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	26 25 24 17 16 15 14 13	Bidirectional Data Bus (D[7:0]). This bus is used during QDSX read and write accesses.
RSTB	Input	7	Active low Reset (RSTB). This signal is set low to asynchronously reset the QDSX. RSTB is a Schmitt-trigger input with an integral pull-up resistor.
TCK	Input	3	Test Clock (TCK). This signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	4	Test Mode Select (TMS). This signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	2	Test Data Input (TDI). This signal carries test data into the QDSX via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate Output	6	Test Data Output (TDO). This signal carries test data out of the QDSX via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output which is inactive except when scanning of data is in progress.

Pin Name	Type	Pin No.	Function
TRSTB	Input	5	Active low Test Reset (TRSTB). This signal provides an asynchronous QDSX test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. When not being used, TRSTB should be tied to RSTB.
VDDO[6] VDDO[5] VDDO[4] VDDO[3] VDDO[2] VDDO[1]	Power	119 112 94 55 48 18	Pad Ring Power Pins (VDDO[6:1]). These pins must be connected to a common well decoupled +5V DC power supply together with the VDDI[3:1], TAVD[4:1], and RAVD[4:1] pins. Care must be taken to avoid coupling noise between these pins.
VDDI[3] VDDI[2] VDDI[1]	Power	36 84 20	Core Power Pins (VDDI[3:1]). These pins must be connected to a common well decoupled +5V DC power supply together with the VDDO[6:1], TAVD[4:1], and RAVD[4:1] pins. Care must be taken to avoid coupling noise between these pins.
VSSO[6] VSSO[5] VSSO[4] VSSO[3] VSSO[2] VSSO[1]	Ground	120 111 93 56 47 19	Pad Ring Ground Pins (VSSO[6:1]). These pins must be connected to a common ground together with the VSSI[15:1], TAVS[4:1], and RAVS[4:1] pins. Care must be taken to avoid coupling noise between these pins.

Pin Name	Type	Pin No.	Function
VSSI[15] VSSI[14] VSSI[13] VSSI[12] VSSI[11] VSSI[10] VSSI[9] VSSI[8] VSSI[7] VSSI[6] VSSI[5] VSSI[4] VSSI[3] VSSI[2] VSSI[1]	Ground	116 115 102 83 82 81 80 65 52 51 38 23 22 21 1	Core Ground Pins (VSSI[15:1]). These pins must be connected to a common ground together with the VSSO[6:1], TAVS[4:1], and RAVS[4:1]pins. Care must be taken to avoid coupling noise between these pins. These pins also act as thermal-dissipation grounds, and as such should be thermally well-connected to a ground plane.
TAVD[4] TAVD[3] TAVD[2] TAVD[1]	TX Analog Power	58 45 109 122	Transmit Analog Power Pins (TAVD[4:1]). These pins provide the +5 V supply to the transmit analog line interfaces. The transmit analog line interface remains in a low power consumption state after reset until enabled. TAVD[4:1] must be connected to a common well decoupled +5 V DC power supply together with the VDDO[6:1], VDDI[3:1], and RAVD[4:1] pins. Care must be taken to avoid coupling noise between these pins.
TAVS[4] TAVS[3] TAVS[2] TAVS[1]	TX Analog Ground	53 50 114 117	Transmit Analog Ground Pins (TAVS[4:1]). These pins provide the ground supply to the transmit analog line interface. TAVS[4:1] must be connected to a common ground together with the VSSO[6:1], VSSI[15:1], and RAVS[4:1] pins. Care must be taken to avoid coupling noise between these pins.

Pin Name	Type	Pin No.	Function
RAVD[4] RAVD[3] RAVD[2] RAVD[1]	RX Analog Power	62 41 105 126	Receive Analog Power Pins (RAVD[4:1]). These pins provide the +5 V DC power supply to the receive analog line interface. RAVD[4:1] must be connected to a common well decoupled +5 V DC power supply together with the VDDO[6:1], VDDI[3:1], and TAVD[4:1] pins. Care must be taken to avoid coupling noise between these pins.
RAVS[4] RAVS[3] RAVS[2] RAVS[1]	RX Analog Ground	60 43 107 124	Receive Analog Ground Pins (RAVS[4:1]). These pins provide the ground supply to the receive analog line interface. RAVS[4:1] must be connected to a common ground together with the VSSO[6:1], VSSI[15:1], and TAVS[4:1] pins. Care must be taken to avoid coupling noise between these pins.

Notes on Pin Description:

1. VDDI[3:1] and VSSI[15:1] are the +5 V and ground connections, respectively, for the core circuitry of the device. VDDO[6:1] and VSSO[6:1] are the +5 V and ground connections, respectively, for the pad ring circuitry of the device. TAVD[4:1] and TAVS[4:1] are the +5 V and ground connections, respectively, for the transmit analog circuitry of the device. RAVD[4:1] and RAVS[4:1] are the
   +5 V and ground connections, respectively, for the receive analog circuitry of the device. These power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate. There is no low impedance connection within the PM4314 QDSX between the core, pad ring, transmit analog, and receive analog supply rails. Failure to properly make these connections may result in improper operation or damage to the device. Care must be taken to avoid coupling of noise into the transmit and receive analog supply rails.

2. Inputs RSTB, ALE, TMS, TDI, and TRSTB have integral pull-up resistors.

3. All QDSX inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.

4. All QDSX digital outputs and bidirectionals have 2 mA drive capability. The data bus outputs, D[7:0], and CLKO8X have 4 mA drive capability. For board layouts, care should be maken with the 2mA drive RCLKO[4:1] signals to guarantee clock signal integrity.

5. The recommended power supply sequencing is as follows:

   5.1 VDDI[3:1] power must be supplied either before VDDO[6:1] or simultaneously with VDDO[6:1]. Connection of VDDI[3:1] and VDDO[6:1] to a common VDD power plane is recommended.

   5.2 The VDDI[3:1] and VDDO[6:1] power must be applied before input pins are driven or the input current per pin must be limited to less than 20 mA.

   5.3 Analog power supplies must be applied after both VDDI[3:1] and VDDO[6:1] have been applied or the they must be current limited to the maximum latchup current specification. (100 mA). In operation the differential voltage measured between TAVD[4:1] and RAVD[4:1] supplies and VDDI[3:1] and VDDO[6:1] must be less than 0.5 volt. The relative power sequencing of TAVD[4:1] and RAVD[4:1] power supplies is not important.

   5.4 Power down the device in the reverse sequence.

9 FUNCTIONAL DESCRIPTION

9.1 Analog Pulse Slicer (RSLC)

The Analog T1/E1 Pulse Slicer function is provided by the RSLC block. The Receive Data Slicer (RSLC) block provides the first stage of signal conditioning for a G.703 1544kbit/s (DSX-1) or 2048 kbit/s (E1) serial data stream by converting bipolar line signals to dual rail RZ pulses. Before an RZ output pulse is generated by the RSLC block, bipolar input signals must rise to 50% (for E1) or 67% (for DSX-1) of their peak amplitude. This level is referred to as the slicing level. The threshold criteria insures accurate pulse or mark recognition in the presence of noise.

The RSLC block relies on an external network for compliance to the DSX-1 and E1 input port specifications. The RSLC block is configured via an off-chip attenuator pad to operate in one of four modes: DSX-1 normal mode, DSX-1 bridging mode, G.703 120 Ω twisted pair, or G.703 75 Ω coax.

According to G.703, the amplitude of a DSX-1 normal mode received pulse at the 1:2 line-coupling transformer's primary should be in the range from 3.6V to 1.2V (depending on the length of the cable from the signal source). In this mode, the QDSX can receive signal levels down to a typical squelching level of 227mV, leaving a 14.5dB margin between the minimum expected signal level and the typical minimum receivable signal level.

In DSX-1 bridging mode, the QDSX is connected to a monitor jack which bridges across the line and attenuates the signal levels by 20 dB, so the expected pulse amplitude at the 1:2 line-coupling transformer's primary should be in the range from 360mV to 120mV (depending on the length of the cable from the signal source). In this mode, the QDSX can receive signal levels down to a squelching level of 50mV, leaving 7.6 dB margin between the minimum expected signal level and the typical minimum receivable signal level.

In 120Ω E1 mode, the amplitude of a received pulse at the 1:2 line-coupling transformer's primary can be in the range from 3.3V to 1.4V (depending on the length of the cable from the signal source). In this mode, the QDSX can receive signal levels down to a squelching level of 276mV, which means that there is 14.1 dB margin between the minimum expected signal level and the typcial minimum receivable signal level.

In 75Ω E1 mode, the amplitude of a received pulse at the 1:2 line-coupling transformer's primary can be in the range from 2.6V to 1.1V (depending on the length of the cable from the signal source). In this mode, the QDSX can receive signal levels down to a squelching level of 220mV which means that there is 14.0 dB margin between the minimum expected signal level and the minimum receivable signal level in the worst case.

The RSLC block provides a squelching circuit, which indicates an alarm when input pulses are below the squelching level threshold. In this state, data is not sliced, which prevents the detection of noise on an idle transmission line. The SQ status bit in the RSLC Interrupt Enable/Status registers (031H, 071H, 0B1H, and 0F1H) goes high whenever the RSLC block is squelching the input signal. The RSLC can be configured to generate an interrupt whenever the SQ status bit changes state.

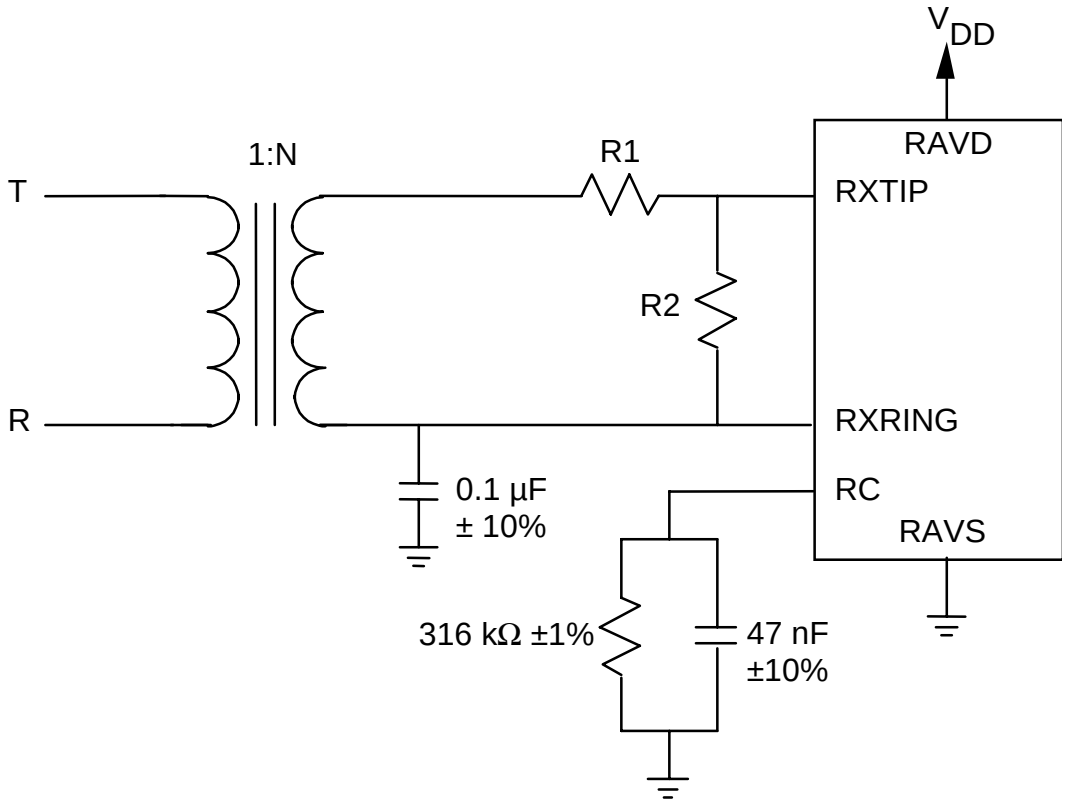
The off-chip attenuator pad network is shown in Figure 6 and the network values below are recommended for the specified applications:

Table 1 -

Signal Type		**Turns Ratio (N ± 5%)**	**R1 (Ω ± 1%)**	**R2 (Ω ± 1%)**	**Squelch Level at Primary (mV Typical)**
CEPT E1	Zo=120Ω	2	357	121	276
	Zo=75Ω	2	205	95.3	220
DSX-1	Normal	2	309	93	227
	Bridging	2	0	402	50

Tight tolerances are required on the resistors and turns ratio to meet the return loss specification.

Figure 6 - External Analog Receive Interface Circuit



Notes:

1. All capacitors ceramic
2. Some transformer manufacturers produce a dual part containing both the 1:2 & 1:1.36 transformers required for the receive and transmit interfaces, respectively.

The transformer used should be designed for use in T1/CEPT/ISDN-PRI applications. Many manufacturers have standard products for these applications. Typical characteristics of a suitable transformer are given in the following table.

Table 2 -

Turns Ratio (PRI:SEC)	OCL (mH min.)	$C_{w/w}$ (pF max.)	L_L (µH max.)	DCR pri. (Ω max.)	DCR sec. (Ω max.)
1:2	1.20	35	0.80	0.80	1.2

where OCL is the open-circuit inductance,

$C_{w/w}$ is the inter-winding capacitance,

L_L is the leakage inductance, and

DCR is the DC resistance.

PMC-Sierra has verified the operation of the RSLC functional block with the following transformers:

- Pulse Engineering PE64931 (1:1:1) and PE64952 (1:2CT)
- BH Electronics 500-1775 (1:1:1) and 500-1777 (1:2CT)

Many manufacturers produce dual transformers containing the 1:2 CT and 1:1.36 transformers necessary for the receiver and transmitter circuits. PMC-Sierra has verified the operation of XPLS and RSLC with the following dual parts:

- Pulse Engineering PE64952
- Pulse Engineering PE65774 (for extended temperature range)
- BH Electronics500-1777

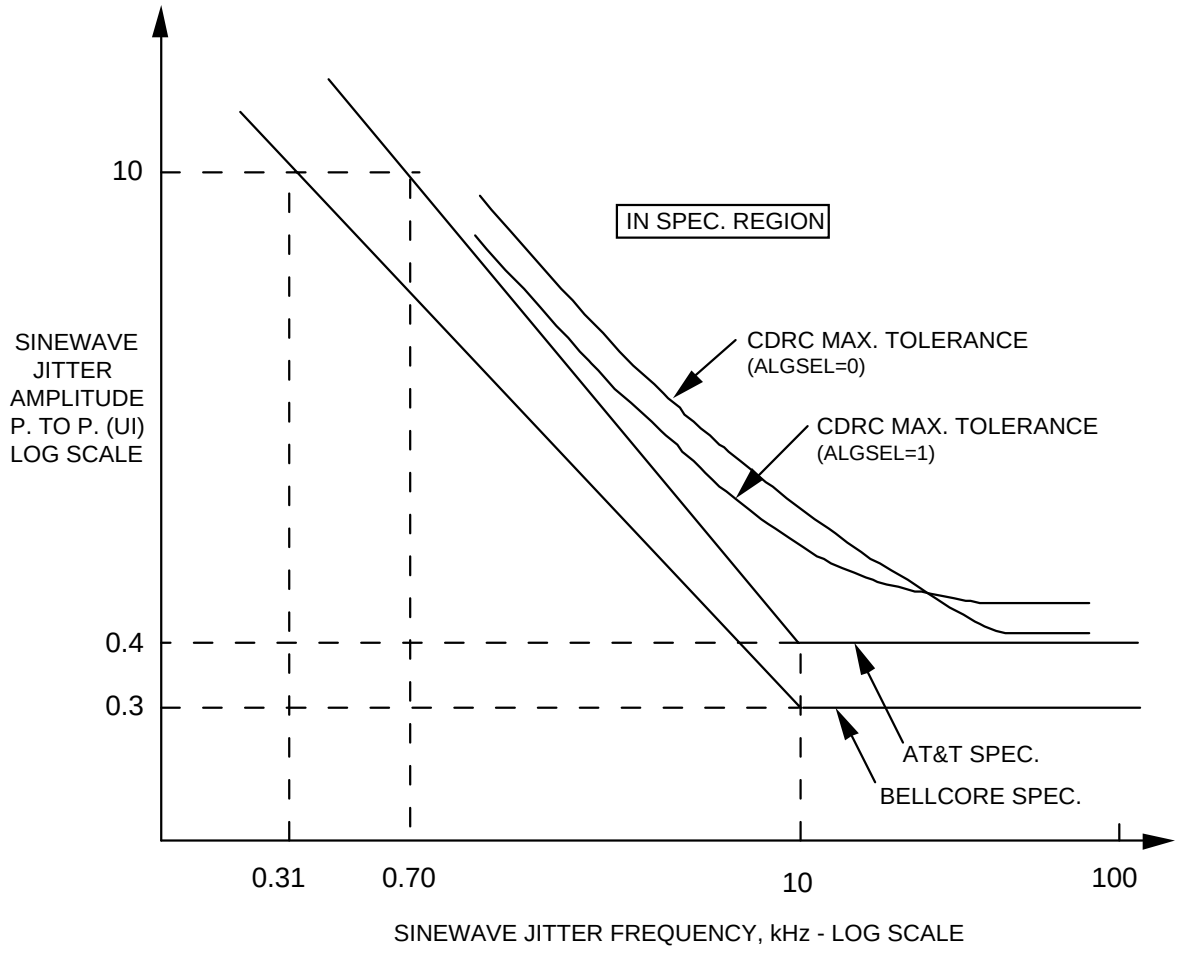
9.2 Clock and Data Recovery (CDRC)

The Clock and Data Recovery function is contained in the CDRC block and is active when clock recovery is not disabled. The CDRC provides clock and data recovery, B8ZS/HDB3 decoding, bipolar violation detection, and loss of signal detection. It recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop and recovers the NRZ data. Loss of signal is declared after exceeding a programmed threshold of 10, 31, 63, or 175 consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is removed after the occurrence of a single line pulse. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns. When the CDRC is disabled, the positive and negative sliced

pulses from RSLC are passed directly to the SDP[X] and SDN[X] outputs respectively.

The input jitter tolerance for DSX-1 interfaces complies with the Bellcore document TA-TSY-000170 and with the AT&T specification TR 62411. The tolerance is measured with a QRSS sequence (2^{20}-1 with 14 zero restriction). The CDRC block provides two algorithms for clock recovery that result in differing jitter tolerance characteristics. The first algorithm (when the ALGSEL register bit in the CDRC Configuration register (010H, 050H, 090H, 0D0H) is logic 0) provides good low frequency jitter tolerance, but the high frequency tolerance is close to the TR 62411 limit. The second algorithm (when ALGSEL is logic 1) provides much better high frequency jitter tolerance, approaching 0.5UIpp (Unit Intervals peak-to-peak), at the expense of the low frequency tolerance; the low frequency tolerance of the second algorithm is approximately 80% of that of the first algorithm. The DSX-1 jitter tolerance with ALGSEL set to 1 and to 0 is shown in Figure 7.

Figure 7 - DSX-1 jitter tolerance



The input jitter tolerance for E1 interfaces complies with ITU-T Recommendation G.823. The tolerance is measured with a 2^{15}-1 sequence. The E1 jitter tolerance with ALGSEL set to 1 and to 0 is shown in Figure 8 and Figure 9.

Figure 8 - E1 jitter tolerance with ALGSEL = 1

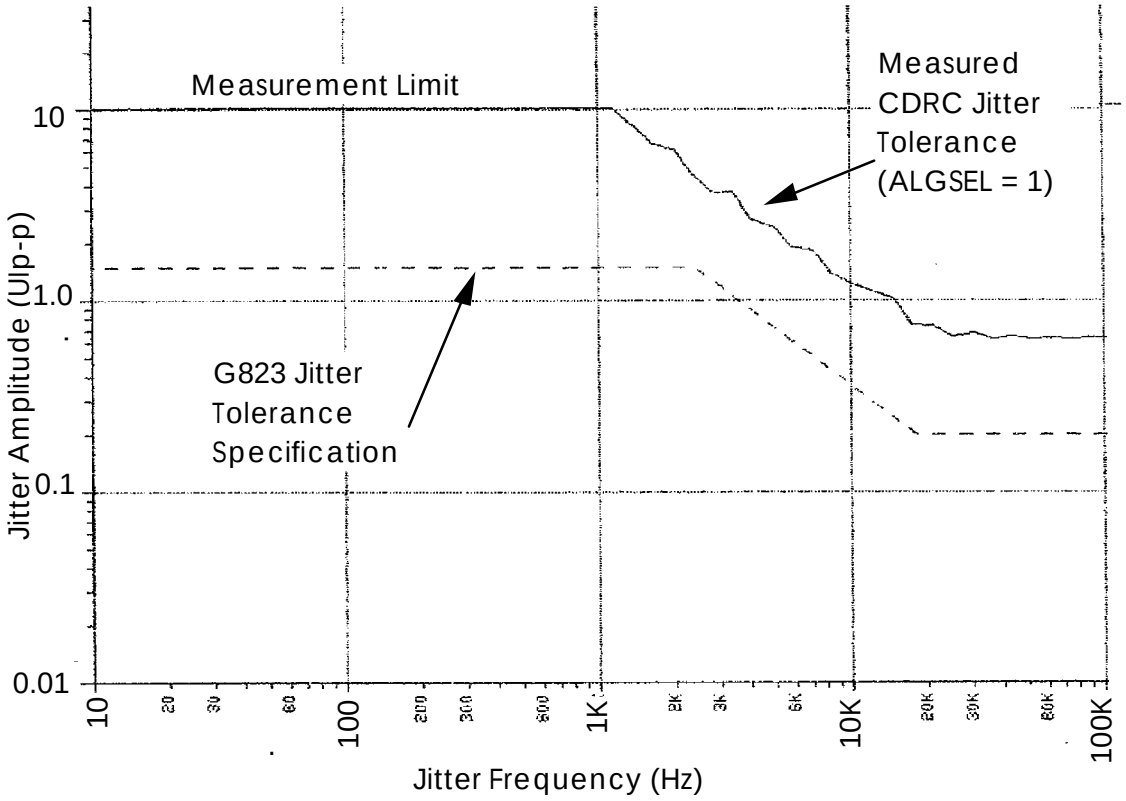
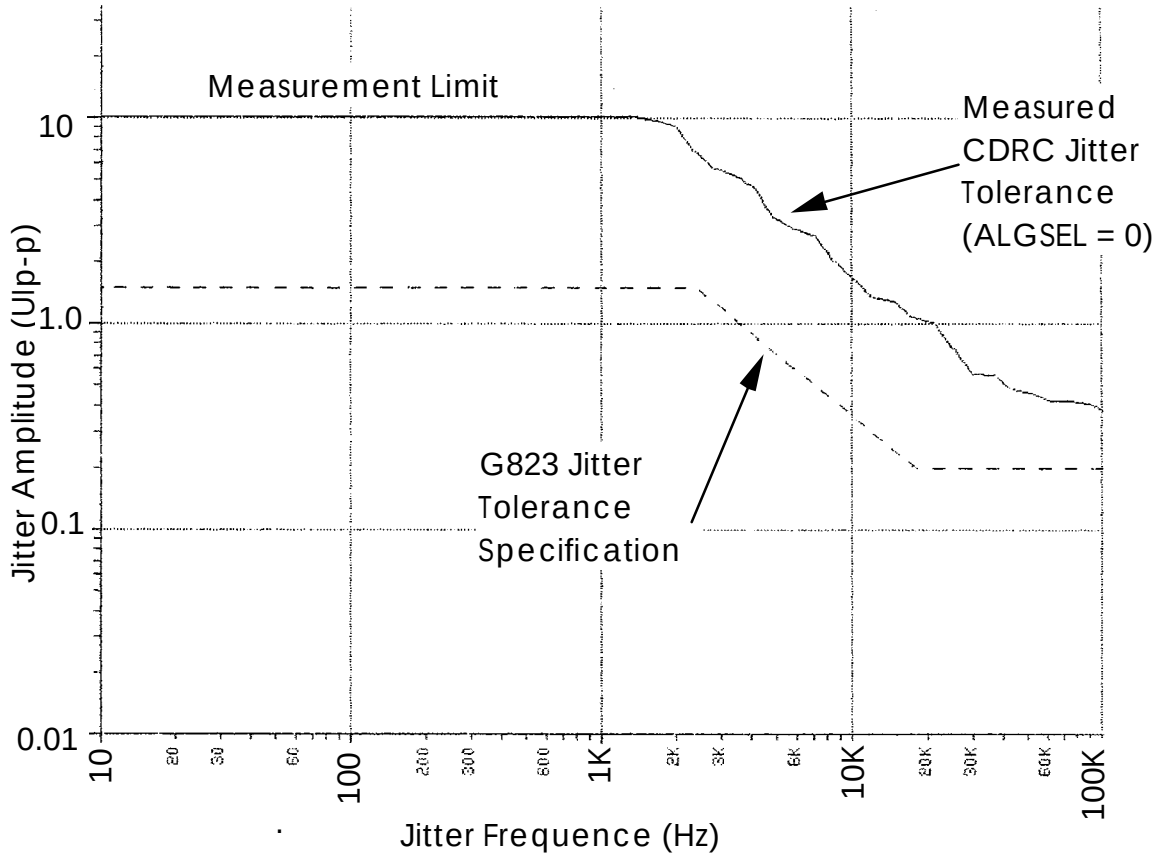


Figure 9 - E1 jitter tolerance with ALGSEL = 0



9.3 Line Code Violation Performance Monitor (LCV_PMON)

The Line Code Violation Performance Monitor function is provided by the (LCV_PMON) block. This block accumulates line code violation events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal. When the transfer clock signal is applied, the LCV_PMON block transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If enabled, an interrupt is generated whenever counter data is transferred into the holding registers. If the holding registers are not read between successive transfer clocks, the OVR register bit in the LCV_PMON Interrupt Enable/Status register (014H, 054H, 094H, and 0D4H) is asserted.

Generation of the individual LCV_PMON transfer clocks for specific quadrants of the QDSX is performed by writing to any of the LCV_PMON counter register locations of the particular quadrant. A global performance monitor transfer clock signal is generated by writing to register 007H. This will latch the counter values in all the LCV_PMONs and PRSMs of the QDSX. The holding register addresses are contiguous to facilitate polling operations.

9.4 Inband Loopback Code Detector (IBCD)

The Inband Loopback Code Detection function is provided by the IBCD block. This block detects the presence of either of two programmable loopback code sequences, ACTIVATE and DEACTIVATE, in framed or unframed DS-1 data streams. The inband code sequences are expected to be overwritten by the framing bit in framed data streams. Each code sequence is defined as the repetition of the programmed code in the PCM stream for at least 5.1 seconds. The code sequence detection and timing is compatible with the specifications defined in T1.403, TA-TSY-000312, and TR-TSY-000303. ACTIVATE and DEACTIVATE code indication is provided through internal register bits. An interrupt is generated to indicate when either code status has changed. The IBCD can detect inband loopback codes in the recovered unipolar receive data when configured to be in the receive data stream or in the unipolar input transmit data when configured to be in the transmit data stream. When enabled in the receive stream, the IBCD can be configured to enable and disable line loopback on detection of inband loopback activate and deactivate sequences.

9.5 Pseudo-Random Bit Sequence Monitor (PRSM)

The Pseudo-Random Sequence Monitor (PRSM) block monitors the recovered PCM data for the presence of an unframed 2^{15}-1 test sequence as defined in Recommendation O.151 and accumulates bit errors detected using this pseudo-random pattern. The test sequence may optionally be inverted before being checked against the generated pattern. The sequence monitor does not synchronize to an all zeroes pattern. The PRSM declares synchronization when less than 15 sequence errors are detected in 256 bit periods. Using this threshold, synchronization is achieved within 663 µsec (for DSX-1 applications) or 500 µsec (for E1 applications), 99.7% of the time, in the presence of a 10^{-2} bit error rate. Once synchronized, the mean time between loss of synchronization events is greater than 136 minutes (for DSX-1) or 103 minutes (for E1), in the presence of a 10^{-2} bit error rate. When the test sequence is no longer present (as indicated by a bit error rate of 0.5) the PRSM will lose synchronization in 48 µsec (for DSX-1) or 36 µsec (for E1), more than 99% of the time. In the

presence of random data (a bit error rate of 0.5) the mean time between false synchronization events is greater than 184 years.

The PRSM can be configured to detect either an inverted or a noninverted 2^{15}-1 pseudorandom bit sequence (PRBS). An inverted 2^{15}-1 PRBS will contain at most 15 consecutive zeroes, while a non-inverted 2^{15}-1 PRBS will contain at most 14 consecutive zeroes.

The PRSM block accumulates bit error events with a saturating counter over consecutive intervals as defined by the period of a latch clock signal. An internal latch clock signal, unique to each PRSM in the QDSX, can be generated by writing to any of the particular PRSM holding registers. A write to any PRSM holding register in quadrant 1 of the QDSX generates an internal latch clock pulse for the PRSM in quadrant 1. Similarly a write to any PRSM holding register in any other quadrant generates an internal latch clock pulse for the PRSM in that same quadrant. A write to register 007H will generate a global performance monitor latch clock signal. A write to this register will toggle the internal latch clock pulses to all four PRSMs as well as all four LCV_PMONs (which operate in a similar fashion).

If enabled, an interrupt is generated whenever counter data is transferred into the PRSM holding registers. If the holding registers are not read between successive transfer clocks, the overrun (OVR) bit in the PRSM Control/Status Register is set.

An indication of whether or not the pseudorandom sequence monitor is synchronized is provided via the PRSM Control/Status register and, if enabled, an interrupt is generated whenever a loss of synchronization or resynchronization occurs. The PRSM can detect pseudorandom sequences in the receive stream, or in the transmit stream if TDUAL is set to logic 0. PRSM functions are available only when microprocessor access is available (MICROEN is high).

9.6 Timing Options (TOPS)

If jitter attenuation is required, then XCLK must be a 24X clock, and TOPS will generate the 8X clock either from the DJAT PLL smoothed 8X clock from quadrant 1, or by dividing XCLK by 3. This 8X clock will be presented on CLKO8X. Otherwise, XCLK is expected to be an 8X high speed clock and TOPS will simply buffer it before passing it off as the internal high speed

reference clock. When an 8X reference is provided, the CLKO1X output is active, and carries the internal 8X reference clock divided by 8.

9.7 Pseudo-Random Bit Sequence Generator (PRSG)

The Pseudo-Random Bit Sequence Generator (PRSG) generates an unframed 2^{15}-1 test sequence as defined in Recommendation O.151. The PRSG can be enabled to overwrite the unipolar input transmit data when configured to be in the transmit data stream or the recovered unipolar receive data when configured to be in the receive data stream. The microprocessor can force the PRSG to insert single bit errors in the pseudorandom data for diagnostic purposes.

The PRSG can be configured to generate either an inverted or a noninverted 2^{15}-1 pseudorandom bit sequence (PRBS). An inverted 2^{15}-1 PRBS will contain at most 15 consecutive zeroes, while a non-inverted 2^{15}-1 PRBS will contain at most 14 consecutive zeroes.

9.8 Inband Loopback Code Generator (XIBC)

The Inband Loopback Code Generator function is provided by the XIBC block. This block generates a stream of inband loopback codes to be inserted into a DS-1 data stream. The stream consists of continuous repetitions of a specific code. The contents of the code and its length are programmable from 3 to 8 bits. The XIBC can be enabled to overwrite the unipolar input transmit data when configured to be in the transmit data stream or the recovered unipolar receive data when configured to be in the receive data stream.

9.9 B8ZS/HDB3/AMI Line Encoder (LCODE)

The B8ZS/HDB3/AMI line encoding function is provided by the LCODE block. This block will encode single-rail data inputs into bipolar B8ZS, HDB3, or AMI format. For DSX-1 applications, B8ZS line encoding is selected by default. For E1 applications, HDB3 line encoding is selected by default. The microprocessor may instruct the LCODE block to insert line code violations for diagnostic purposes.

9.10 Digital Jitter Attenuator (DJAT)

The Digital Jitter Attenuator (DJAT) function is used to attenuate jitter in the transmit clock when required. The DJAT block receives jittered data and stores

this data in a FIFO. The data emerges from the DJAT timed to the jitter attenuated clock and is transferred to the XPLS block for transmission.

The DJAT generates a "jitter-free" 1.544/2.048 MHz clock by adaptively dividing the 24x XCLK input according to the phase difference between the generated "jitter-free" clock and the input data clock to DJAT (TCLKI[X] when DJAT is in the default transmit path, or the recovered clock RCLKO[X] if in line loopback mode or when DJAT is configured to be on the receive path). Phase variations in the input clock with a jitter frequency above 8.8 Hz (for the E1 format) or 6.6 Hz (for the T1 formats) are attenuated by 6 dB per octave of jitter frequency. Phase variations below these jitter frequencies are tracked by the "jitter-free" clock.

Jitter Characteristics

The DJAT provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 28 UIpp of input jitter at jitter frequencies above 6 Hz for DSX-1 interfaces or 9 Hz for E1 interfaces. For jitter frequencies below 6/9 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In most applications DJAT will limit jitter tolerance at lower jitter frequencies only. The DJAT block meets the low frequency jitter tolerance requirements of AT&T TR 62411 for DSX-1 interfaces, and ITU-T G.823 for E1 interfaces.

Outgoing jitter may be dominated by the generated residual jitter in cases where the incoming jitter is insignificant. This residual jitter is directly related to the use of the 24x clock for the digital phase locked loop.

For DSX-1 interfaces, DJAT meets the jitter attenuation requirements of AT&T TR 62411. DJAT meets the implied jitter attenuation requirements for a TE or an NT1 specified in ANSI T1.408, and for a type II customer interface specified in ANSI T1.403.

For E1 interfaces, DJAT meets the jitter attenuation requirements of ITU-T Recommendations G.737, G.738, G.739, and G.742.

Jitter Tolerance

Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For DJAT, the input jitter tolerance is 29 Unit Intervals peak-to-peak (UIpp) for a DSX-1 interface with a worst case frequency offset of 354 Hz. The input jitter tolerance is 35 UIpp for an E1 interface with a worst case frequency offset

of 308 Hz. It is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK divided by 24 and that of the input data clock. These tolerances are shown in Figure 10 and Figure 11.

Figure 10 - DSX-1 Jitter Tolerance

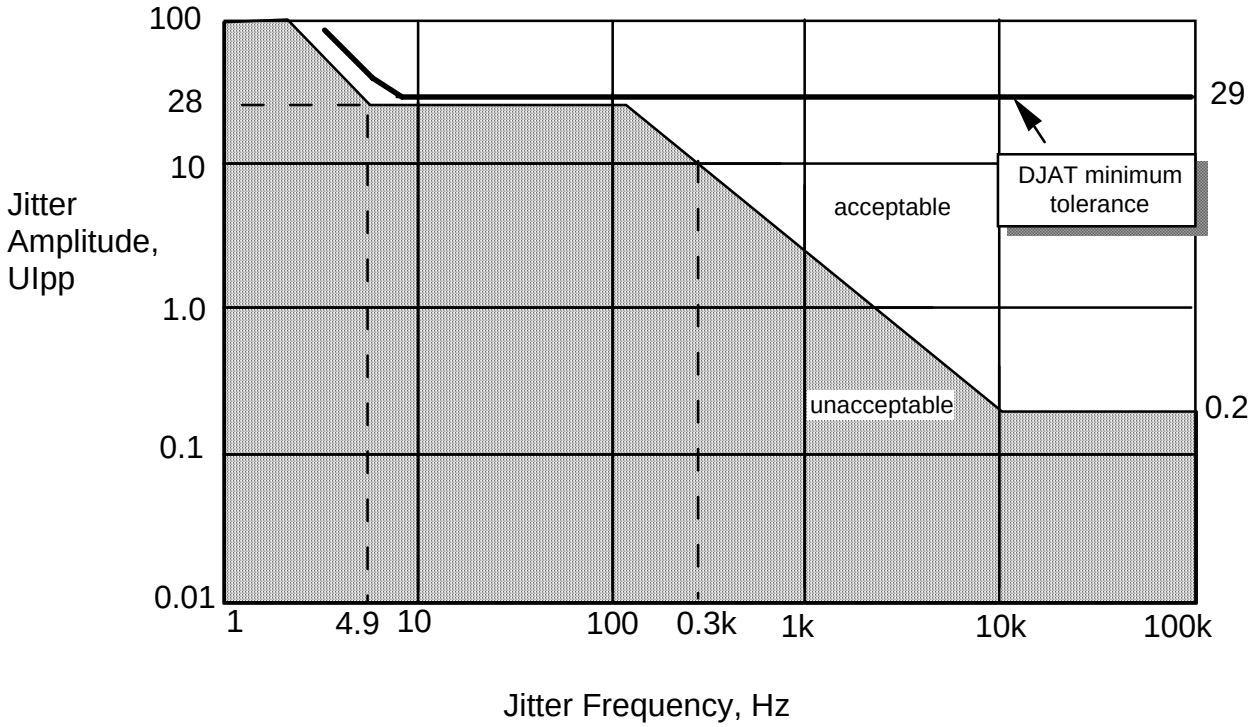
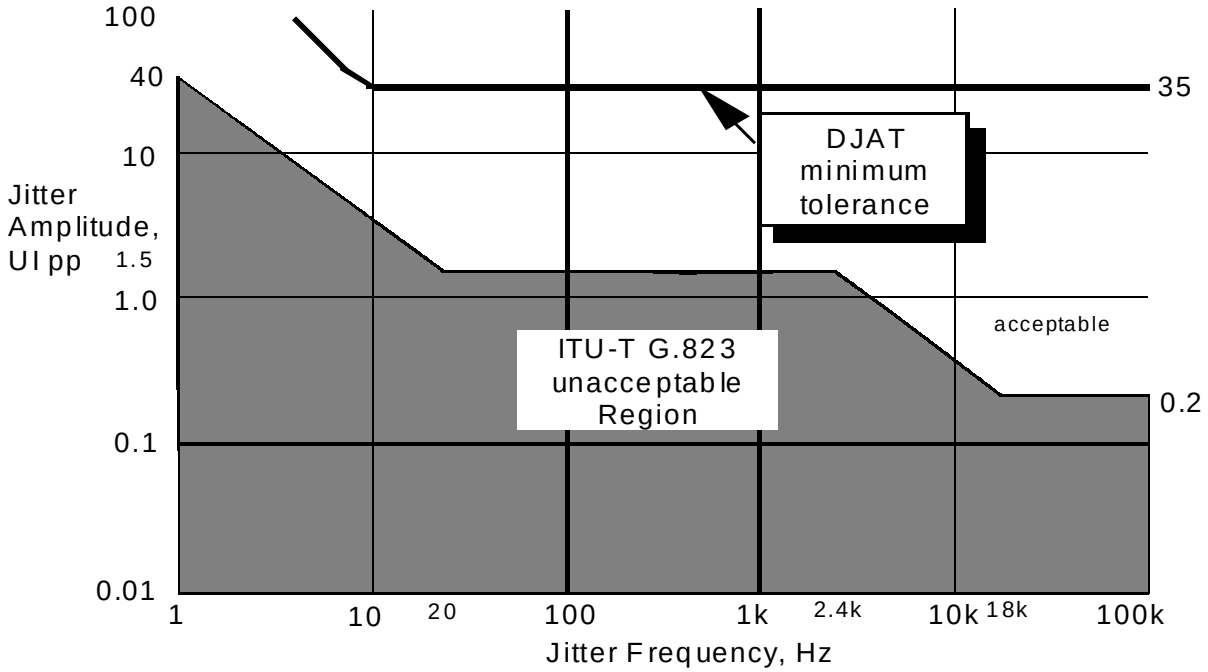


Figure 11 - E1 Jitter Tolerance



The accuracy of the XCLK frequency and that of the DJAT PLL reference input clock used to generate the "jitter-free" clock have an effect on the minimum jitter tolerance. For DSX-1 interfaces, the DJAT PLL reference clock accuracy can be ±130 Hz from 1.544 MHz, and the XCLK input accuracy can be ±100 ppm from 37.056 MHz. For E1 interfaces, the PLL reference clock accuracy can be ± 50 Hz from 2.048 MHz, and the XCLK input accuracy can be ±50 ppm from 49.152 MHz. The minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK ÷ 24 are shown in Figure 12 and Figure 13.

Figure 12 - DJAT Minimum Jitter Tolerance vs. XCLK Accuracy (DSX-1 Case)

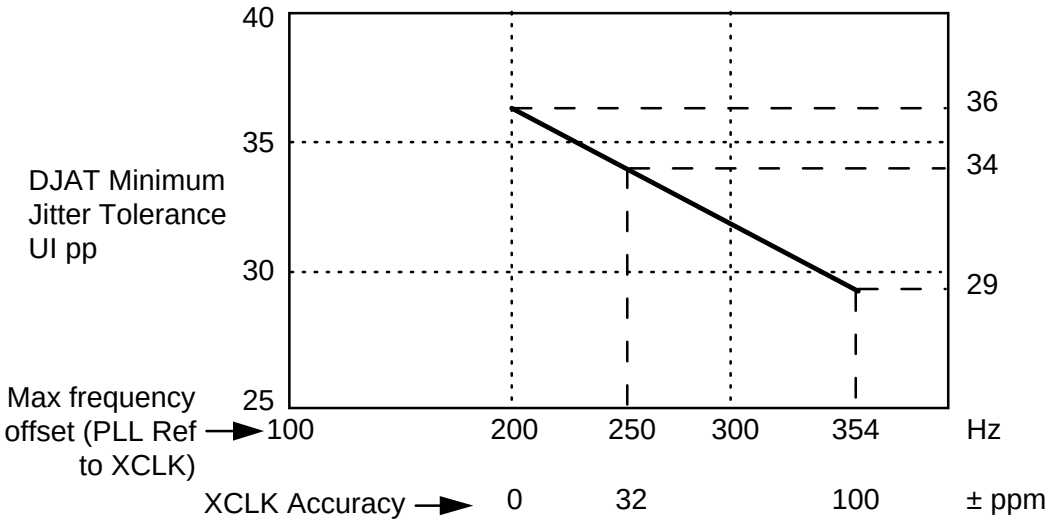
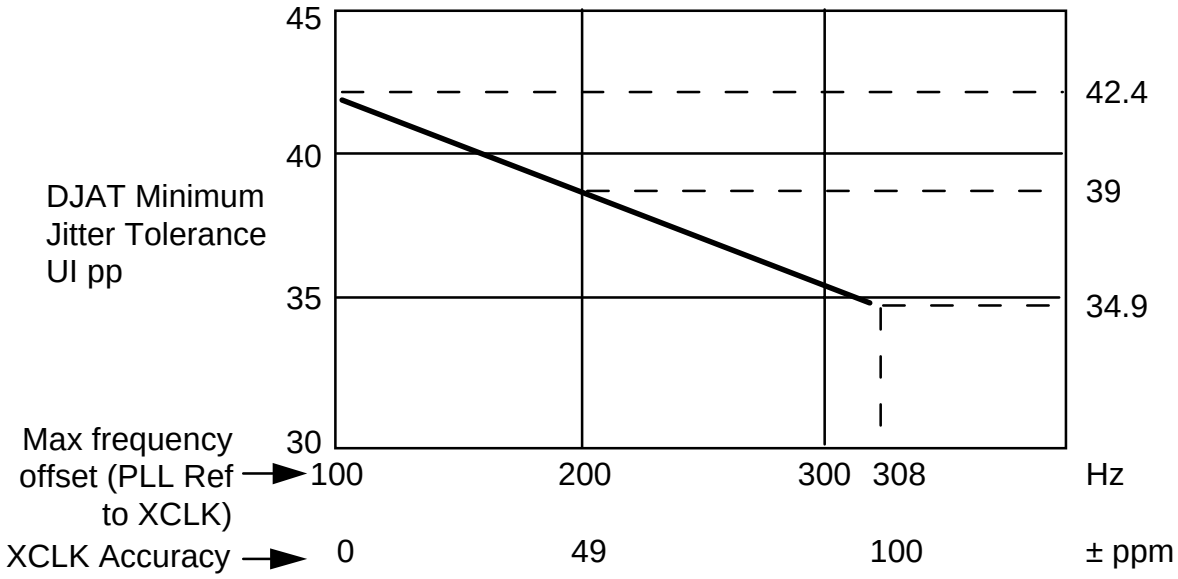


Figure 13 - DJAT Minimum Jitter Tolerance vs. XCLK Accuracy (E1 Case)



Jitter Transfer

The output jitter for jitter frequencies from 0 to 6.6 Hz (for DSX-1 interfaces) or from 0 to 8.8 Hz (for E1 interfaces) is no more than 0.1 dB greater than the input jitter, excluding the residual jitter. Jitter frequencies above 6.6/8.8 Hz are attenuated at a level of 6 dB per octave, as shown in Figure 14 and Figure 15.

Figure 14 - DSX-1 Jitter Transfer

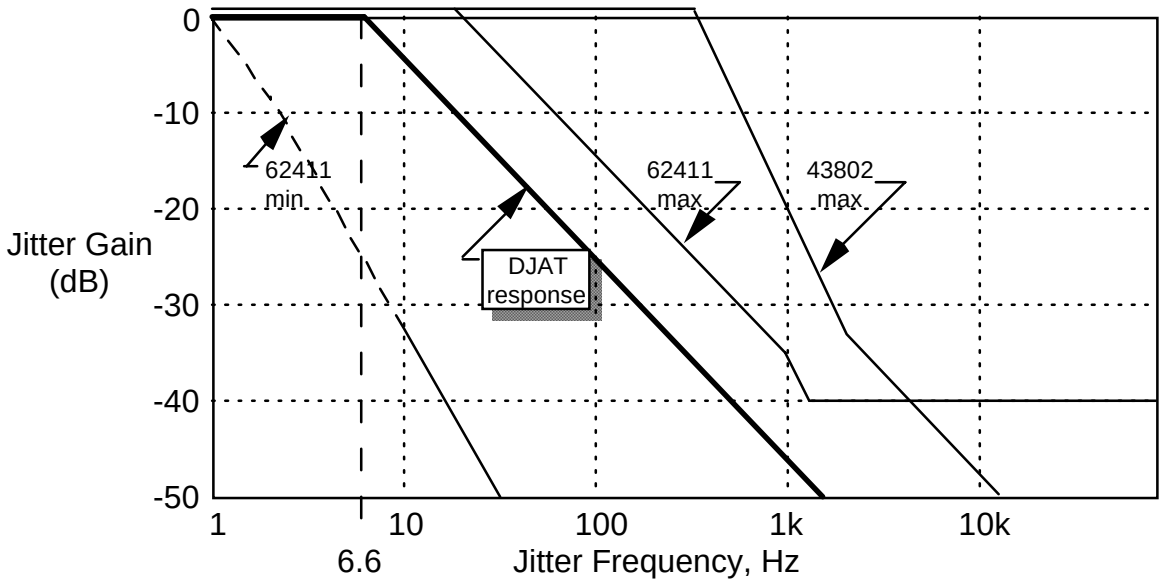
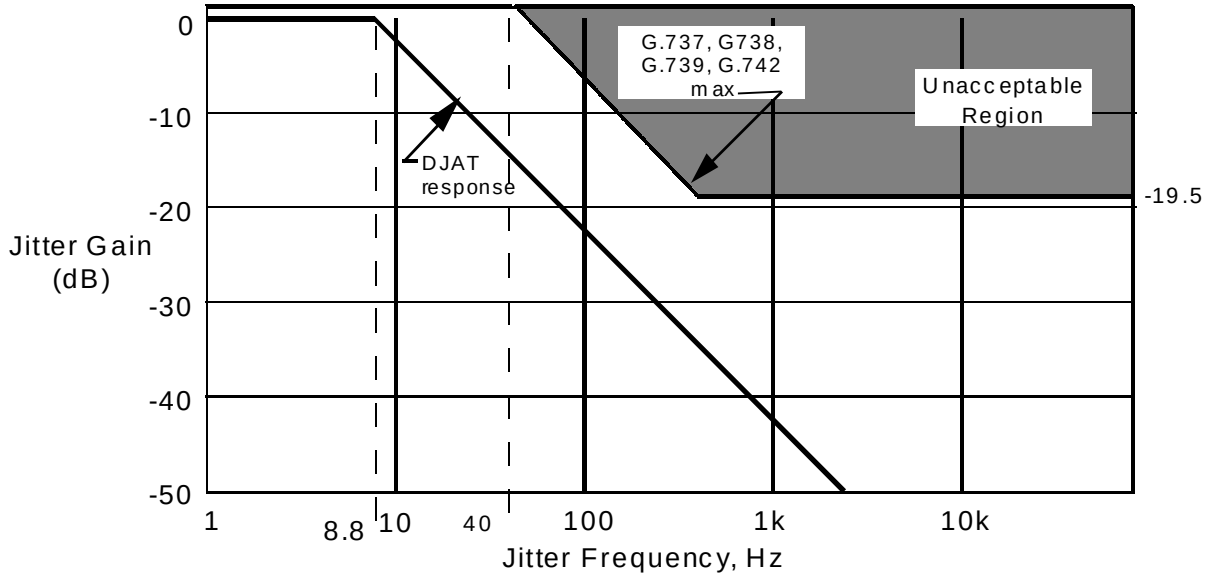


Figure 15 - E1 Jitter Transfer



9.11 Analog Pulse Generator (XPLS)

The Analog Pulse Generator function is provided by the Transmit Pulse Generator (XPLS) block that converts Non-Return-to-Zero (NRZ) pulses into line signals suitable for use in a G.703 1544 kbit/s and 2048 kbit/s intra-office environment. A logical "1" on the positive NRZ input to XPLS causes a positive pulse to be transmitted; a similar signal on the negative NRZ input to XPLS causes a negative pulse to be transmitted. If both positive and negative NRZ inputs to XPLS are logical "0" or "1," no output pulse is transmitted.

The output pulse shape is synthesized digitally from user-programmed template settings with an internal Digital to Analog (D/A) converter. The converter is updated eight times per period with these programmed words. These words define the output pulse shape. Recommended codes for DSX-1 and CEPT E1 120 Ω symmetrical lines and 75 Ω coaxial lines are given in the Operations section. If an external circuit different from that recommended in the following diagram is used, the pulse generator permits creation of custom pulse shapes. Refer to the Operations section for details.

AMI signaling is created by exciting either the internal TIP or RING DRIVERS that drive a line-coupling transformer differentially via the TXTIP[4:1] and

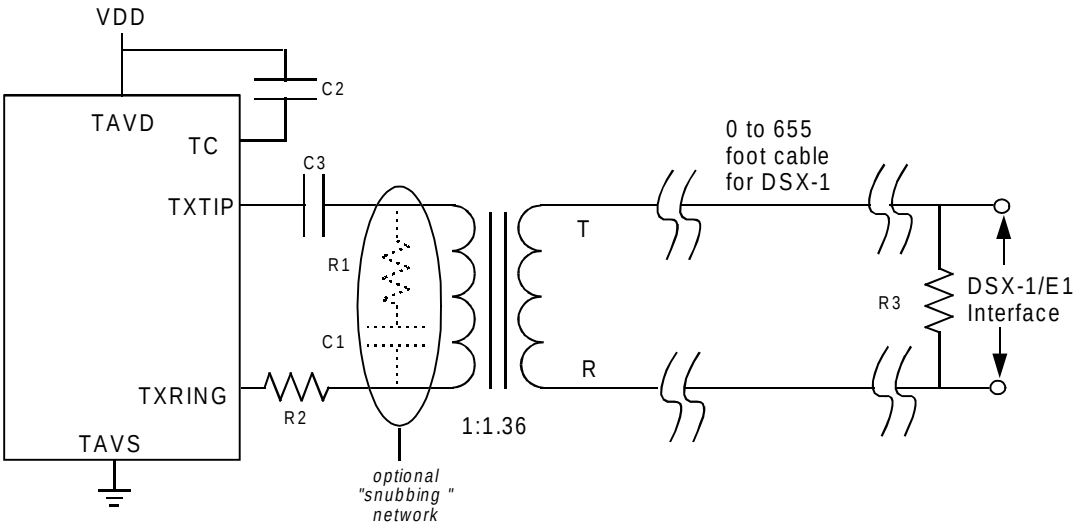
TXRING[4:1] outputs. This differential driving scheme insures a small positive to negative pulse imbalance. The drivers, with the step-up transformer, amplify the output pulses to their final levels. The TIP and RING drivers also supply the high current capability required to drive the low impedance output load.

A small, high-frequency negative-going spike may be observed on the falling edge of the transmit pulse. This spike can be filtered out by using the optional "snubbing" network shown in the following diagram. This snubbing network should not be required when driving longer DSX-1 lines.

The XPLS includes a driver performance monitor to detect nonfunctional links. Two monitor inputs, PM_TIP and PM_RING, are internally bonded to the XPLS's own TXTIP and TXRING outputs. If no pulses are detected alternately across the TIP or RING monitor points for 62 or 63 consecutive clock periods (the exact number of clock periods, 62 or 63, depends upon the pattern of bipolar violations and the line-build out), the monitored link is declared failed. The XPLS can be programmed to produce an interrupt whenever the link monitor state changes.

The XPLS block provides Alarm Indication Signaling (AIS) generation capability by generating alternating mark signals on the link when the TAIS bit is set high in the XPLS Control/Status register (02DH, 06DH, 0ADH, and 0EDH). This AIS generation may optionally be enabled when internal loopback modes are enabled.

Figure 16 - External Analog Transmit Interface Circuit



Format	R1	R2	R3	C1	C2	C3
DSX-1Zo=100 Ω	22Ω±10%	0Ω	100Ω	1nF±10%	470nF±10%	0.68µF±10%,50V
E1 Zo=120 Ω	47Ω±10%	2.7Ω±5%,1/8W	120Ω	1nF±10%	470nF±10%	0.68µF±20%,50V
E1 Zo=75 Ω	47Ω±10%	6.2Ω±5%,1/8W	75Ω	1nF±10%	470nF±10%	0.68µF±20%,50V

The transformer used should be designed for use in T1/CEPT/ISDN-PRI applications. Many manufacturers have standard products for these applications. Typical characteristics of a suitable transformer are given in the following table.

Table 3 -

Turns Ratio (PRI:SEC)	OCL (mH min.)	$C_{w/w}$ (pF max.)	L_L (µH max.)	DCR pri. (Ω max.)	DCR sec. (Ω max.)
1:1.36	1.20	35	0.80	0.80	1.2

where OCL is the open-circuit inductance,

$C_{w/w}$ is the inter-winding capacitance,

L_L is the leakage inductance, and

DCR is the DC resistance.

PMC-Sierra has verified the operation of the XPLS functional block with the following 1:1.36 transformers:

- Pulse Engineering PE64937 (1:1.36)
- Pulse Engineering PE65340 (1:1.36) (for extended temperature range)
- BH Electronics 500-1776 (1:1.36)

Many manufacturers produce dual transformers containing the1:2 CT and 1:1.36 transformers necessary for the receiver and transmitter circuits. PMC-Sierra has verified the operation of XPLS and RSLC with the following dual parts:

- Pulse Engineering PE64952
- Pulse Engineering PE65774 (for extended temperature range)
- BH Electronics500-1777

9.12 IEEE P1149.1 JTAG Test Access Port

The IEEE P1149.1 JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The QDSX identification code is 043140CD in hexadecimal format, shifted least significant bit first.

9.13 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the QDSX. The register set is accessed as follows:

9.14 Register Memory Map

Address				Register
#1	# 2	# 3	# 4	
000H	040H	080H	0C0H	Receive Configuration
001H	041H	081H	0C1H	Transmit Configuration
002H	042H	082H	0C2H	TX/RX Block Placement
003H	043H	083H	0C3H	Interrupt Source
004H	044H	084H	0C4H	Reserved
005H	045H	085H	0C5H	Diagnostics
006H				Master Test
007H				Revision/Chip ID/Global Monitoring Update
008H				Interrupt Quadrant ID
009H				TOPS Master Clock Configuration/Clock Activity Monitor
	046H	086H	0C6H	Reserved
	047H	087H	0C7H	Reserved
	048H	088H	0C8H	Reserved
	049H	089H	0C9H	Reserved
00AH	04AH	08AH	0CAH	TOPS Clock Timing Options
00BH	04BH	08BH	0CBH	LCODE Transmit Line Code Configuration
00CH	04CH	08CH	0CCH	Reserved
00DH	04DH	08DH	0CDH	Reserved
00EH	04EH	08EH	0CEH	Reserved
00FH	04FH	08FH	0CFH	Reserved
010H	050H	090H	0D0H	CDRC Configuration
011H	051H	091H	0D1H	CDRC Interrupt Enable

Address				Register
#1	# 2	# 3	# 4	
012H	052H	092H	0D2H	CDRC Interrupt Status
013H	053H	093H	0D3H	Reserved
014H	054H	094H	0D4H	LCV_PMON Interrupt Enable/Status
015H - 019H	056H - 059H	096H - 099H	0D6H - 0D9H	LCV_PMON Reserved
01AH	05AH	09AH	0DAH	LCV_PMON LCV Count (LSB)
01BH	05BH	09BH	0DBH	LCV_PMON LCV Count (MSB)
01CH	05CH	09CH	0DCH	DJAT Interrupt Status
01DH	05DH	09DH	0DDH	DJAT Reference Clock Divisor (N1) Control
01EH	05EH	09EH	0DEH	DJAT Output Clock Divisor (N2) Control
01FH	05FH	09FH	0DFH	DJAT Configuration
020H	060H	0A0H	0E0H	IBCD Configuration
021H	061H	0A1H	0E1H	IBCD Interrupt Enable/Status
022H	062H	0A2H	0E2H	IBCD Activate Code
023H	063H	0A3H	0E3H	IBCD Deactivate Code
024H	065H	0A4H	0E4H	XIBC Control
025H	065H	0A5H	0E5H	XIBC Loopback Code
026H	066H	0A6H	0E6H	Reserved
027H	067H	0A7H	0E7H	PRSG Configuration
028H	068H	0A8H	0E8H	PRSM Reserved
029H	069H	0A9H	0E9H	PRSM Control/Status
02AH	06AH	0AAH	0EAH	PRSM Bit Error Event Count (LSB)
02BH	06BH	0ABH	0EBH	PRSM Bit Error Event Count (MSB)
02CH	06CH	0ACH	0ECH	XPLS Line Length Configuration
02DH	06DH	0ADH	0EDH	XPLS Control/Status

Address				Register
#1	# 2	# 3	# 4	
02EH	06EH	0AEH	0EEH	XPLS CODE Indirect Address
02FH	06FH	0AFH	0EFH	XPLS CODE Indirect Data
030H	070H	0B0H	0F0H	RSLC Configuration
031H	071H	0B1H	0F1H	RSLC Interrupt Enable/Status
100H-1FFH				Reserved for Test

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the QDSX. Normal mode registers (as opposed to test mode registers) are selected when A[8] is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits should be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the QDSX to determine the programming state of the device.

3. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect QDSX operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the QDSX operates as intended, reserved register bits must only be written with logic zero. Similarly, writing to reserved registers should be avoided.

Register 000H, 040H, 080H, and 0C0H: Receive Configuration

Bit	Type	Function	Default
Bit 7	R/W	RDPINV	0
Bit 6	R/W	RDNINV	0
Bit 5	R/W	RDUAL	0
Bit 4	R/W	RRISE	0
Bit 3	R/W	AUTO_LLB_EN	0
Bit 2	R/W	AUTO_AIS_EN	0
Bit 1	R/W	BPVCNT	0
Bit 0	R/W	CEPT	0

These registers enable the Receive Interface to handle the various input and output waveform formats.

RDPINV,RDNINV:

The RDPINV and RDNINV bits enable the Receive Interface to logically invert the signals output on multifunction pins RDD/RDP[X] and RLCV/RDN[X], respectively. When RDPINV is set to logic 1, the interface inverts the output on RDD/RDP[X]. When RDPINV is set to logic 0, the interface outputs RDD/RDP[X] normally. When RDNINV is set to logic 1, the interface inverts the output on RLCV/RDN[X]. When RDNINV is set to logic 0, the interface outputs RLCV/RDN[X] normally.

RDUAL:

RDUAL configures the RDD/RDP[X] and RLCV/RDN[X] outputs to unipolar or bipolar form. When the RDUAL bit is set to logic 1, the bipolar outputs RDP[X] and RDN[X] are enabled. When the RDUAL bit is set to logic 0, the unipolar outputs RDD[X] and RLCV[X] are enabled. The RDUAL bit is logically "ORed" with the RDUAL input pin. If either are set to logic 1, then the bipolar outputs RDP and RDN will be enabled. If the XIBC or PRSG are in the receive path, they will be bypassed if RDUAL is set. Also, though bipolar violations in the input data will appear on RDP and RDN, the IBCD and PRSM blocks will operate on a HDB3/B8ZS/AMI decoded version of the data, depending on the configuration of CDRC. Note that the DCR bit in the CDRC Configuration register (010H, 050H, 090H, and 0D0H) takes precedence over the RDUAL bit.

RRISE:

The RRISE bit configures the interface to update the multifunction outputs RDD/RDP[X] and RLCV/RDN[X] on the rising edge of RCLKO[X]. When RRISE is set to logic 1, the interface is enabled to update the RDD[X]/TDP[X] and RLCV/RDN[X] output pins on the rising RCLKO[X] edge. When RRISE is set to logic 0, the interface is enabled to update the outputs on the falling RCLKO[X] edge.

AUTO_LLB_EN:

When the AUTO_LLB_EN bit is set to logic 1 and the IBCD is enabled in the receive path, then when the IBCD in a quadrant detects the inband loopback activate code, the quadrant is immediately placed in line loopback mode. The quadrant is taken out of line loopback when the inband loopback deactivate code is detected, or when AUTO_LLB_EN is written with a logic zero. Whenever the quadrant is placed in line loopback mode due to the reception of an inband loopback code, the AUTO_LLB bit will be set to logic 1 in the Diagnostics register. AUTO_LLB_EN should not be set to logic 1 if the DJAT is bypassed (FIFOBYP=1), or if DJATTX =0. AUTO_LLB_EN has no effect when IBCDTX =1.

AUTO_AIS_EN:

When set to logic 1, the AUTO_AIS_EN bit enables the insertion of AIS in the receive path whenever the quadrant is in line loopback mode due to the reception of an inband line loopback activate code. AUTO_AIS_EN has no effect when AUTO_LLB_EN is a logic zero.

BPVCNT:

The BPVCNT bit enables only bipolar violations to indicate line code violations and be accumulated in the LCV_PMON LCV Count registers. When BPVCNT is set to logic 1, only BPVs not part of a valid AMI, B8ZS, or HDB3 signature (depending on the configuration of the receiver) generate an LCV indication and increment the LCV_PMON LCV counter. When BPVCNT is set to logic 0, both BPVs not part of a valid signature and excessive zeros generate an LCV indication and increment the LCV_PMON LCV counter. Excessive zeros is defined for this operation to be a sequence of zeros greater than 15 bits long for an AMI coded T1 signal, greater than 7 bits long for a B8ZS coded signal, and greater than 3 bits long for an E1 signal.

CEPT:

The CEPT bit configures the receiver for E1 applications. When CEPT is set to logic 1, the receiver is configured for E1 applications. When CEPT is set to logic 0, the receiver is configured for T1 applications. All CEPT bits in all four

quadrants and in both the Transmit Configuration (registers 001H, 041H, 081H, and 0C1H) and Receive Configuration registers should be set to the same value.

Register 001H, 041H, 081H, and 0C1H: Transmit Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TDPINV	0
Bit 3	R/W	TDNINV	0
Bit 2	R/W	TDUAL	0
Bit 1	R/W	TFALL	0
Bit 0	R/W	CEPT	0

These registers enable the Transmit Interface to generate the required digital output waveform format.

TDPINV,TDNINV:

The TDPINV and TDNINV bits enable the Transmit Interface to logically invert the input signals on the TDD/TDP[X] and TDN[X] inputs, respectively. When TDPINV is set to logic 1, the TDD/TDP[X] input is inverted. When TDPINV is set to logic 0, the TDD/TDP[X] input is not inverted. When TDNINV is set to logic 1, the TDN[X] input is inverted. When TDNINV is set to logic 0, the TDN[X] input is not inverted.

TDUAL:

TDUAL configures the TDD/TDP[X] and TDN[X] inputs to unipolar or bipolar form. When the TDUAL bit is set to logic 1, the bipolar inputs TDP[X] and TDN[X] are enabled. When the TDUAL bit is set to logic 0, the unipolar input TDD[X] is enabled and TDN[X] is ignored. The TDUAL bit is logically "ORed" with the TDUAL input pin. If either are set to logic 1, then the bipolar inputs will be enabled.

TFALL:

The TFALL bit enables the Transmit Interface to sample the TDD/TDP[X] and TDN[X] inputs on the falling TCLKI[X] edge. When TFALL is set to logic 1, the interface is enabled to sample the inputs on the falling TCLKI[X] edge. When TFALL is set to logic 0, the interface is enabled to sample the inputs on the rising TCLKI[X] edge.

CEPT:

The CEPT bit configures the transmitter for E1 applications. When CEPT is set to logic 1, the transmitter is configured for E1 applications. When CEPT is set to logic 0, the transmitter is configured for T1 applications. All CEPT bits in all four quadrants and in both the Transmit Configuration and Receive Configuration (registers 000H, 040H, 080H, and 0C0H) registers should be set to the same value.

Register 002H, 042H, 082H, and 0C2H: TX/RX Block Placement

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PRSMTX	0
Bit 3	R/W	PRSGTX	1
Bit 2	R/W	IBCDTX	0
Bit 1	R/W	XIBCTX	1
Bit 0	R/W	DJATTX	1

This register is used to configure the PRSM, PRSG, IBCD, XIBC, and DJAT blocks to be on the transmit or the receive data paths.

PRSMTX:

The PRSMTX bit determines whether the PRSM block is placed on the transmit or receive data paths. When PRSMTX is set to a logic 1, then the PRSM block is moved to the transmit path and will be used to synchronize to 2^{15}-1 PRBS sequences on the TDD[X] input. When the PRSM block is in the transmit path, the TDUAL bits (in registers 001H, 041H, 081H, and 0C1H) and the TDUAL input pin must be set to logic 0 for proper operation. When PRSMTX is set to a logic 0, then the PRSM block is moved to the receive path and will be used to synchronize to 2^{15}-1 PRBS sequences from the analog RXTIP[X] and RXRING[X] inputs.

PRSGTX:

The PRSGTX bit determines whether the PRSG block is placed on the transmit or receive data paths. When PRSGTX is set to a logic 1, then the PRSG block is moved to the transmit path and can be used to insert the 2^{15}-1 PRBS sequence into the transmit data. When the TDUAL bit or the TDUAL pin are logic 1, then the PRSG has no effect if placed in the transmit path. When PRSGTX is set to a logic 0, then the PRSG block is moved to the receive path and can be used to source an unframed 2^{15}-1 PRBS sequence to the RDD[X] output.

IBCDTX:

The IBCDTX bit determines whether the IBCD block is placed on the transmit or receive data paths. When IBCDTX is set to a logic 1, then the IBCD block is moved to the transmit path and can be used to detect inband loopback code sequences in the transmit data. When the IBCD block is in the transmit path, the TDUAL bits (in registers 001H, 041H, 081H, and 0C1H) and the TDUAL input pin must be set to logic 0 for proper operation. When IBCDTX is set to a logic 0, then the IBCD block is moved to the receive path will be used to detect inband loopback code sequences from the analog RXTIP[X] and RXRING[X] inputs.

XIBCTX:

The XIBCTX bit determines whether the XIBC block is placed on the transmit or receive data paths. When XIBCTX is set to a logic 1, then the XIBC block is moved to the transmit path and can be used to insert unframed inband loopback code sequences into the transmit data. When the TDUAL bit or the TDUAL pin are logic 1, then the XIBC has no effect if placed the transmit path. When XIBCTX is set to a logic 0, then the XIBC block is moved to the receive path and can be used to source an unframed inband loopback code sequence to the RDD[X] output.

DJATTX:

The DJAT bit determines whether the DJAT block is placed on the transmit or receive data paths. When DJATTX is set to a logic 1, then the DJAT block is moved to the transmit path to attenuate jitter in the transmit data stream. When DJATTX is set to a logic 0, then the DJAT block is moved to the receive path and will attenuate the jitter on the RDD/RDP[X], RLCV/RDN[X], and RCLKO[X] outputs. Note that a 24X clock must be input on XCLK for jitter attenuation to operate (see TOPS Clock Timing Options register 00AH, 04AH, 08AH, and 0CAH and TOPS Master Clock Configuration/Clock activity monitor register 009H). Whenever the DJAT is not active in the transmit path, the system 8X clock (presented on CLK08X) must be synchronous to TCLKI[X], and line loopback cannot be used. Refer to the operations section for more details on using the QDSX without the DJAT enabled in the transmit path.

Register 003H, 043H, 083H, and 0C3H: Interrupt Source

Bit	Type	Function	Default
Bit 7	R	RLSC	0
Bit 6	R	XPLS	0
Bit 5	R	IBCD	0
Bit 4	R	PRSM	0
Bit 3	R	LCV_PMON	0
Bit 2		Unused	X
Bit 1	R	CDRC	0
Bit 0	R	DJAT	0

These registers allow software to determine the block within the corresponding quadrant which produced the interrupt on the INTB output pin.

Reading these registers does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 005H, 045H, 085H, and 0C5H: Diagnostics

Bit	Type	Function	Default
Bit 7	R/W	LCVINS	0
Bit 6		Unused	X
Bit 5	R	AUTO_LLB	X
Bit 4	R/W	RXAISEN	0
Bit 3	R/W	TXAISEN	0
Bit 2	R/W	DIALB	0
Bit 1	R/W	DMLB	0
Bit 0	R/W	LINELB	0

These registers allow software to enable the diagnostic modes on each interface.

LCVINS:

The LCVINS bit introduces a single line code violation on the transmitted data stream. In B8ZS, the violation is generated by masking the first violation pulse of a B8ZS signature. In AMI, one pulse is sent with the same polarity as the previous pulse. In HDB3, the violation is generated by causing the next HDB3-code generated bipolar violation pulse to be of the same polarity as the previous bipolar violation. See the Operations section for details. To generate another violation, this bit must first be written to 0 and then to logic 1 again. At least one bit period should elapse between writing LCVINS 0 and writing it 1 again, or vice versa, if an error is to be successfully inserted. LCVINS has no effect when TDUAL is set to logic 1.

AUTO_LLB:

When this bit is set, it indicates that the quadrant has been placed in line loopback mode due to the reception of an inband loopback code while AUTO_LLB_EN was set. AUTO_LLB is cleared when the quadrant is taken out of line loopback mode by the reception of an inband loopback deactivate code, or when AUTO_LLB_EN for that quadrant is set to logic 0. Line loopback should not be enabled in the QDSX unless DJAT is enabled in the transmit path.

RXAISEN:

When RXAISEN is set to logic 1, an AIS is presented on the RDD/RDP[X] and RDN[X] outputs. When RDD[X] is enabled, RDD[X] will be held always high. If RDP[X] and RDN[X] are enabled, an alternating ones pattern (i.e. a sequence of AMI coded ones) will be presented on RDP and RDN. Note that the RDPINV and RDNINV bits will invert the inserted AIS signal in the same way as other data. When RXAISEN is set to logic 0, RDD/RDP[X] and RDN[X] carry data normally.

TXAISEN:

When the TXAISEN bit is set to logic one, an AIS signal is inserted on TXTIP[X] and TXRING. This AIS signal consists of an AMI-encoded all-ones sequence. When TXAIS is set to logic zero, TXTIP[X] and TXRING[X] carry data as normal.

DIALB:

The DIALB bit selects the diagnostic digital loopback mode, where the transmit data stream is connected to the receive data stream. When DIALB is set to logic 1, the diagnostic digital loopback mode is enabled. When DIALB is set to logic 0, the diagnostic digital loopback mode is disabled.

DMLB:

The DMLB bit enables the diagnostic metallic loopback mode, where the digital, RZ positive and negative sliced versions of the analog signals output on the TXTIP[X] and TXRING[X] pins from XPLS are internally connected to the receive positive and negative pulse inputs of CDRC. When DMLB is set to logic 1, the diagnostic metallic loopback mode is enabled. When DMLB is set to logic 0, the diagnostic metallic loopback mode is disabled. Because diagnostic metallic loopback is essentially a zero-line-length loopback, the 0’-110’ line build out should be selected when using DMLB in T1 operation.

LINELB:

The LINELB bit selects the line loopback mode, where the data input on RXTIP[X] and RXRING[X] is passed through the CDRC and then through DJAT before being retransmitted on TXTIP[X] and TXRING[X] respectively. When LINELB is set to logic 1, the line loopback mode is enabled. When LINELB is set to logic 0, line loopback mode is disabled. Line loopback should not be enabled in the QDSX unless DJAT is enabled in the transmit path.

Register 006H or 106H: Master Test

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	A_TM[7]	X
Bit 5	R/W	A_TM[6]	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable QDSX test features. All bits, except PMCTST and A_TM[7:6] are reset to zero by a hardware reset of the QDSX.

Register 006H and 106H access the same register. The "mirroring" of this register to the two register spaces is done to ensure access to this register is available if the A[8] address pin is tied to logic 1 or 0.

Reserved:

This bit must be set to logic 0 for proper normal mode operation.

Eng: HWTST:

A_TM[6]:

The state of the A_TM[6] bit internally replaces the input address line A[6] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

PMCTST:

The PMCTST bit is used to configure the QDSX for PMC's manufacturing tests. When PMCTST is set to logic one, the QDSX microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high (IOTST must be set to logic 1 since CSB high resets PMCTST) causes the QDSX to drive the data bus and holding the CSB pin low tristates the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the QDSX for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequentially the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section). The IOTST bit is also used in conjunction with the HWTST bit as described below.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tristate modes of the QDSX. While the HIZIO bit is a logic one, all output pins of the QDSX except the data bus and output TDO are held tristate. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

Register 007H: Revision/Chip ID/Global Monitoring Update

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TIP	X
Bit 5	R	TYPE	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

RESET:

The RESET bit allows software to asynchronously reset the QDSX. The software reset is equivalent to setting the RSTB input pin low. When a logic 1 is written to RESET, the QDSX is reset. When a logic 0 is written to RESET, the reset is removed. The RESET bit must be explicitly set and cleared by writing the corresponding logic value to this register.

TIP:

The TIP bit is set to a logic one when any value with Bit 7 set to logic 0 is written to this register. Such a write initiates an accumulation interval transfer and loads all the performance meter registers in the LCV_PMON and PRSM blocks. TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

TYPE:

The chip identification TYPE bit is set at a logic 0.

ID[4:0]:

The ID[4:0] bits allows software to identify the version level of the device.

Register 008H: Interrupt Quadrant ID

Bit	Type	Function	Default
Bit 7	R	INT[4]	0
Bit 6	R	INT[3]	0
Bit 5	R	INT[2]	0
Bit 4	R	INT[1]	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides interrupt identification to show which quadrant of the QDSX asserted the INTB output.

INT[4], INT[3], INT[2], INT[1]:

The INT[X] bit will be high if the xth QDSX interface causes the INTB pin to transition low.

Register 009H: TOPS Master Clock Configuration/Clock Activity Monitor

Bit	Type	Function	Default
Bit 7	R	TCLKIA[4]	X
Bit 6	R	TCLKIA[3]	X
Bit 5	R	TCLKIA[2]	X
Bit 4	R	TCLKIA[1]	X
Bit 3	R	XCLKA	X
Bit 2	R	CLKO8XA	X
Bit 1	R/W	XSEL[1]	0
Bit 0	R/W	XSEL[0]	0

This register provides activity monitoring on QDSX clock inputs and configures the QDSX for the appropriate XCLK input. Figure 12 illustrates the different timing configurations.

TCLKIA[4],TCLKIA[3],TCLKIA[2],TCLKIA[1]:

The TCLKIA[4:1] bits monitors for low to high transitions on the TCLKI[4:1] inputs respectively. TCLKIA[X] is set high on a rising edge of TCLKI[X], and is set low when this register is read.

XCLKA:

The XCLKA bit monitors for low to high transitions on the XCLK input. XCLKA is set high on a rising edge of XCLK, and is set low when this register is read.

CLKO8XA:

The CLKO8XA bit monitors for low to high transitions on the CLKO8X output. CLKO8XA is set high on a rising edge of CLKO8X, and is set low when this register is read.

XSEL[1:0]:

The XSEL[1:0] bits configures the QDSX for the desired XCLK input and for the CLKO8X/CLK01X output according to the following table:

XSEL[1]	XSEL[0]	XCLK Requirements	CLKO8X/CLK01X Output
0	0	24X input clock	DJAT smoothed 8X output clock
0	1	24X input clock	XCLK ÷ 3
1	0	8X input clock	XCLK ÷ 8 (CLKO1X)
1	1	Reserved	Reserved

Register 00AH, 04AH, 08AH, and 0CAH: TOPS Clock Timing Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	FIFOBYP	0
Bit 1	R/W	PLLREF[1]	0
Bit 0	R/W	PLLREF[0]	0

This register is used to configure the timing options for the corresponding QDSX quadrant. Figure 12 illustrates the different timing configurations.

FIFOBYP:

The FIFOBYP bit enables the transmit input signals to DJAT to be bypassed around the FIFO to the outputs. When FIFOBYP is set to logic 1, the inputs to DJAT are routed around the FIFO to the outputs. When FIFOBYP is set to logic 0, the transmit data passes through the DJAT FIFO. When the DJATTX bit (registers 002H, 042H, 082H, and 0C2H) is set to logic 0, the FIFO is automatically bypassed on the transmit path. Whenever the FIFO is not active in the transmit path, the system 8X clock (presented on CLK08X) must be synchronous to TCLKI[X], and line loopback cannot be used. Refer to the Operations section for more details on using the QDSX without the DJAT enabled in the transmit path.

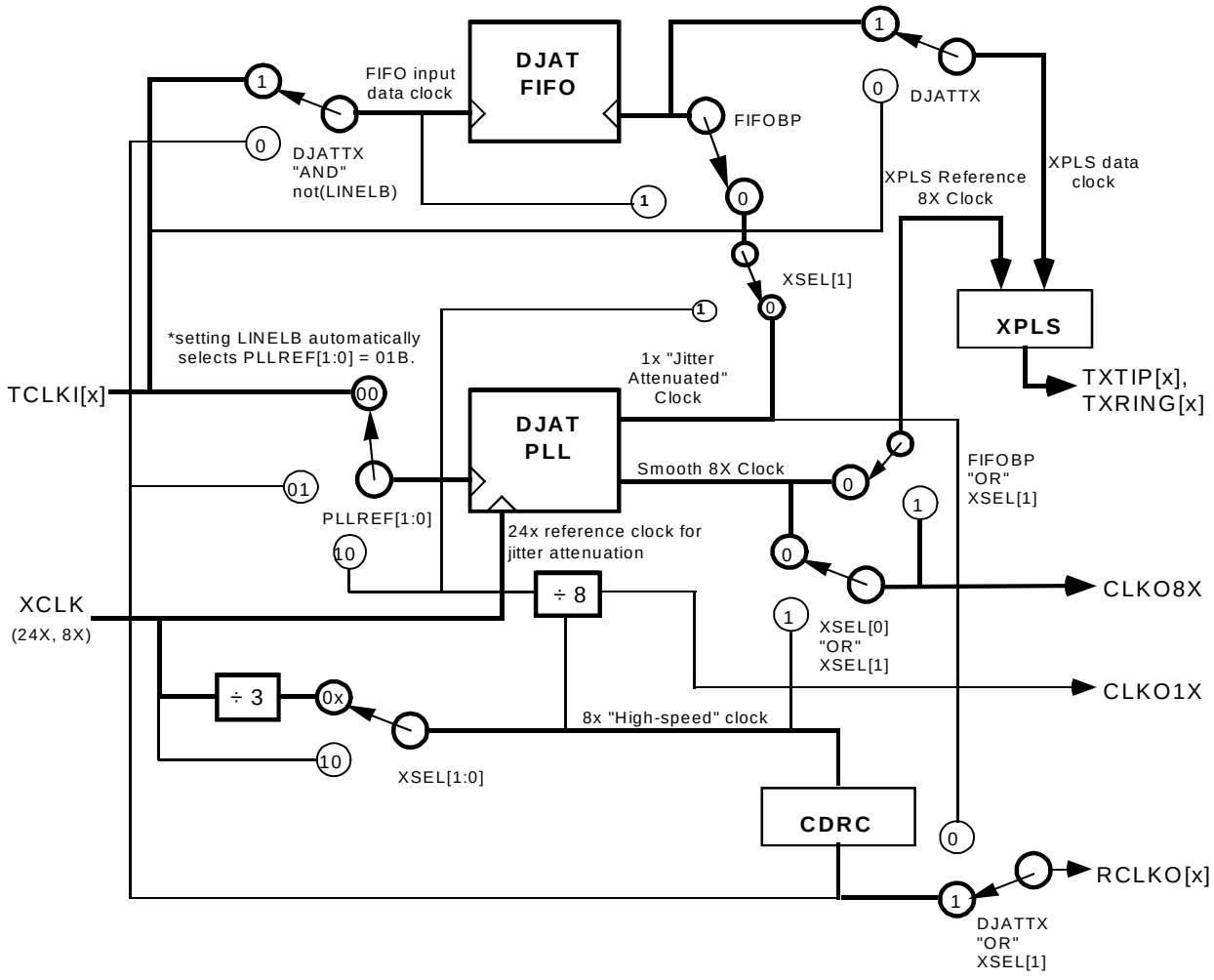
PLLREF[1:0]:

The PLLREF[1:0] bits select the source of the Digital Jitter Attenuator phase locked loop reference signal as follows:

PLLREF[1]	PLLREF[0]	Transmit Reference Source
0	0	TCLKI[X] input.
0	1	Clock recovered from the RXTIP[X] and RXRING[X] inputs.

PLLREF[1]	PLLREF[0]	Transmit Reference Source
1	0	XCLK input divided by 24. XSEL[1] must be set to 0 if this option is selected. (register 009H)
1	1	Reserved. Not to be used.

Figure 17 - Timing Options



Note:

The CLKO8X and CLKO1X outputs are generated from the first quadrant of the device.

Register 00BH, 04BH, 08BH, and 0CBH: LCODE Transmit Line Code Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AMI	0

AMI:

The AMI bit enables AMI line coding. If AMI is set to a logic 1, the QDSX will perform AMI line encoding on the TDD[X] single-rail input data stream. If AMI is set to a logic 0, the QDSX will perform B8ZS (if the CEPT bit in register 001H, 041H, 081H, and 0C1H is set to logic 0) or HDB3 (if the CEPT bit is set to logic 1) line encoding on the TDD[X] single-rail input data stream. The AMI bit has no function if the TDUAL bit in the Transmit Configuration register (001H, 041H, 081H, and 0C1H) or if the TDUAL input pin is set to logic 1.

Register 010H, 050H, 090H, and 0D0H: CDRC Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6	R/W	LOS[1]	0
Bit 5	R/W	LOS[0]	0
Bit 4	R/W	DCR	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ALGSEL	0
Bit 1	R/W	O162	0
Bit 0	R/W	Reserved	0

Reserved:

The reserved bits must be programmed with a logic 0

AMI:

The alternate mark inversion (AMI) bit selects the line code of the incoming E1 or DS1 signal. A logic 1 selects AMI line code; a logic 0 selects HDB3 (E1 format) or B8ZS (DSX-1 format).

LOS[1:0]:

The LOS[1:0] bits select the loss of signal declaration threshold. For example, if the threshold is set to 10, the 11th consecutive zero causes the declaration of LOS. LOS is removed when a single non-zero pulse is detected in the receive stream. The LOS declaration thresholds are shown in the table below:

LOS[1]	LOS[0]	Threshold (bit periods)
0	0	10 (E1 format selected) 15 (DSX-1 format or AMI line code selected)
0	1	31
1	0	63
1	1	175

DCR:

The disable clock recovery (DCR) bit is logically "ORed" with the DCR input pin. DCR enables the sliced positive and negative pulses from the analog receive slicer to be visible on the SDP[X] and SDN[X] outputs. When DCR is set to logic 1, the SDP[X] and SDN[X] outputs are enabled. When DCR is set to logic 0, either the RDP[X] and RDN[X] or the RDD[X] and RLCV[X] outputs are enabled depending on the setting of the RDUAL bit in the Receive Configuration register (000H, 040H, 080H, and 0C0H). Note that the DCR bit takes precedence over the RDUAL bit.

ALGSEL:

The Algorithm Select (ALGSEL) bit specifies the algorithm used by the DPLL for clock and data recovery. The choice of algorithm determines the high frequency input jitter tolerance of the CDRC. When ALGSEL is set to logic 1, the CDRC jitter tolerance is increased to approach 0.5UIpp for jitter frequencies above 20KHz. When ALGSEL is set to logic 0, the jitter tolerance is increased for frequencies below 20KHz (i.e. the tolerance is improved by 20% over that of ALGSEL=1 at these frequencies), but the tolerance approaches 0.4UIpp at the higher frequencies.

O162:

When the E1 format is selected and the AMI bit is logic 0, the Recommendation O.162 compatibility select bit (O162) allows selection between two line code definitions:

1. If O162 is a logic 0, a line code violation is indicated if the serial stream does not match the verbatim HDB3 definition given in Recommendation G.703. A bipolar violation that is not part of an HDB3 signature or a bipolar violation in an HDB3 signature that is the same polarity as the last bipolar violation results in a line code violation indication.

2. If O162 is a logic 1, a line code violation is indicated by a LCV output pulse if a bipolar violation is of the same polarity as the last bipolar violation, as per Recommendation O.162.

Registers 011H, 051H, 091H and 0D1H: CDRC Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LCVE	0
Bit 6	R/W	LOSE	0
Bit 5	R/W	LCSDE	0
Bit 4	R/W	EXZE	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The bit positions LCVE, LOSE, LCSDE and EXZE of this register are interrupt enables to select which of the status events (Line Code Violation , Loss Of Signal, B8ZS/HDB3 Signature Detection, or Excessive Zeros Detection), either individually or in combination, are enabled to generate an interrupt on the INTB pin when they are detected. A logic 1 bit in the corresponding bit position enables the detection of these signals to generate an interrupt; a logic 0 bit in the corresponding bit position disables that signal from generating an interrupt.

Registers 012H, 052H, 092H and 0D2H: CDRC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	LCVI	X
Bit 6	R	LOSI	X
Bit 5	R	LCSDI	X
Bit 4	R	EXZI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOS	X

The bit positions LCVI, LOSI, LCSDI and EXZI of this register indicate which of the status events generated an interrupt. A logic 1 in these bit positions indicate that the corresponding event was detected; a logic 0 in these bit positions indicate that no corresponding event has been detected. The bit positions LCVI, LCSDI and EXZI are set on the assertion of a line code violation, a line code signature detection, and excessive zeros detection, respectively. LOSI is set on a change of state of the LOS alarm. Bits LCVI, LOSI, LCSDI and EXZI are cleared by reading this register. The current state of the LOS alarm can be determined by reading bit 0 of this register.

Note:

In the CDRC, excess zeros is defined as a string greater than: 3 consecutive zeros for E1 data, or 7 consecutive zeros for T1 data.

Register 014H, 054H, 094H, and 0D4H: LCV_PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INT	X
Bit 0	R	OVR	X

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt. A logic 0 bit in the INTE position disables the generation of an interrupt.

INT:

The INT bit is the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer has occurred. A logic 0 indicates that no transfer has occurred. The interrupt is cleared (acknowledged) by reading this register.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

Registers 01AH-01BH, 05AH-05BH, 09AH-09BH, 0DAH-0DBH: Latching LCV Performance Data

The LCV Performance Data registers for one of the four interfaces on the QDSX are updated as a group by writing to any of the LCV_PMON count registers (addresses 01AH-01BH, 05AH-05BH, 09AH-09BH, 0DAH-0DBH). A write to any of these locations loads performance data located in the LCV_PMON block of that quadrant into the internal holding registers. The data contained in the holding registers can then be subsequently read by microprocessor accesses of the LCV_PMON LCV Count registers. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed. NOTE: it is necessary to write to one, and only one, count register address to latch all the count data register values into the holding registers and to reset all the counters of the particular quadrant for each polling cycle.

Alternately, one may write to the Global Monitoring Update register (009H) to transfer the contents of all four LCV_PMON counters and the PRSM counters. The transfer in progress (TIP) bit in register 007H is polled to determine when the transfer is complete.

Registers 01AH, 05AH, 09AH and 0DAH: LCV_PMON Line Code Violation Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Registers 01BH, 05BH, 09BH and 0DBH: LCV_PMON Line Code Violation Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

These registers indicate the number of LCV error events that occurred during the previous accumulation interval. An LCV event is defined as the occurrence of a Bipolar Violation or Excessive Zeros. The counting of Excessive Zeros (a string of greater than: 3 consecutive zeros for E1 data, 7 consecutive zeros for B8ZS, or 15 consecutive zeros for T1 AMI) can be disabled by the BPVCNT bit of the Receive Configuration register (000H, 040H, 080H, and 0C0H).

Registers 01CH, 05CH, 09CH and 0DCH: DJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	X
Bit 0	R	UNDI	X

These registers contain the indication of the DJAT FIFO status.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the FIFO when the FIFO is already full. When UNDI is a logic 1, an overrun event has occurred.

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred.

Register 01DH, 05DH, 09DH and 0DDH: DJAT Reference Clock Divisor (N1) Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

These registers define an 8-bit binary number, N1, which is one less than the magnitude of the divisor used to scale down the DJAT PLL reference clock input. The REF divisor magnitude, (N1+1), is the ratio between the frequency of REF input and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit in the DJAT Configuration register is high, will also reset the FIFO.

Registers 01EH, 05EH, 09EH and 0DEH: DJAT Output Clock Divisor (N2) Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

These registers define an 8-bit binary number, N2, which is one less than the magnitude of the divisor used to scale down the DJAT smooth output clock signal. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit is high, will also reset the FIFO.

Registers 01FH, 05FH, 09FH and 0DFH: DJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	WIDEN	1
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	SYNC	1
Bit 0	R/W	LIMIT	1

These registers control the operation of the DJAT FIFO read and write pointers and controls the generation of interrupt by the FIFO status.

WIDEN:

The WIDEN bit controls the width of the generated pulse from the XPLS block. When WIDEN is set to logic 1, the high phase of one cycle of the 8X clock generated by the DJAT PLL is modified to be nominally one 24X clock period wider. This results in the XPLS producing a greater pulse width. When WIDEN is set to logic 0, the smooth 8X clock from DJAT is not modified, resulting in pulses of minimum allowable width (approx. 50% duty cycle). These narrow pulses reduce the amount of energy sourced by the QDSX into the line. The WIDEN bit has no effect when the DJAT PLL is not used.

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, then the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions. CENT can only be set to logic 1 if SYNC is set to logic 0.

OVRE,UNDE:

The OVRE and UNDE bits control the generation of an interrupt on the microprocessor INTB pin when a FIFO error event occurs. When OVRE or UNDE is set to logic 1, an overrun event or underrun event, respectively, is allowed to generate an interrupt on the INTB pin. When OVRE or UNDE is set to logic 0, the FIFO error events are disabled from generating an interrupt.

SYNC:

The SYNC bit enables the PLL to synchronize the phase delay between the FIFO input and output data to the phase delay between reference clock input and smooth output clock at the PLL. For example, if the PLL is operating so that the smooth output clock lags the reference clock by 24 UI, then the synchronization pulses that the PLL sends to the FIFO will force its output data to lag its input data by 24 UI.

LIMIT:

The LIMIT bit enables the PLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one unit interval (UI) of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 1, the PLL jitter attenuation is limited. When LIMIT is set to logic 0, the PLL is allowed to operate normally.

Registers 020H, 060H, 0A0H and 0E0H: IBCD Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	DSEL1	0
Bit 2	R/W	DSEL0	0
Bit 1	R/W	ASEL1	0
Bit 0	R/W	ASEL0	0

These registers provide the selection of the Activate and De-activate T1 loopback code lengths (from 3 bits to 8 bits) as follows:

Table 4 -

DEACTIVATE Code		ACTIVATE Code		CODE LENGTH
DSEL1	DSEL0	ASEL1	ASEL0	
0	0	0	0	5 bits
0	1	0	1	6 (or 3*) bits
1	0	1	0	7 bits
1	1	1	1	8 (or 4*) bits

***Note:**

3 and 4 bit code sequences can be accommodated by configuring the IBCD for 6 or 8 bits and by programming two repetitions of the code sequence.

Reserved:

The reserved bit must be programmed to logic 0 for correct operation.

Registers 021H, 061H, 0A1H and 0E1H: IBCD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R	LBACP	X
Bit 6	R	LBDCP	X
Bit 5	R/W	LBAE	0
Bit 4	R/W	LBDE	0
Bit 3	R	LBAI	X
Bit 2	R	LBDI	X
Bit 1	R	LBA	X
Bit 0	R	LBD	X

LBACP,LBDCP:

The LBACP and LBDCP bits indicate when the corresponding loopback code is present during a 39.8 ms interval (DSX-1 applications).

LBAE:

The LBAE bit enables the assertion or deassertion of the inband Loopback Activate (LBA) detect indication to generate an interrupt on the INTB pin. When LBAE is set to logic 1, any change in the state of the LBA detect indication generates an interrupt. When LBAE is set to logic 0, no interrupt is generated by changes in the LBA detect state.

LBDE:

The LBDE bit enables the assertion or deassertion of the inband Loopback Deactivate (LBD) detect indication to generate an interrupt on the INTB pin. When LBDE is set to logic 1, any change in the state of the LBD detect indication generates an interrupt. When LBDE is set to logic 0, no interrupt is generated by changes in the LBD detect state.

LBAI,LBDI:

The LBAI and LBDI bits indicate which of the two expected loopback codes has changed state. A logic 1 in these bit positions indicate that a state change in that code has occurred; a logic 0 in these bit positions indicate that no state change has occurred.

LBA,LBD:

The LBA and LBD bits indicate the current state of the corresponding loopback code detect indication. A logic 1 in these bit positions indicate the presence of that code has been detected; a logic 0 in these bit positions indicate the absence of that code.

Registers 022H, 062H, 0A2H and 0E2H: IBCD Activate Code

Bit	Type	Function	Default
Bit 7	R/W	ACT7	0
Bit 6	R/W	ACT6	0
Bit 5	R/W	ACT5	0
Bit 4	R/W	ACT4	0
Bit 3	R/W	ACT3	0
Bit 2	R/W	ACT2	0
Bit 1	R/W	ACT1	0
Bit 0	R/W	ACT0	0

This 8 bit register selects the Activate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8 bit register. For example, if code sequence is a repeating 00001, then the first 8 bits of two repetitions (0000100001) is programmed into the register (i.e. 00001000). Note that bit ACT7 corresponds to the first code bit received.

Registers 023H, 063H, 0A3H and 0E3H: IBCD Deactivate Code

Bit	Type	Function	Default
Bit 7	R/W	DACT7	0
Bit 6	R/W	DACT6	0
Bit 5	R/W	DACT5	0
Bit 4	R/W	DACT4	0
Bit 3	R/W	DACT3	0
Bit 2	R/W	DACT2	0
Bit 1	R/W	DACT1	0
Bit 0	R/W	DACT0	0

This 8 bit register selects the Deactivate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8 bit register. For example, if code sequence is a repeating 001, then the first 8 bits of three repetitions (001001001) is programmed into the register (i.e. 00100100). Note that bit DACT7 corresponds to the first code bit received.

Registers 024H, 064H, 0A4H and 0E4H: XIBC Control

Bit	Type	Function	Default
Bit 7	R/W	EN	0
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	CL1	0
Bit 0	R/W	CL0	0

These registers control the transmission of T1 inband loopback activate and deactivate codes.

EN:

The EN bit controls whether the inband code is transmitted or not. A logic 1 in the EN bit position enables transmission of inband codes; a logic 0 in the EN bit position disables inband code transmission.

Reserved:

This bit is reserved and should be set to logic 0 for proper operation.

CL1, CL0:

The bit positions CL[1:0] (bits 1 & 0) of this register indicate the length of the inband loopback code sequence, as follows:

CL1	CL0	Code Length
0	**0**	**5**
0	**1**	**6**
1	**0**	**7**
1	**1**	**8**

Codes of 3 or 4 bits in length may be accommodated by treating them as half of a double-sized code (i.e. a 3-bit code would use the 6-bit code length setting).

Registers 025H, 065H, 0A5H and 0E5H: XIBC Loopback Code

Bit	Type	Function	Default
Bit 7	R/W	IBC7	X
Bit 6	R/W	IBC6	X
Bit 5	R/W	IBC5	X
Bit 4	R/W	IBC4	X
Bit 3	R/W	IBC3	X
Bit 2	R/W	IBC2	X
Bit 1	R/W	IBC1	X
Bit 0	R/W	IBC0	X

These registers contain the inband loopback code pattern to be transmitted. The code is transmitted most significant bit (IBC7) first, followed by IBC6 and so on. The code, regardless of the length, must be aligned with the MSB always in the IBC7 position (a 5-bit code would occupy the IBC7 through IBC2 bit positions). To transmit a 3-bit or a 4-bit code pattern, the pattern must be paired to form a double-sized code (the 3-bit code '011' would be written as the 6-bit code '011011').

Register 027H, 067H, 0A7H, 0E7H: PRSG Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	PRBSINV	0
Bit 1	R/W	PRBSERR	0
Bit 0	R/W	PRBSGEN	0

This register enables the PRSG pseudo-random bit sequence generation.

PRBSINV:

When the PRBSINV bit is set, the PRSG block inverts the 2^{15}-1 PRBS data before transmission. An inverted 2^{15}-1 PRBS will contain at most 15 consecutive zeroes, while a non-inverted 2^{15}-1 PRBS will contain at most 14 consecutive zeroes. Some testers may only support the inverted sequence.

PRBSGEN:

The PRBSGEN bit enables the PRSG block to insert the 2^{15}-1 PRBS data stream into the transmit data stream. When PRBSGEN is set to logic 1, the PRSG block will overwrite the data stream with the PRBS data stream. When PRBSGEN is set to logic 0, the PRBS generation is disabled.

PRBSERR:

When the PRBSERR bit is written with a logic 1, a single error is inserted in the pseudo-random bit stream by inverting a single bit. To insert another bit error, the PRBSERR bit must be written with a logic 0, and then re-written with another logic 1. At least one bit period should elapse between writing PRBSERR 0 and writing it 1 again, or vice versa, if an error is to be successfully inserted. PRBSERR has no effect when PRBSGEN is set to 0.

Register 029H, 069H, 0A9H, 0E9H: PRSM Control/Status

Bit	Type	Function	Default
Bit 7	R/W	PRBSINV	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	OOSE	0
Bit 4	R	OOSI	X
Bit 3	R	OOS	X
Bit 2	R/W	INTE	0
Bit 1	R	INT	X
Bit 0	R	OVR	X

This register shows the PRBS monitor synchronization state and enables an interrupt to be generated whenever synchronization is lost or regained. This register also enables an interrupt to be generated whenever the PRBS error counter data is transferred into the PRSM holding registers. The configuration register also contains status information as to whether these holding registers have been overrun.

PRBSINV:

When the PRBSINV bit is set, the PRSM inverts the incoming data. This will allow it to synchronize to an inverted pseudorandom bit sequence. In the default setting, the PRSM synchronizes to a non-inverted sequence. An inverted 2^{15}-1 PRBS will contain at most 15 consecutive zeroes, while a non-inverted 2^{15}-1 PRBS will contain at most 14 consecutive zeroes. Some testers may only support the inverted sequence.

Reserved:

The Reserved bit must be programmed to logic 0 for proper operation.

OOSE:

The OOSE bit controls the generation of a microprocessor interrupt when a change of PRBS synchronization state occurs A logic 1 bit in the OOSE position enables the generation of an interrupt; a logic 0 bit in the OOSE position disables the generation of an interrupt. The interrupt is cleared by reading this register.

OOSI:

The OOSI bit shows the current status of the interrupt signal. A logic 1 in this bit position indicates that a change in PRBS synchronization state has occurred. A logic 0 indicates that no change in PRBS synchronization state has occurred. The OOSI bit is cleared following a read of this register.

OOS:

The OOS bit indicates the current PRBS synchronization status of the PRSM block. A logic 1 in this bit position indicates that the PRSM block is out of sync. When out of sync, bit error events are not accumulated. A logic 0 indicates that the PRSM block is synchronized and accumulating bit error events.

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt; a logic 0 bit in the INTE position disables the generation of an interrupt. The interrupt is cleared (acknowledged) by reading this register.

INT:

The INT bit is the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer has occurred. A logic 0 indicates that no transfer has occurred. The INT bit is cleared following a read of this register.

OVR:

The OVR bit holds the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

Latching Performance Data

The Pseudo-Random Sequence Monitor (PRSM) holding registers (02AH-02BH, 06AH-06BH, 0AAH-0ABH, and 0EAH-0EBH) are updated by a microprocessor write to either of the particular PRSM's holding registers. The PRSM block is loaded with new performance data within 4 clock periods (RCLKO[X] if in the receive path, TCLKI[X] if in the transmit path) after the write. Thus, the PRSM holding registers should not be read until after 2 µs (E1 case) or 2.6 µs (DSX-1 case) has elapsed since the write was completed. Alternatively, the PRSM Control/Status register may be polled until the INT bit goes to logic 1, indicating

that the transfer is complete and the data is ready to be read. The data contained in the holding registers can subsequently be read by the microprocessor. The loading is synchronized to the internal event timing so that no events are missed.

Alternately, one may write to the Global Monitoring Update register (009H) to transfer the contents of the PRSM counters as well as the LCV_PMON registers of all four quadrants. The transfer in progress (TIP) bit in register 007H is polled to determine when the transfer is complete.

Register 02AH, 06AH, 0AAH, 0EAH: PRSM Bit Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	BER[7]	X
Bit 6	R	BER[6]	X
Bit 5	R	BER[5]	X
Bit 4	R	BER[4]	X
Bit 3	R	BER[3]	X
Bit 2	R	BER[2]	X
Bit 1	R	BER[1]	X
Bit 0	R	BER[0]	X

Register 02BH, 06BH, 0ABH, 0EBH: PRSM Bit Error Event Count MSB

Bit	Type	Function	Default
Bit 7	R	BER[15]	X
Bit 6	R	BER[14]	X
Bit 5	R	BER[13]	X
Bit 4	R	BER[12]	X
Bit 3	R	BER[11]	X
Bit 2	R	BER[10]	X
Bit 1	R	BER[9]	X
Bit 0	R	BER[8]	X

These holding registers indicate the number of bit error events that occurred during the previous accumulation interval. The contents of these registers are valid 2 µs after a transfer is triggered by a write to any one of the PMON's holding register addresses, or to register 007H.

Register 02CH, 06CH, 0ACH, 0ECH: XPLS Line Length Configuration

Bit	Type	Function	Default
Bit 7	R/W	RPT	0
Bit 6	R/W	Reserved	0
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register allows software to select the length of cable that XPLS is required to drive and to enable generation of user-programmable output templates.

RPT:

The RPT bit enables the 4-bit DAC codes contained in the Programmable Template CODE registers to generate the output waveform. When RPT is set to a logic 1, the internal user-programmable XPLS CODE registers supply the DAC codes used to generate the waveform. RPT must be set to logic 1 and the desired template codes programmed for correct output pulse generation. The Operations section contains the required details for programming the templates.

SM:

Reserved

The reserved bits must be programmed to logic 0 for correct operation.

ILS[2:0]:

Register 02DH, 06DH, 0ADH, 0EDH: XPLS Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	TAIS	0
Bit 2	R	DPMV	X
Bit 1	R	DPMI	X
Bit 0	R/W	DPME	0

TAIS:

The TAIS bit enables the XPLS to generate an unframed all-ones AIS alarm on the TXTIP[X] and TXRING[X] output pins. When TAIS is set to logic 1, the outputs are forced to pulse alternately, creating an all-ones signal. When TAIS is set to logic 0, the outputs operate normally. The transition to transmitting AIS is done in such a way as to not introduce any bipolar violations.

DPMV:

The DPMV bit reflects the current state of the DPM alarm signal.

DPMI:

The DPMI bit is set to logic 1 when any change of state occurs on the Driver Performance Monitor (DPM) alarm signal. This bit is cleared when the register is read.

DPME:

The DPME bit controls the generation of an interrupt on the microprocessor INTB pin by the driver performance monitor portion of XPLS. When DPME is set to logic 1, an interrupt is generated on INTB whenever an alarm condition occurs on the driver performance monitor points. A driver performance monitor alarm is declared whenever a period of 62 or 63 consecutive bit periods with no pulses on either the TXTIP[x] or TXRING[x] output pins occurs. The exact threshold (62 or 63 bit periods) depends on the line build-out and the pattern of bipolar violations. When DPME is set to logic 0, detection of a driver performance monitor alarm condition is disabled from generating an interrupt.

Register 02EH, 06EH, 0AEH, 0EEH: XPLS CODE Indirect Address

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	CRA2	0
Bit 1	R/W	CRA1	0
Bit 0	R/W	CRA0	0

This register allows software to select any one of the eight internal waveform CODE registers, addressed by the CRA[2:0] bits, for subsequent access through the CODE Indirect Data register. When accessing the internal CODE registers, the address of the desired register must first be written to this register. Then, by reading or writing the Indirect Data register (registers 2FH, 06FH, 0AFH, 0EFH), the microprocessor can either read from or write to the internal register identified by the CRA[2:0] bits.

The CRA[2:0] bits address the internal registers as follows:

CRA2	CRA1	CRA0	Internal Code Register
0	0	0	CODE register #0 - first code applied
0	0	1	CODE register #1
0	1	0	CODE register #2
0	1	1	CODE register #3
1	0	0	CODE register #4
1	0	1	CODE register #5
1	1	0	CODE register #6
1	1	1	CODE register #7 - last code applied

See the Operations section for more details on setting up custom waveform templates.

Register 02FH, 06FH, 0AFH, 0EFH: XPLS CODE Indirect Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	CRD3	0
Bit 2	R/W	CRD2	0
Bit 1	R/W	CRD1	0
Bit 0	R/W	CRD0	0

This register allows software to access the contents of any one of the eight internal waveform CODE registers, addressed by the CRA[2:0] bits in the CODE Indirect Address register. When accessing the internal CODE registers, the address of the desired register must first be written to the Indirect Address register (registers 2EH, 06EH, 0AEH, 0EEH). Then, by reading or writing the Indirect Data register, the microprocessor can either read from or write to the internal register identified by the CRA[2:0] bits.

The value read from or written to the internal CODE registers is contained in the CRD[3:0] bits. CRD3 is the most significant bit.

See the Operations section for more details on setting up custom waveform templates.

Register 030H, 070H, 0B0H, 0F0H: RSLC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	THS	0

THS:

The bit THS controls the selection of slicing threshold. The analog pulse slicer generates a logic one on either the SDP or SDN output if the amplitude (positive or negative) of the line voltage exceeds the adaptive slicing threshold. The THS bit selects between two fractions of the pulse amplitude for the slicing threshold.

When THS is set to logic 0, the slicing threshold is 67% of the peak amplitude and is intended for DSX-1 applications.

When THS is set to logic 1, the slicing threshold is 50% of the peak amplitude and is intended for G.703 2048 kbit/s applications.

The THS bit is internally ORed with the CEPT bit in the Receive Configuration Register (Registers 000H, 040H, 080H, 0C0H).

Register 031H, 071H, 0B1H, 0F1H: RSLC Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	SQ	X
Bit 1	R	SQI	X
Bit 0	R/W	SQE	0

SQ:

The SQ bit reflects the current state of the squelch alarm.

SQI:

The SQI bit is set to logic 1 when a change in the state of the squelch alarm occurs. The bit is cleared to logic 0 when the register is read.

SQE:

The SQE bit enables the generation of an interrupt when the squelch alarm changes state. When SQE is set to logic 1, the squelch alarm event is enabled to generate an interrupt on the microprocessor INTB pin.

When the QDSX is reset, the SQE bit is set to logic 0, disabling a squelch event from generating an interrupt.

11 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the QDSX. Test mode registers (as opposed to normal mode registers) are selected when A[8] is high.

Test mode registers may also be used for board testing. When all of the TSBs within the QDSX are placed in test mode 0, device digital inputs may be read and outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

In addition, the QDSX also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 5 - Test Mode Register Memory Map

Address	Register
000H-0FFH	Normal Mode Registers
006H or 106H	Master Test Register
100H-10FH	QDSX Test Reserved
110H, 150H, 190H, 1D0H	CDRC Test Register 0
111H, 151H, 191H, 1D1H	CDRC Test Register 1
112H, 152H, 192H, 1D2H	CDRC Test Register 2
113H, 153H, 193H, 1D3H	QDSX Test Reserved
114H, 154H, 194H, 1D4H	LCV_PMON Test Register 0
115H, 155H, 195H, 1D5H	LCV_PMON Test Register 1
116H-11BH, 156H-15BH, 196H-19BH, 1D6H-1DBH	LCV_PMON Test Reserved
11CH, 15CH, 19CH, 1DCH	DJAT Test Register 0
11DH, 15DH, 19DH, 1DDH	DJAT Test Register 1

Address	Register
11EH, 15EH, 19EH, 1DEH	DJAT Test Register 2
11FH, 15FH, 19FH, 1DFH	DJAT Test Reserved
120H, 160H, 1A0H, 1E0H	IBCD Test Register 0
121H, 161H, 1A1H, 1E1H	IBCD Test Register 1
122H-123H, 162H-163H, 1A2H-1A3H, 1E2H-1E3H	IBCD Test Reserved
124H, 164H, 1A4H, 1E4H	XIBC Test Register 0
125H, 165H, 1A5H, 1E5H	XIBC Test Register 1
126H-12BH, 166H-16BH, 1A6H-1ABH, 1E6H-1EBH	QDSX Test Reserved
12CH, 16CH, 1ACH, 1ECH	XPLS Test Register 0
12DH, 16DH, 1ADH, 1EDH	XPLS Test Register 1
12EH, 16EH, 1AEH, 1EEH	XPLS Test Register 2
12FH, 16FH, 1AFH, 1EFH	XPLS Test Register 3
130H, 170H, 1B0H, 1F0H	RSLC Test Register 0
131H, 171H, 1B1H, 1F1H	RSLC Test Register 1

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

11.1 Test Mode 0 Details

In test mode 0, the QDSX allows the logic levels on the digital device inputs to be read through the microprocessor interface and allows the digital device outputs to be forced to either logic level through the microprocessor interface. The IOTST bit in the Master Test register must be set to logic one to access the device I/O.

To enable test mode 0, the IOTST bit in the Master Test register is set to logic one, all normal mode registers should be set to their default state, and the

following addresses must be written with 00H: 111H, 115H, 11DH, 121H, 125H, 129H, 12DH, 131H, 151H, 155H, 15DH, 161H, 165H, 169H, 16DH, 171H, 191H, 195H, 19DH, 1A1H, 1A5H, 1A9H, 1ADH, 1B1H, 1D1H, 1D5H, 1DDH, 1E1H, 1E5H, 1E9H, 1EDH, and 1F1H.

Reading the following address locations returns the values on the indicated inputs:

Table 6 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
110H				DCR				
11CH			TCLKI[1]		XCLK		TDN[1]	TDP[1]
120H								RDUAL
124H								TDUAL
15CH			TCLKI[2]		XCLK		TDN[2]	TDP[2]
19CH			TCLKI[3]		XCLK		TDN[3]	TDP[3]
1DCH			TCLKI[4]		XCLK		TDN[4]	TDP[4]

Writing the following address locations forces the outputs to the value in the corresponding bit position (zeros should be written to all unused test register locations):

Table 7 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
110H		INT[1]						RCLKO[1]
114H								INT[1]
11CH	INT[1]				CLKO8X			
120H						INT[1]		
12CH								INT[1]
130H						RDP[1]	RDN[1]	INT[1]
150H		INT[1]						RCLKO[2]
154H								INT[1]
15CH	INT[1]							
160H						INT[1]		
16CH								INT[1]
170H						RDP[2]	RDN[2]	INT[1]

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
190H		INT[1]						RCLKO[3]
194H								INT[1]
19CH	INT[1]							
1A0H						INT[1]		
1ACH								INT[1]
1B0H						RDP[3]	RDN[3]	INT[1]
1D0H		INT[1]						RCLKO[4]
1D4H								INT[1]
1DCH	INT[1]							
1E0H						INT[1]		
1ECH								INT[1]
1F0H						RDP[4]	RDN[4]	INT[1]

Notes:

1. Writing a logic 1 to any of the block interrupt signals asserts the INTB output low. To deassert INTB, all the INT register bits should be set to logic 0.

11.2 JTAG Test Port

The QDSX JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 8 - Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010

Instructions	Selected Register	Instruction Codes, IR[2:0]
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length - 32 bits

Version number - 0H

Part Number - 4314H

Manufacturer's identification code - 0CDH

Device identification - 043140CDH

Table 9 - Boundary Scan Register (Length - 64 bits)

Pin/Enable	Boundary Scan Register Bit	Pin/Enable	Boundary Scan Register Bit
RSTB[4]	63	RDP[3]	27
ALE	62	RCLKO[2]	26
CSB	61	RDN[2]	25
WRB	60	RDP[2]	24
RDB	59	RCLKO[1]	23
A[0:8]	58 - 50	RDN[1]	22
VDDI[3]	49	RDP[1]	21
DCR	48	RDUAL	20
TDUAL	47	INTB	19
TDN[4]	46	INTB_OEN[1]	18
TDP[4]	45	D[0]	17

Pin/Enable	Boundary Scan Register Bit	Pin/Enable	Boundary Scan Register Bit
TCLKI[4]	44	D0_OEN[1]	16
TDN[3]	43	D[1]	15
TDP[3]	42	D1_OEN[1]	14
TCLKI[3]	41	D[2]	13
TDN[2]	40	D2_OEN[1]	12
TDP[2]	39	D[3]	11
TCLKI[2]	38	D3_OEN[1]	10
TDN[1]	37	D[4]	9
TDP[1]	36	D4_OEN[1]	8
TCLKI[1]	35	D[5]	7
XCLK	34	D5_OEN[1]	6
CLKO8X	33	D[6]	5
RCLKO[4]	32	D6_OEN[1]	4
RDN[4]	31	D[7]	3
RDP[4]	30	D7_OEN[1]	2
RCLKO[3]	29	HIZ[2][2]	1
RDN[3]	28	HIZ[4][3]	0

Note:

1. All OEN signals will set the corresponding bidirectional signal to an output when set low.
2. When set high, RDP[4:1], RDN[4:1], and RCLKO[4:1] will be set to high impedance.
3. When set high, CLKO8X will be set to high impedance.
4. RSTB is the first bit of the boundary scan chain.

12 OPERATIONS

12.1 Programming the XPLS Waveform Template

The internal XPLS CODE registers, at registers 02FH, 06FH, 0AFH, 0EFH, are used to create a custom waveform across the analog transmit outputs, TXTIP[X] and TXRING[X]. These eight CODE registers are accessed indirectly through register 2EH, 06EH, 0AEH, 0EEH and contain 4-bit binary values corresponding to one of 16 quantized levels for the amplitude of the output pulse during each of eight synchronous, "high-speed" clock periods within a data clock cycle. The full swing of the amplifier outputs TXTIP[X] and TXRING[X] ranges from 0 to 4.02 Volts. The codes select the nominal voltage levels into 50Ω as follows:

Table 10 -

CODE	Typical Output Voltage	CODE	Typical Output Voltage
0000	0.05 V	1000	2.16 V
0001	0.31 V	1001	2.43 V
0010	0.58 V	1010	2.70 V
0011	0.85 V	1011	2.97 V
0100	1.16 V	1100	3.23 V
0101	1.38 V	1101	3.49 V
0110	1.65 V	1110	3.76 V
0111	1.91 V	1111	4.02 V

The contents of the CODE registers are used by XPLS and internally applied to the output D/A converter in sequence, beginning with CODE reg. #0, on the first falling edge of the internal, synchronous high-speed clock once the data clock has gone low. The first four codes determine the shape of the bulk of the pulse, whereas the last four codes determine the shape of the tail end of the pulse. Depending on the polarity of the input pulse (either on the positive pulse input or the negative pulse input to XPLS), the bulk of the pulse is generated on either TXTIP[X] or TXRING[X], with the tail generated on TXTIP[X] or TXRING[X], respectively. The pulse is produced differentially across the transformer primary

so that, for example, while the first four codes are generating the pulse on TXTIP[X], TXRING[X] is grounded through the output amplifier. To generate the negative portion of the pulse, the last four codes generate the tail of the pulse on TXTIP[X] while TXRING[X] is grounded through the other output amplifier. The ON-resistance of either TXTIP[X] or TXRING[X] output amplifier is nominally 2.5Ω when acting as a ground for the transformer. The output impedance of the amplifier when driving the pulse is typically <0.5Ω at half the bit rate.

The recommended template waveforms codes are given below. The WIDEN=1 and WIDEN=0 function corresponds to the state of the WIDEN bit in the DJAT Configuration register (01FH, 05FH, 09FH, and 0DFH) if the 24X clock is input to XCLK. Note that if the transmit jitter attenuation function is not enabled (XSEL[1] = 1, or FIFOBYP=1, or DJATTX=0), then the WIDEN=0 configuration is enabled by default.

Table 11 -

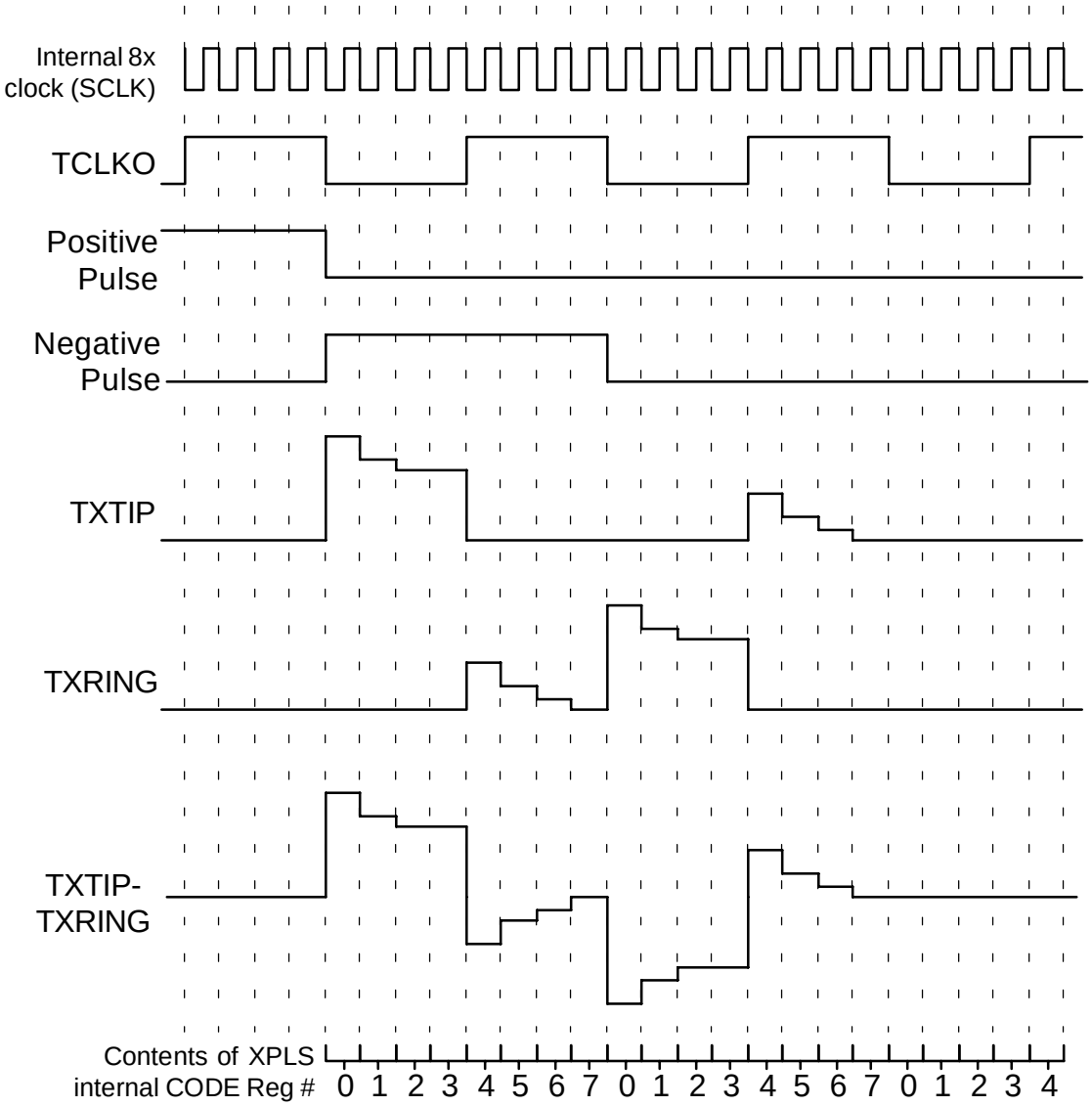
Length Setting (ft.)	**Recommended Code Register Values (WIDEN=1)**							
Register #	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0-110	A	9	9	9	3	2	1	0
110-220	C	B	A	A	4	3	2	1
220-330	E	C	B	B	5	4	2	1
330-440	E	D	B	B	6	5	3	1
440-550	E	B	A	A	7	4	2	1
550-660	F	C	B	A	8	5	3	1
G.703 2048 kbit/s 75 Ω	8	8	8	8	0	0	0	0
G.703 2048 kbit/s 120 Ω	9	9	9	9	0	0	0	0

Table 12 -

Length Setting (ft.)	Recommended Code Register Values (WIDEN=1)							
Register #	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0-110	A	9	9	9	3	2	1	0
110-220	C	A	A	A	3	2	1	0
220-440	D	B	A	A	5	4	2	1
440-660	E	B	A	9	7	4	2	1
G.703 2048 kbit/s 75 Ω	8	8	8	8	0	0	0	0
G.703 2048 kbit/s 120 Ω	9	9	9	9	0	0	0	0

Figure 18 shows the relationship between the data clock (TCLKO[X]), the internal synchronous, high-speed clock SCLK timing, and the application of the CODE register contents for a positive pulse immediately followed by a negative pulse. The resultant waveform across TXTIP[X] and TXRING[X] is also shown.

Figure 18 - CODE Register Sequence During Pulse Generation

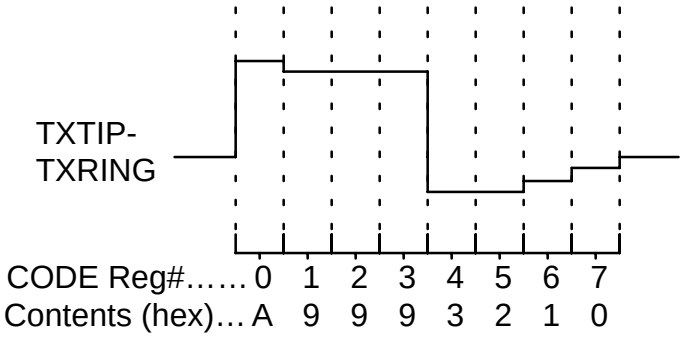


The actual waveform produced at the transformer secondary depends upon the turns ratio of the transformer used, the series resistance on the primary side used to match the line, the output impedance of the amplifier, the on-resistance of the amplifier while providing the transformer ground, and the transformer winding resistance. To ensure that the amplifiers can drive the reflected load, it is recommended that a transformer have a turns ratio of no more than 1:2. It is also recommended that the codes presented here be used as a guideline and that the

actual code values be verified (and modified) on the bench with the device driving the actual transformer and termination expected in the application.

Figure 19 shows the D/A codes necessary for XPLS to drive a DSX-1 pulse using a Pulse Engineering 1:1.36 ± 5% turns ratio step-up transformer (PE # 64952, or PE 65774) and 0-110ft of 22 AWG twisted pair cable. (These code values are the same as those contained in the internal XPLS ROM for the 0-110 ft. waveform template, i.e. SM=1, ILS[2:0]=000.)

Figure 19 - CODE Register Sequence For 0-110 feet Build-out



To program the XPLS CODE registers for a custom waveform template, the following sequence should be used:

1. Set the RPT bit in the XPLS Configuration register (02CH, 06CH, 0ACH, 0ECH) to logic 0.

2. Write the CODE register address (0-7) in the XPLS CODE Indirect Address register (register 02EH, 06EH, 0AEH, 0EEH).

3. Write the desired code value to the XPLS CODE Indirect Data register (register 02FH, 06FH, 0AFH, 0EFH).

4. Repeat steps 2 and 3 until all the CODE registers are written.

5. Enable XPLS to generate the new waveform by setting RPT to logic 1.

The contents of the XPLS CODE registers can be reviewed at any time by using the following sequence:

1. Write the CODE register address (0-7) in the XPLS CODE Indirect Address register (register 02EH, 06EH, 0AEH, 0EEH).

2. Read the XPLS CODE Indirect Data register (register 02FH, 06FH, 0AFH, 0EFH). This returns the code contents of the desired code register.

12.2 Using the Digital Jitter Attenuator

The key to using DJAT lies in selecting the appropriate divisors for the phase comparison between the selected reference clock and the generated "jitter-free" clock.

Default Application

Upon reset, the QDSX default condition provides jitter attenuation with the "jitter-free" clock referenced to the transmit clock TCLKI[X]. The DJAT SYNC bit is also logic 1 by default. DJAT is configured to divide its input clock rate, TCLKI[X], and its output "jitter-free" clock rate, both by 48, which is the maximum length of the FIFO. These divided down clock rates are then used by the phase comparator to update the DJAT DPLL. The phase delay between TCLKI[X] and the "jitter-free" clock is synchronized to the physical data delay through the FIFO. For example, if the phase delay between TCLKI[X] and the "jitter-free" clock is 12 UI (unit intervals), the FIFO will be forced to lag its output data 12 bits from its input data.

The default mode works well with TCLKI[X] at 1.544MHz for T1 operation format or at 2.048MHz for E1 operation format.

Data Burst Application

In applications where TCLKI[X] works at a higher than nominal instantaneous rate (but with gapping to provide the same nominal rate over time), a few factors must be considered to adequately filter the resultant "jitter-free" clock into a smooth 1.544MHz or 2.048MHz clock. The magnitude of the phase shifts in the incoming bursty data are too large to be properly attenuated by the PLL alone. However, the magnitudes, and the frequency components of these phase shifts are known, and are most often multiples of 8 kHz.

In this situation, the input clock to DJAT is a gapped bursty clock. The phase shifts of the input clock with respect to the generated "jitter-free" clock in this case are large, but when viewed over a longer period, such as a frame, there is little net phase shift. Therefore, by choosing the divisors appropriately, the large phase shifts can be filtered out, leaving a stable reference for the DPLL to lock onto. In this application, the N1 and N2 divisors should be changed to C0H (i.e. divisors of 193 for T1 applications) or FFH (i.e. divisors of 256 for E1

applications). Consequently, the frequency of the clock inputs to the phase discriminator in the PLL is 8 kHz. The DJAT SYNC option must be disabled since the divisor magnitude of 193 or 256 is not an integer multiple of the FIFO length 48.

The DJAT phase lock loop has a single order low pass jitter transfer function. By default, the corner frequency is 8.8 Hz. The corner may be moved by the appropriate selection of clock divisors:

$$f_c = \frac{f_t}{1536\pi(N2+1)}$$

where

f_c= corner frequency

f_t = TCLKI[X] average frequency

N2= value in the Output Clock Divisor Control register

Ensure the Reference Clock Divisor Control value (N1) is also modified to be equal to the Output Clock Divisor Control value(N2).

The self-centering circuitry of the FIFO should be enabled by setting the CENT register bit. This sets up the FIFO read pointer to be at least 4 UI away from the end of the FIFO registers, and then disengages. Should variations in the frequency of input clock or the output clock cause the read pointer to drift to within one unit interval of FIFO overflow or underflow, the pointer will be incrementally pushed away by the LIMIT control without any loss of data.

With SYNC disabled, and CENT and LIMIT enabled, the maximum tolerable phase difference between the bursty input clock and the smooth "jitter-free" clock is 40UI. Phase wander between the two clock signals is compensated for by the LIMIT control.

12.3 Using XPLS without DJAT

The XPLS requires an 8X clock that is synchronous to its transmit clock, and which satisfies particular setup and hold requirements with respect to that transmit clock. When the DJAT PLL is in the transmit stream, it provides the necessary clocks. Should the DJAT be bypassed or in the receive stream, or should a 24X clock not be available to the PLL, alternate arrangements must be made to supply XPLS with its required clocks. The possible cases are: a)

FIFOBYP =1 or DJATTX =0 when XSEL[1] = 0, b) FIFOBYP = 1 or DJATTX =0 when XSEL[1:0] = 10, c) FIFOBYP=0 and DJATTX=1 but XSEL[1] = 1, d) FIFOBYP = 1 or DJATTX =0 when XSEL[1:0] = 11, and e) FIFOBYP = 0 and DJATTX =1 but XSEL[1:0] = 11.

12.3.1 FIFO not in Tx path, XSEL[1] = 0

When FIFOBYP =1 or DJATTX =0, but XSEL[1] = 0, a 24X clock must be provided on XCLK. An 8X clock will be internally generated, either by dividing XCLK by 3 (if XSEL[0] = 1) or synchronous to the PLL reference. (XSEL[0] = 0). All quadrants on the QDSX share a single 8X clock, which is presented on CLKO8X. TCLKI[4:1] must be synchronous to CLKO8X, and must satisfy the setup and hold conditions specified in the A.C. Characteristics section.

12.3.2 FIFO not in Tx path, XSEL[1] = 1, XSEL[0] = 0.

When FIFOBYP =1 or DJATTX =0, but XSEL[1:0] = 10, a 8X clock must be provided on XCLK. This 8X clock must be synchronous with TCLKI[4:1], and TCLKI[4:1] must satisfy the setup and hold relationships to XCLK specified in the A.C. Characteristics section.

12.3.3 FIFO is in Tx path, XSEL[1] = 1, XSEL[0] = 0.

When FIFOBYP = 0 and DJATTX = 1, but XSEL[1:0] = 10, then the DJAT FIFO is used to buffer between TCLKI[4:1] and an XPLS transmit clock generated by dividing down the system 8X clock. This arrangement guarantees the XPLS will get the clocks it needs. In this case, the 8X clock (provided on XCLK) need only be frequency locked to 8X the TCLKI[4:1] frequency. TCLKI[4:1] need not be phase locked to the 8X clock in this case.

12.3.4 FIFO not in Tx path, XSEL[1] = 1, XSEL[0] = 1.

This setting is reserved.

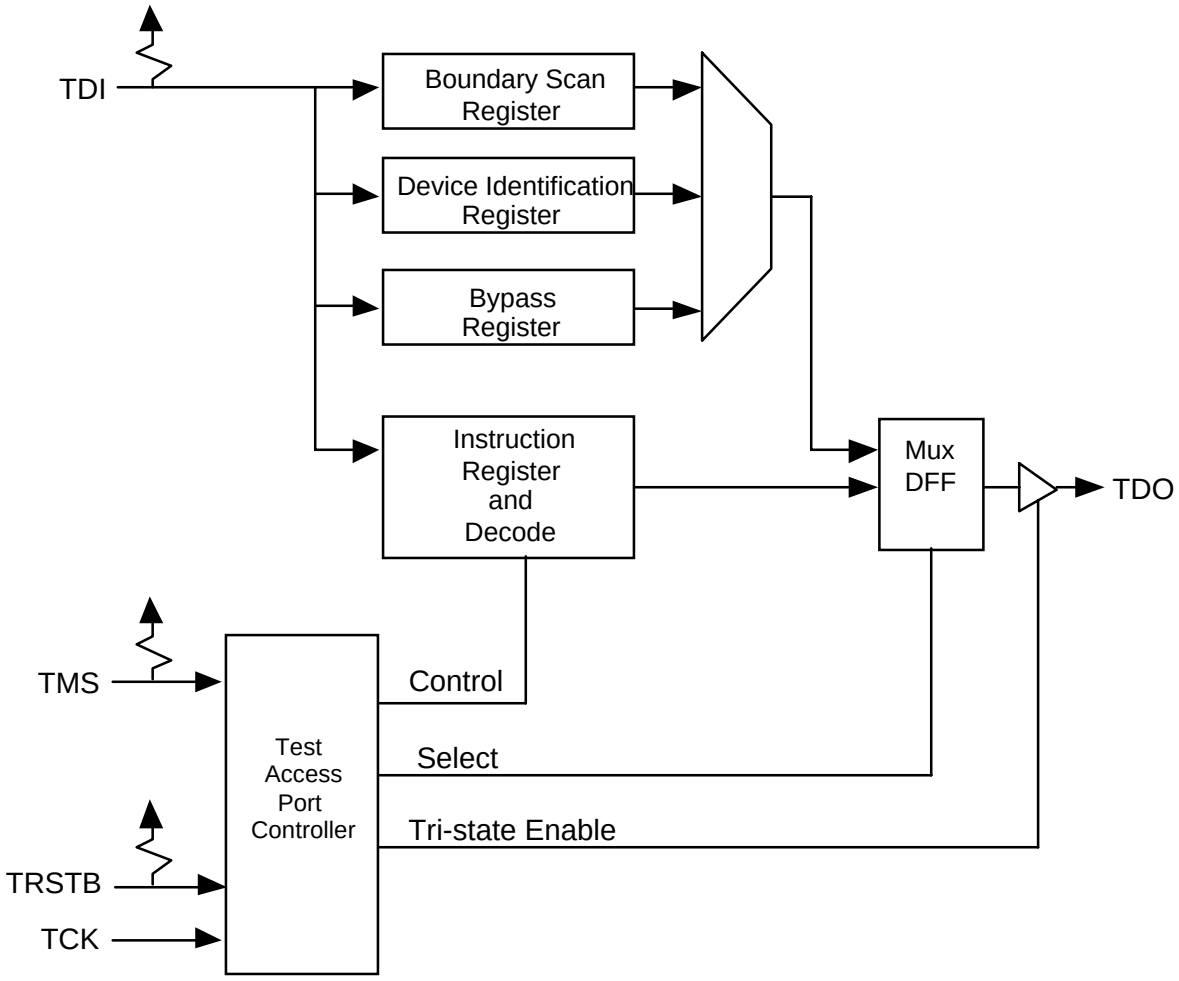
12.3.5 FIFO is in Tx path, XSEL[1] = 1, XSEL[0] = 1.

This setting is reserved.

12.4 JTAG Support

The QDSX supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 20.

Figure 20 - Boundary Scan Architecture



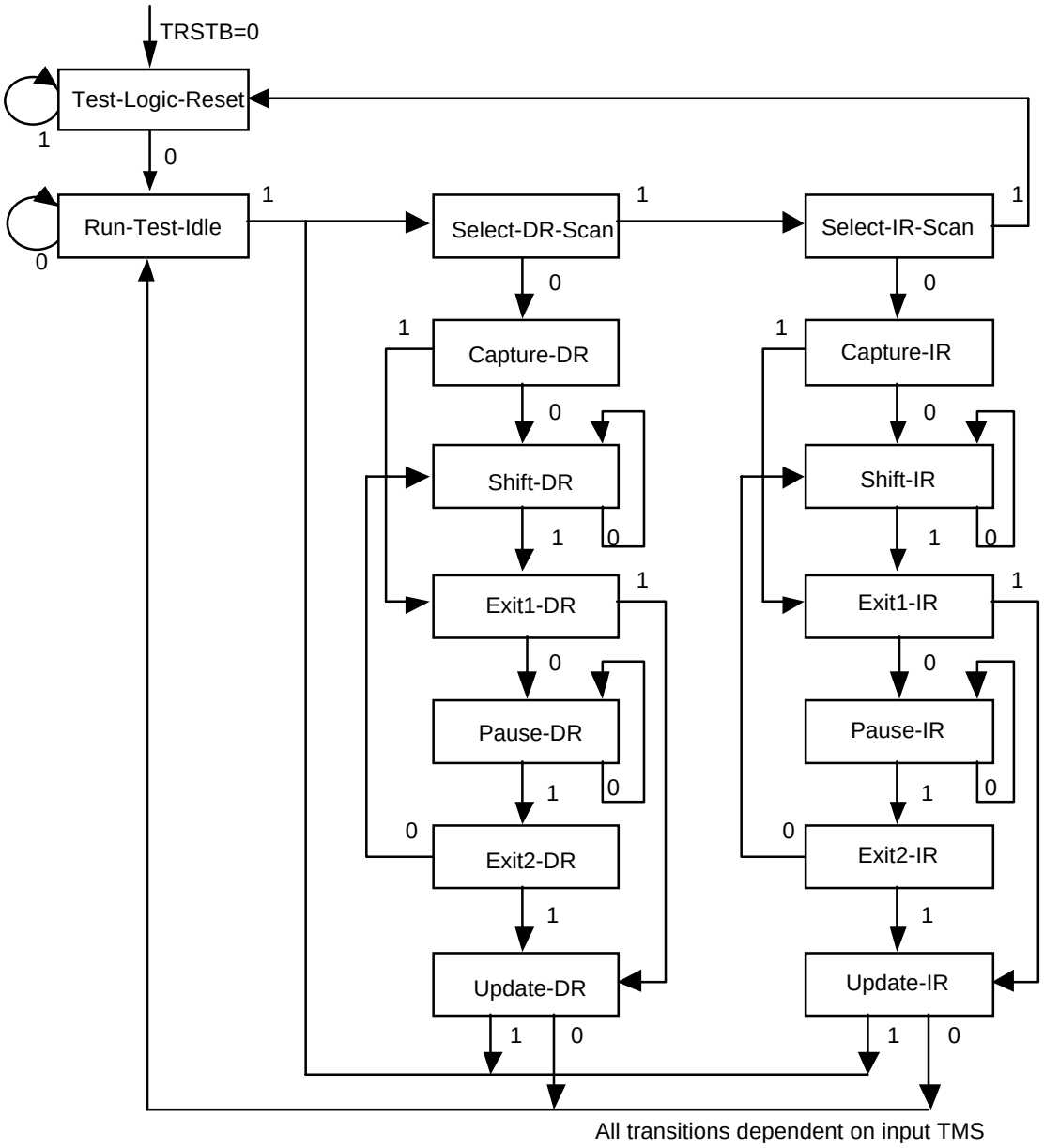
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input TDI to primary output TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output TDO. In addition, patterns can be shifted in on primary input TDI and forced onto all digital outputs.

TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary TMS. The finite state machine is shown in Figure 21.

Figure 21 - TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input,

TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input TDI and output TDO.

BYPASS

The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out TDO using the Shift-DR state.

Boundary Scan Register

The boundary scan register is made up of 64 boundary scan cells, divided into input observation (in_cell), output (out_cell), and bidirectional (io_cell) cells. These cells are detailed in the pages which follow. The first 32 cells form the ID code register, and carry the code 043140CD. The cells are arranged as follows:

Table 13 -

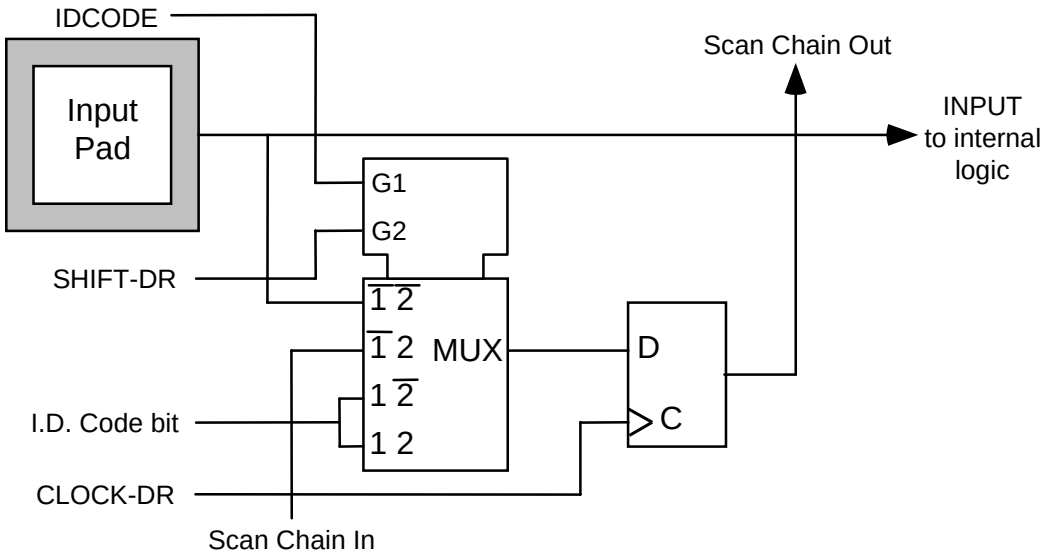
Pin/Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
RSTB[4]	63	IN_CELL	0	RDP[3]	27	OUT_CELL	-
ALE	62	IN_CELL	0	RCLKO[2]	26	OUT_CELL	-
CSB	61	IN_CELL	0	RDN[2]	25	OUT_CELL	-
WRB	60	IN_CELL	0	RDP[2]	24	OUT_CELL	-
RDB	59	IN_CELL	0	RCLKO[1]	23	OUT_CELL	-
A[0:8]	58 - 50	IN_CELL	100001100	RDN[1]	22	OUT_CELL	-
DDI[3]	49	IN_CELL	0	RDP[1]	21	OUT_CELL	-
DCR	48	IN_CELL	1	RDUAL	20	IN_CELL	-
TDUAL	47	IN_CELL	0	INTB	19	IO_CELL	-
TDN[4]	46	IN_CELL	1	INTB_OEN 1	18	OUT_CELL	-
TDP[4]	45	IN_CELL	0	D[0]	17	IO_CELL	-

Pin/Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
TCLKI[4]	44	IN_CELL	0	D0_OEN[1]	16	OUT_CELL	-
TDN[3]	43	IN_CELL	0	D[1]	15	IO_CELL	
TDP[3]	42	IN_CELL	0	D1_OEN[1]	14	OUT_CELL	-
TCLKI[3]	41	IN_CELL	0	D[2]	13	IO_CELL	-
TDN[2]	40	IN_CELL	0	D2_OEN[1]	12	OUT_CELL	-
TDP[2]	39	IN_CELL	1	D[3]	11	IO_CELL	-
TCLKI[2]	38	IN_CELL	1	D3_OEN[1]	10	OUT_CELL	-
TDN[1]	37	IN_CELL	0	D[4]	9	IO_CELL	-
TDP[1]	36	IN_CELL	0	D4_OEN[1]	8	OUT_CELL	-
TCLKI[1]	35	IN_CELL	1	D[5]	7	IO_CELL	-
XCLK	34	IN_CELL	1	D5_OEN[1]	6	OUT_CELL	-
CLKO8X	33	OUT_CELL	0	D[6]	5	IO_CELL	
RCLKO[4]	32	OUT_CELL	1	D6_OEN[1]	4	OUT_CELL	-
RDN[4]	31	OUT_CELL	-	D[7]	3	IO_CELL	-
RDP[4]	30	OUT_CELL	-	D7_OEN[1]	2	OUT_CELL	
RCLKO[3]	29	OUT_CELL	-	HIZ[2][2]	1	OUT_CELL	-
RDN[3]	28	OUT_CELL	-	HIZ[4][3]	0	OUT_CELL	-

Notes:

1. All OEN signals will set the corresponding bidirectional pin to an output when set low.
2. When set high, RDP[4:1], RDN[4:1], and RCLKO[4:1] will be set to high impedance.
3. When set high, CLKO8X will be set to high impedance.
4. RSTB is the first bit of the boundary scan chain.

Figure 22 - Input Observation Cell (IN_CELL)



In this diagram and those that follow, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the centre of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the table above.

Figure 23 - Output Cell (OUT_CELL)

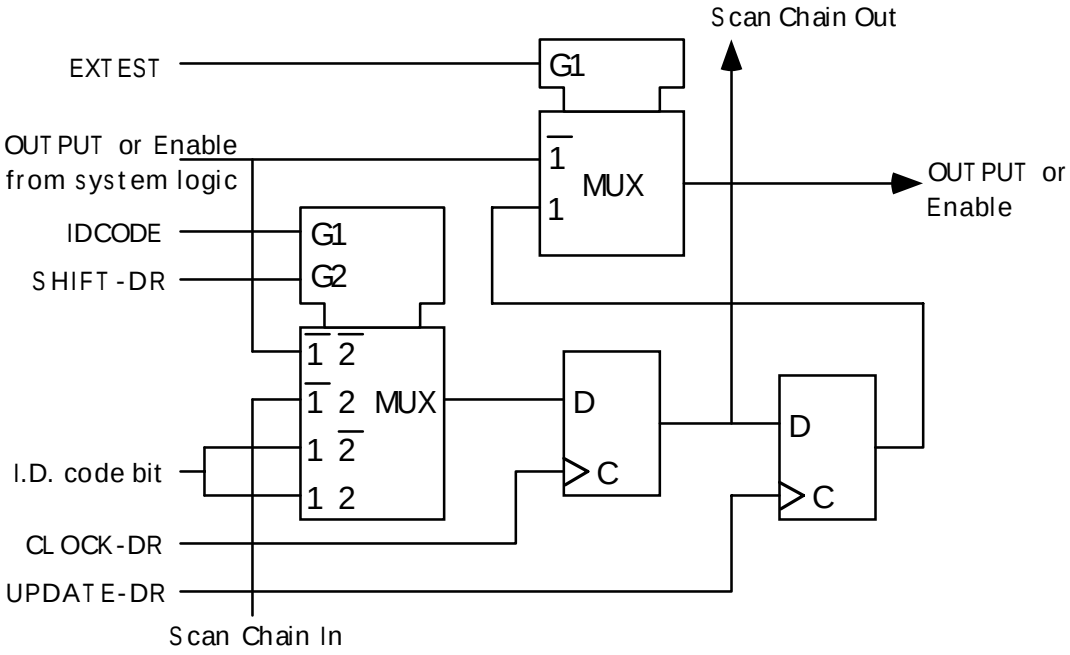


Figure 24 - Bidirectional Cell (IO_CELL)

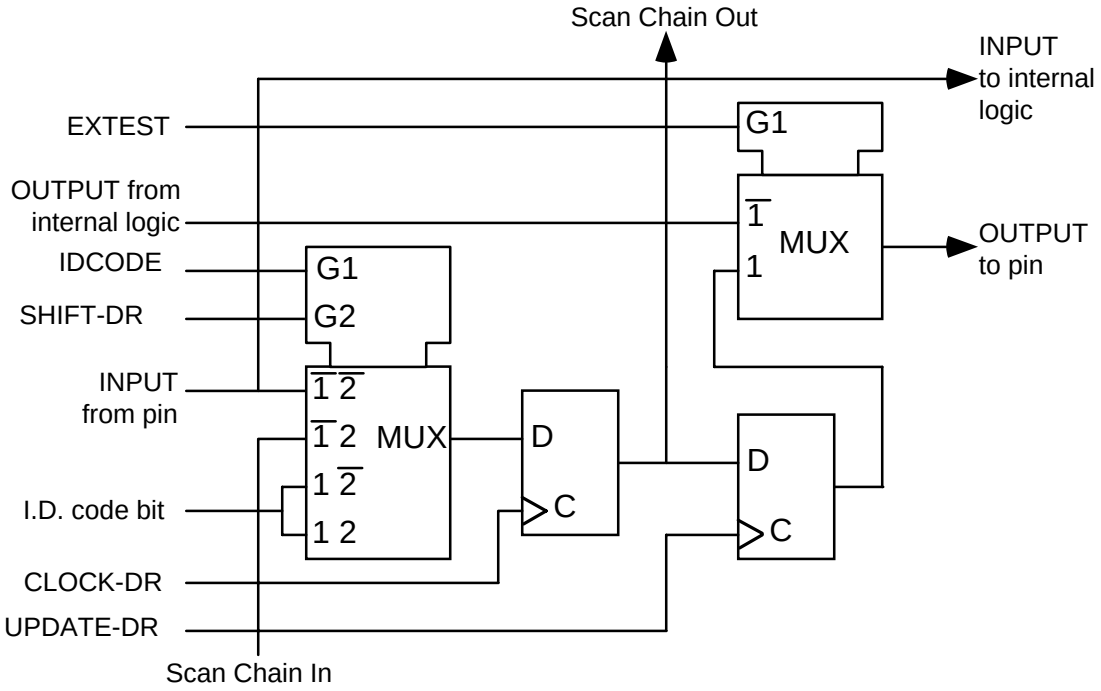
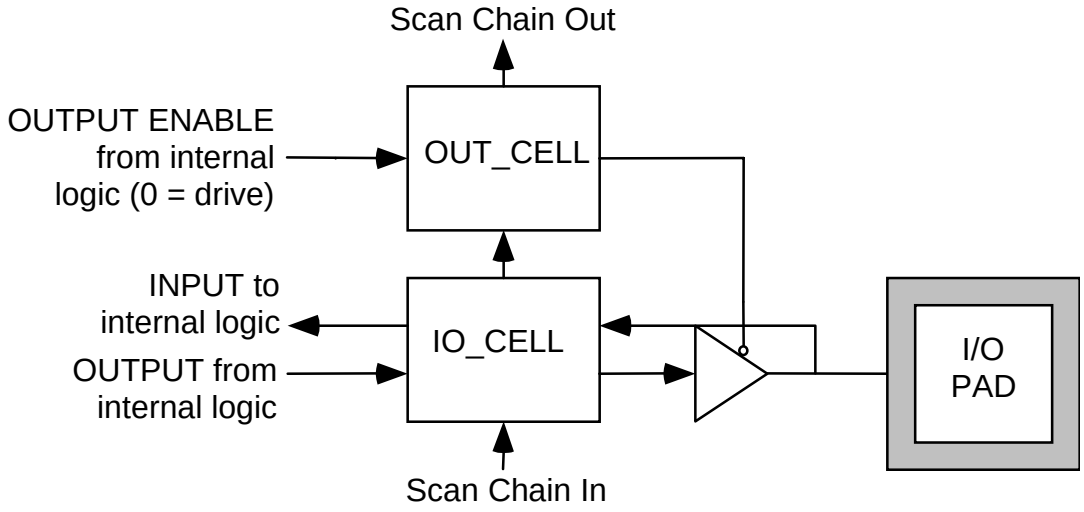


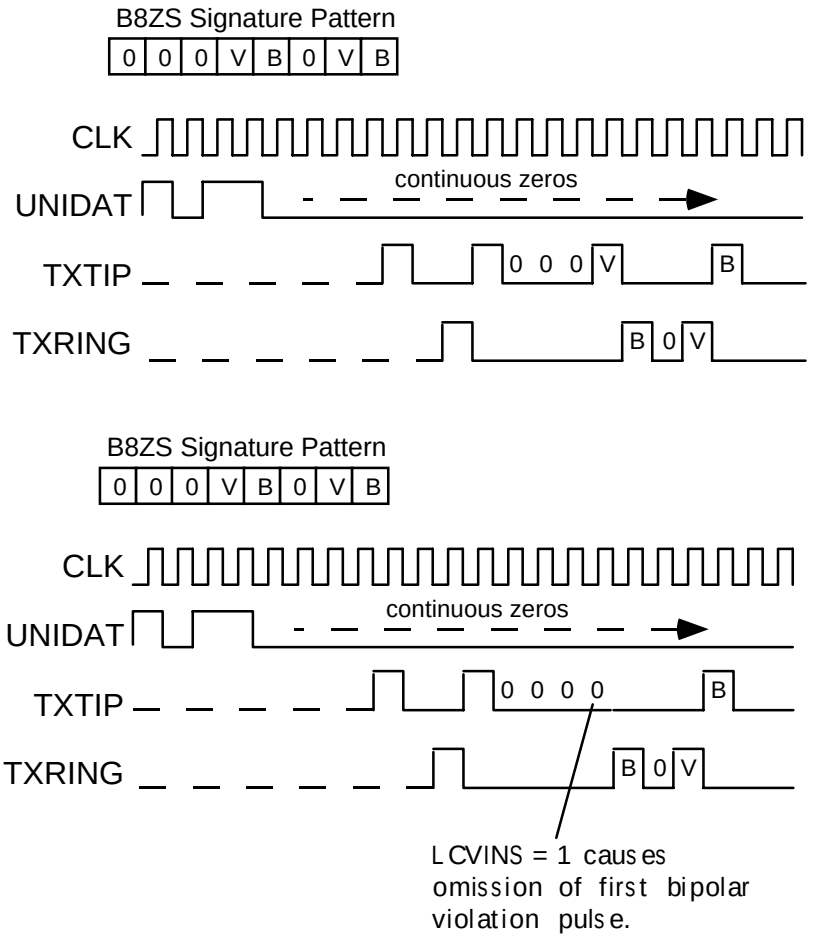
Figure 25 - Layout of Output Enable and Bidirectional Cells



13 FUNCTIONAL TIMING

13.1 Line Code Violation Insertion

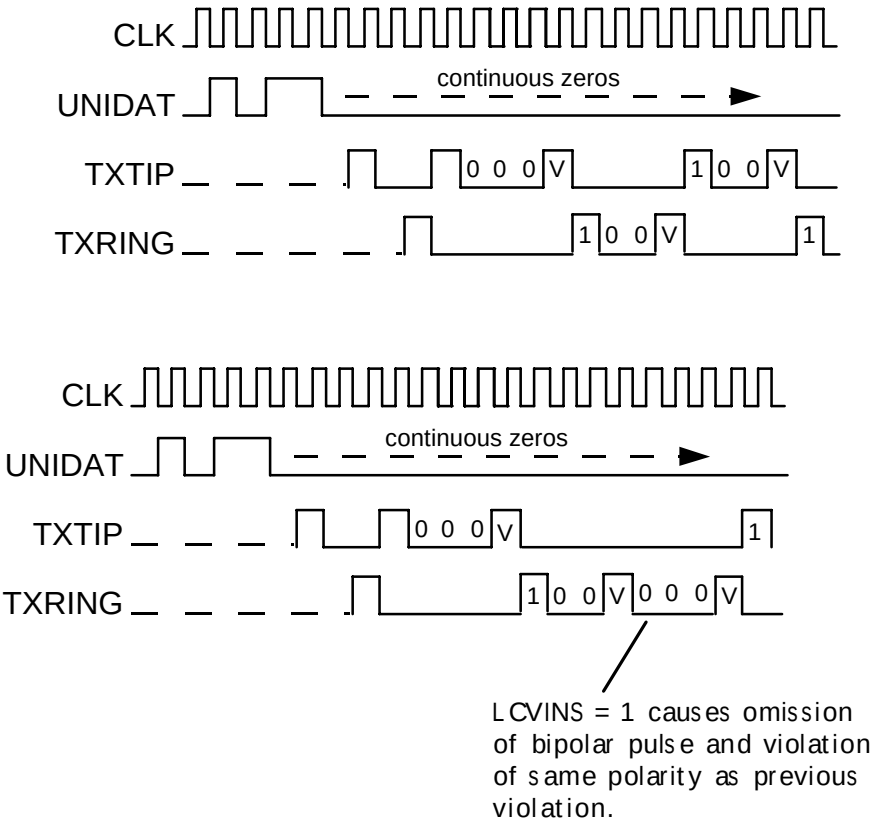
Figure 26 - B8ZS Line Code Violation Insertion



The effect of setting the LCVINS bit of the Diagnostics register (005H, 045H, 085H, and 0C5H) is shown in the above diagrams. The signals CLK and UNIDAT are not actual signals but are used as reference guidelines and TXTIP[X] and TXRING[X] have been shown as square NRZ pulses for illustrative purposes. CLK shows the reference 1x clock used to generate the TXTIP[X] and TXRING[X] outputs. UNIDAT is the unipolar data stream that is B8ZS encoded to generate the TXTIP[X] and TXRING[X] bipolar output streams. Setting LCVINS

to a logic 1 generates one line code violation and 3 bit errors by causing the omission of the first line code violation pulse when a string of 8 consecutive zeros occurs in the unipolar data stream UNIDAT. To generate another line code violation, the LCVINS bit must be reset to logic 0 and then set to logic 1 again.

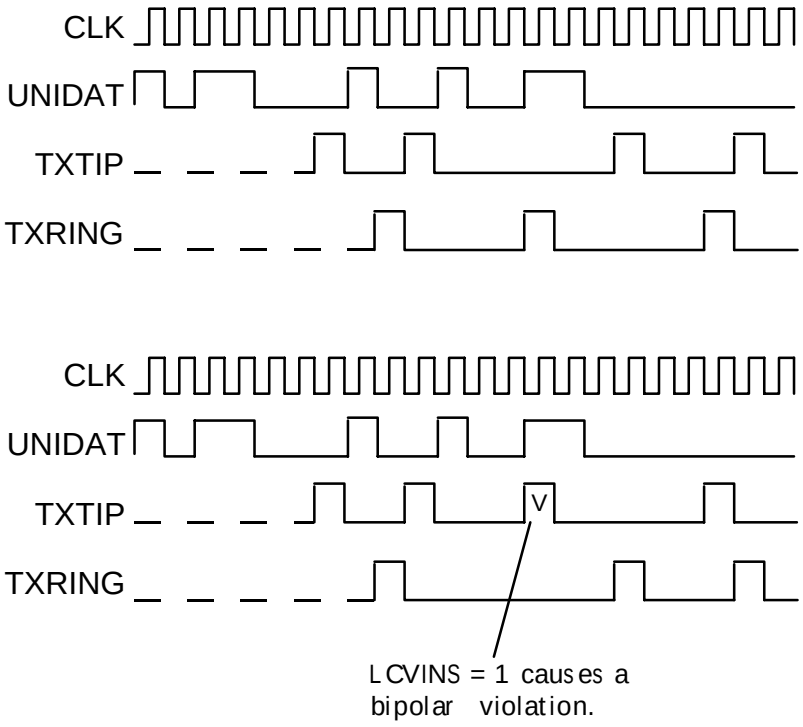
Figure 27 - HDB3 Line Code Violation Insertion



The effect of setting the LCVINS bit of the Diagnostics register (005H, 045H, 085H, and 0C5H) is shown in the above diagrams. The signals CLK and UNIDAT are not actual signals but are used as reference guidelines and TXTIP[X] and TXRING[X] have been shown as square NRZ pulses for illustrative purposes. CLK shows the reference 1x clock used to generate the TXTIP[X] and TXRING[X] outputs. UNIDAT is the unipolar data stream that is HDB3 encoded to generate the TXTIP[X] and TXRING[X] bipolar output streams. Setting LCVINS to a logic 1 generates one line code violation by causing the a bipolar violation pulse of the same polarity as the previous bipolar violation pulse when a string of 4 consecutive zeros occurs in the unipolar data stream UNIDAT. To

generate another line code violation, the LCVINS bit must be reset to logic 0 and then set to logic 1 again.

Figure 28 - AMI Line Code Violation Insertion



The effect of setting the LCVINS bit of the Diagnostics register (005H, 045H, 085H, and 0C5H) is shown in the above diagrams. The signals CLK and UNIDAT are not actual signals but are used as reference guidelines and TXTIP[X] and TXRING[X] have been shown as square NRZ pulses for illustrative purposes. CLK shows the reference 1x clock used to generate the TXTIP[X] and TXRING[X] outputs. UNIDAT is the unipolar data stream that is AMI encoded to generate the TXTIP[X] and TXRING[X] bipolar output streams. Setting LCVINS to a logic 1 generates one line code violation by causing the next pulse to be of the same polarity as the previous pulse. Subsequent pulses will be of alternate polarity. To generate another line code violation, the LCVINS bit must be reset to logic 0 and then set to logic 1 again.

14 ABSOLUTE MAXIMUM RATINGS

Table 14 -.QDSX Absolute Maximum Ratings

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on VDD with Respect to GND	-0.6V to +6.0V
Voltage on Any Pin	-0.6V to VDD+0.6V
Static Discharge Voltage	±1000 V
Latch-Up Current (T_A = -40°C to +85°C)	±100 mA
Package Power Dissipation	2.0 W

15 CAPACITANCE

Table 15 - QDSX Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{in}	Input Capacitance	10	pF	T_A = 25°C, f = 1 MHz (sampled only)
C_{out}	Output Capacitance	10	pF	T_A = 25°C, f = 1 MHz (sampled only)
C_{bidir}	Bidirectional Capacitance	10	pF	T_A = 25°C, f = 1 MHz (sampled only)

16 D.C. CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 5 V ±5%)

(Typical Conditions: T_A = 25°C, V_{DD} = 5 V)

Table 16 - QDSX D.C. Characteristics

Symbol	Parameter	Min	Typ.	Max	Units	Conditions
V_{DD},RA_{VD}, TA_{VD}	Power Supply	4.75	5.0	5.25	Volts	
V_{IL}	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0		V_{DD}+ 0.5	Volts	Guaranteed Input HIGH Voltage
V_{RXTIP}	Analog Input Voltage	A_{VS} -0.6		A_{VD} +0.6	Volts	
V_{OL}	Output or Bidirectional Low Voltage		0.1	0.4	Volts	V_{DD} = 5.0 V, I_{OL} = -4 mA for Data Bus Pins and -2 mA for others, Note 3
V_{OH}	Output or Bidirectional High Voltage	VDD-1.0V	4.7		Volts	V_{DD} = 5.0 V, I_{OH} = 4 mA for Data Bus Pins and 2 mA for others, Note 3
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			1.0	Volts	

Symbol	Parameter	Min	Typ.	Max	Units	Conditions
V_{TH}	Reset Input Hysteresis Voltage		1.0		Volts	
I_{ILPU}	Input Low Current	+20	+83	+200	µA	V_{IL} = GND, Notes 1, 3
I_{IHPU}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 1, 3
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND, Notes 2, 3
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$, Notes 2, 3
I_{DDOP1}	Operating Current DSX-1 Configuration			325	mA	V_{DD} = 5.25 V, Outputs Unloaded, XCLK = 37.056 MHz, TCLKI[4:1] = 1.544 MHz, 1.544 Mbit/s data rate on RXTIP. Note 4
I_{DDOP2}	Operating Current E1 Configuration			330	mA	V_{DD} = 5.25 V, Outputs Unloaded, XCLK = 49.152 MHz, TCLKI[4:1] = 2.048 MHz, 2.048 Mbit/s data rate on RXTIP. Note 4

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.

2. Input pin or bidirectional pin without internal pull-up resistors

3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

4. I_{DDOP} is the sum of all power supply currents when transmitting all ones from XPLS. For DSX-1, XPLS is using the 440'-550' line buildout, which is the most energetic, and a 50Ω resistor is connected across TXTIP and TXRING of each quadrant in order to mimic a 100Ω line reflected back through a 1:1.36 transformer. For E1, XPLS is using the 75Ω template, and a 44Ω resistor is connected across TXTIP and TXRING of each quadrant in order to mimic a 75Ω line reflected back through a 1:1.36 transformer.

5. Typical Values are given as an aid to the system designer. Product is not tested to the typical values given in the data sheet.

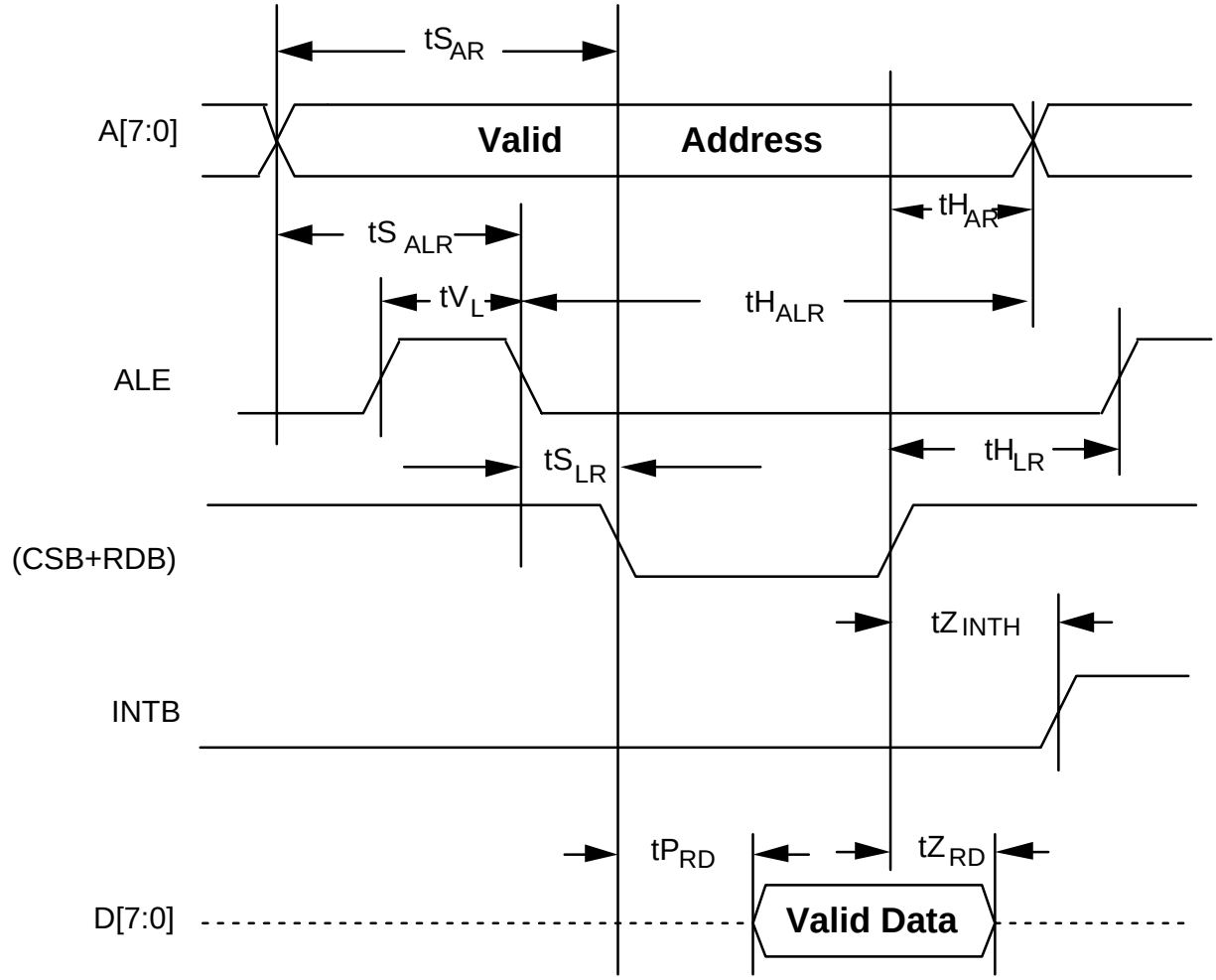
17 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

T_A = -40°C to +85°C, V_{DD} = 5 V ±5%

Table 17 - Microprocessor Interface Read Access (Figure 29)

Symbol	Parameter	Min	Max.	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tristate		20	ns
tZ_{INTH}	Valid Read Negated to INTB open		50	ns

Figure 29 - Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high and parameters tSALR, tHALR, tVL, tSLR, and tHLR are not applicable.

5. Parameter tH_{AR} is not applicable if address latching is used.

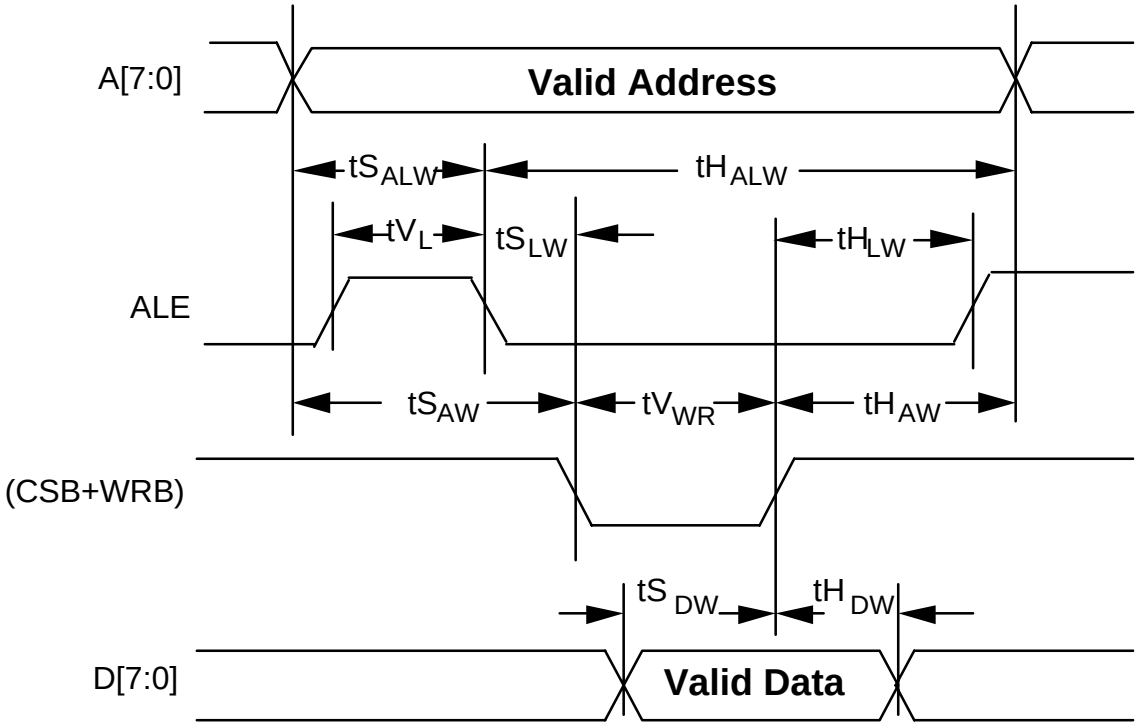
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 18 - Microprocessor Interface Write Access (Figure 30)

Symbol	Parameter	Min	Max.	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 30 - Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2. In non-multiplexed address/data bus architectures, ALE should be held high and parameters tSALW, tHALW, tVL, tSLW, and tHLW are not applicable.

3. Parameter tH_{AW} is not applicable if address latching is used.

4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

18 A.C. TIMING CHARACTERISTICS

T_A= -40° to +85°C, V_{DD}=5V ±5%

Table 19 - XCLK Input for Jitter Attenuation (Figure 31)

Symbol	Description	Min	Max.	Units
tXCLK	XCLK Frequency (nominally 37.056 MHz ± 100 ppm for T1 format or 49.152 MHz ± 50 ppm for E1 format)		50	MHz
	XCLK Duty Cycle (at XCLK = 37.056 MHz for T1, 49.152 MHz for E1)	40	60	%

Figure 31 - XCLK Input Timing for Jitter Attenuation

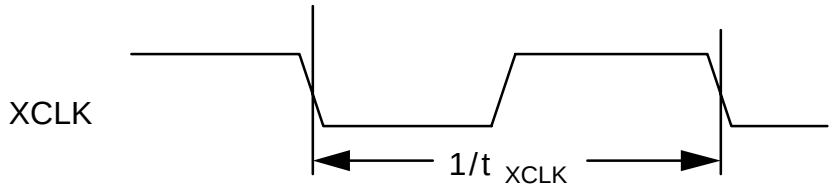
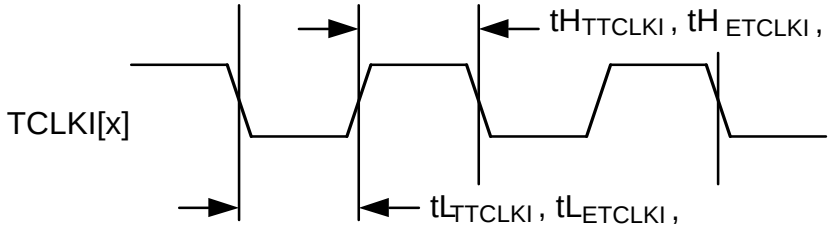
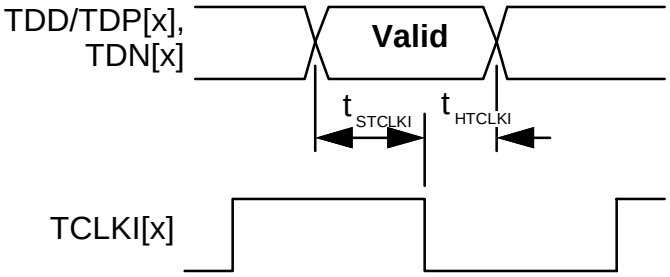


Table 20 - TCLKI Input Timing (Figure 32)

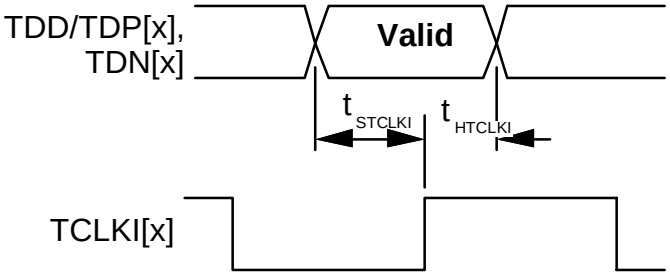
Symbol	Description	Min	Max.	Units
tT1TCLKI	TCLKI Frequency for T1[1] (nominally 1.544 MHz ± 130 ppm)		1.545	MHz
tE1TCLKI	TCLKI Frequency for E1 (note 1)[1] (nominally 2.048 MHz ± 50 ppm)		2.049	MHz
tHTTCLKI	TCLKI High Duration (for T1 formats)	165		ns
tLTTCLKI	TCLKI Low Duration (for T1 formats)	165		ns
tHETCLKI	TCLKI High Duration (for E1 formats)	125		ns
tLETCLKI	TCLKI Low Duration (for E1 formats)	125		ns
tSTCLKI	TCLKI to TDD/TDP or TDN Input Set-up Time	20		ns
tHTCLKI	TCLKI to TDD/TDP or TDN Input Hold-up Time	20		ns

Figure 32 - TCLKI Input Timing





With TFALL bit =1



With TFALL bit =0

Table 21 - CLKO8X Input Timing (FIFO not in TX path) (Figure 33)

Symbol	Description	Min	Max.	Units
$t_{SCLKO8X}$	TCLKI[X] to CLKO8X Setup Time	25		ns
$t_{HCLKO8X}$	TCLKI[X] to CLKO8X Hold Time	10		ns

The above timing parameters apply when FIFOBYP=1 or DJATTX=0, but XSEL[1:0] is not set to 10 binary.

Figure 33 - CLKO8X Input Timing Diagram (FIFO not in TX path)

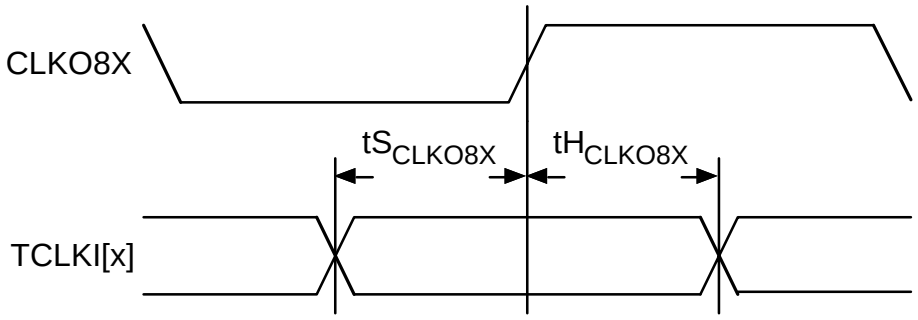


Table 22 - XCLK Input Timing (FIFO not in TX path) (Figure 34)

Symbol	Description	Min	Max.	Units
tS_{XCLK}	TCLKI[X] to XCLK Setup Time	10		ns
tH_{XCLK}	TCLKI[X] to XCLK Hold Time	25		ns

The above timing parameters apply when FIFOBYP=1 or DJATTX=0, and XSEL[1:0] is set to 10 binary.

Figure 34 - XCLK Input Timing Diagram (FIFO not in TX path)

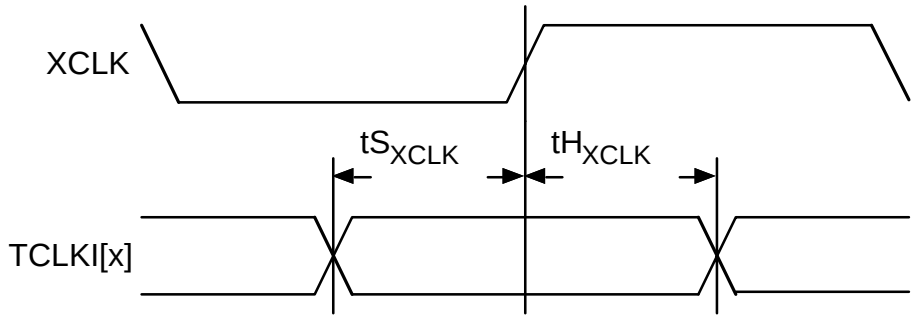
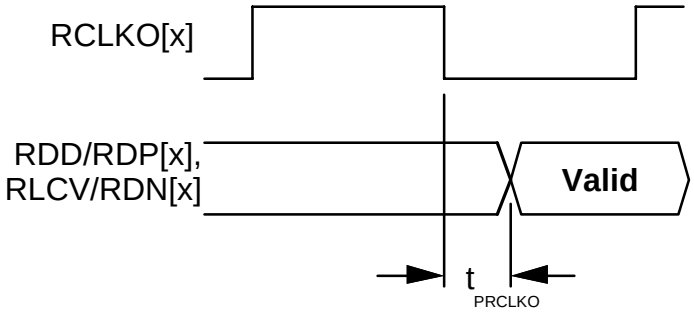


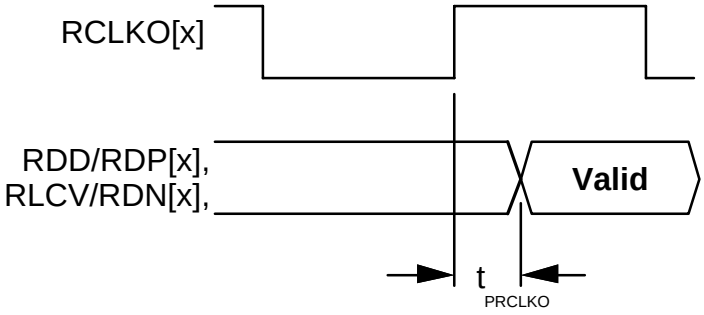
Table 23 - RCLKO Output Timing (Figure 35)

Symbol	Description	Min	Max.	Units
tPRCLKO	RCLKO to Output Signals Propagation Delay		50	ns

Figure 35 - RCLKO Output Timing Diagram



With RRISE bit=0



With RRISE bit=1

Table 24 - JTAG Port Interface Timing (Figure 36)

Symbol	Description	Min	Max.	Units
t_{TCK}	TCK Frequency		1	MHz
tD_{TCK}	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns

Figure 36 - JTAG Port Interface Timing

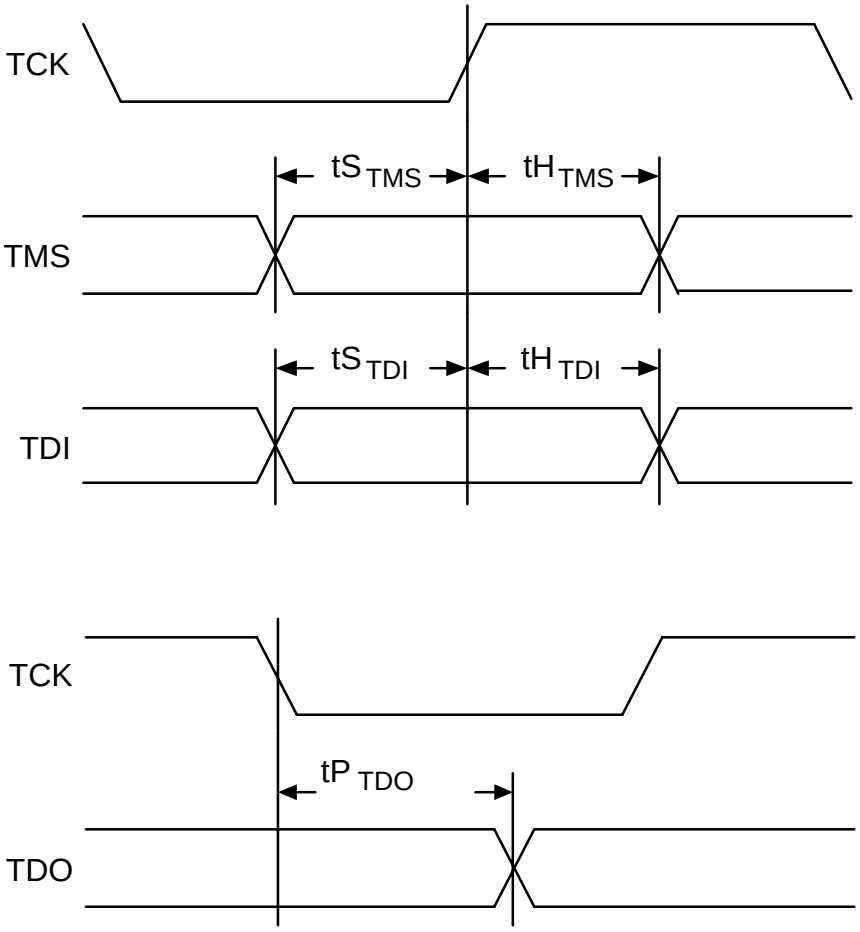
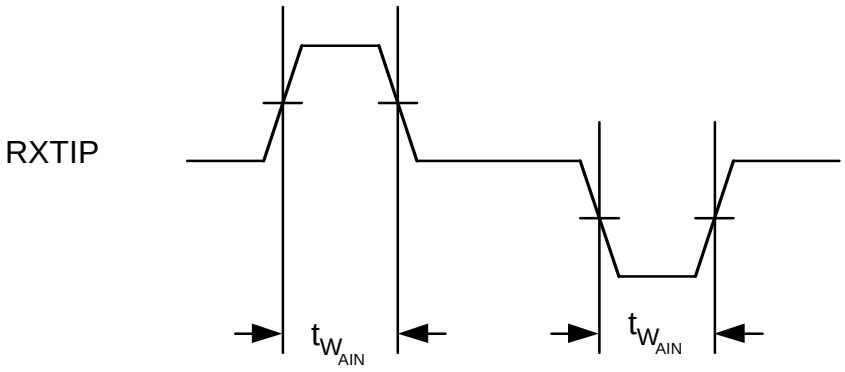


Table 25 - Analog Receive Data Input Timing (Figure 37)

Symbol	Description	Min	Max.	Units
tWE1AIN	Receive Analog Data Signal Pulse Width in CEPT E1 mode[5]	200	300	ns
tWT1AIN	Receive Analog Data Signal Pulse Width in T1 mode[5]	250	400	ns

Figure 37 - Analog Receive Data Input Timing Diagram



Notes on Input Timing:

1. TCLKI can be a jittered clock signal subject to the minimum high and low durations tH_{TTCLKI}, tL_{TTCLKI}, tH_{ETCLKI}, and tL_{ETCLKI}. These durations correspond to the nominal XCLK input frequency for the selected DSX-1 or CEPT E1 format. Proper operation when TCLKI is a jittered clock is guaranteed by the design of the DJAT, and thus is not completely production tested.

2. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

3. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

4. When an input high clock time is specified, the clock high pulse width is measured between the 1.4 Volt points of the rise and fall ramps. When an input low clock time is specified, the clock low pulse width is measured between the 1.4 Volt points of the fall and rise ramps.

5. Parameter guaranteed by design, not production tested.

6. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

7. Maximum output propagation delays are measured with a 50 pF load on the outputs.

19 ORDERING AND THERMAL INFORMATION

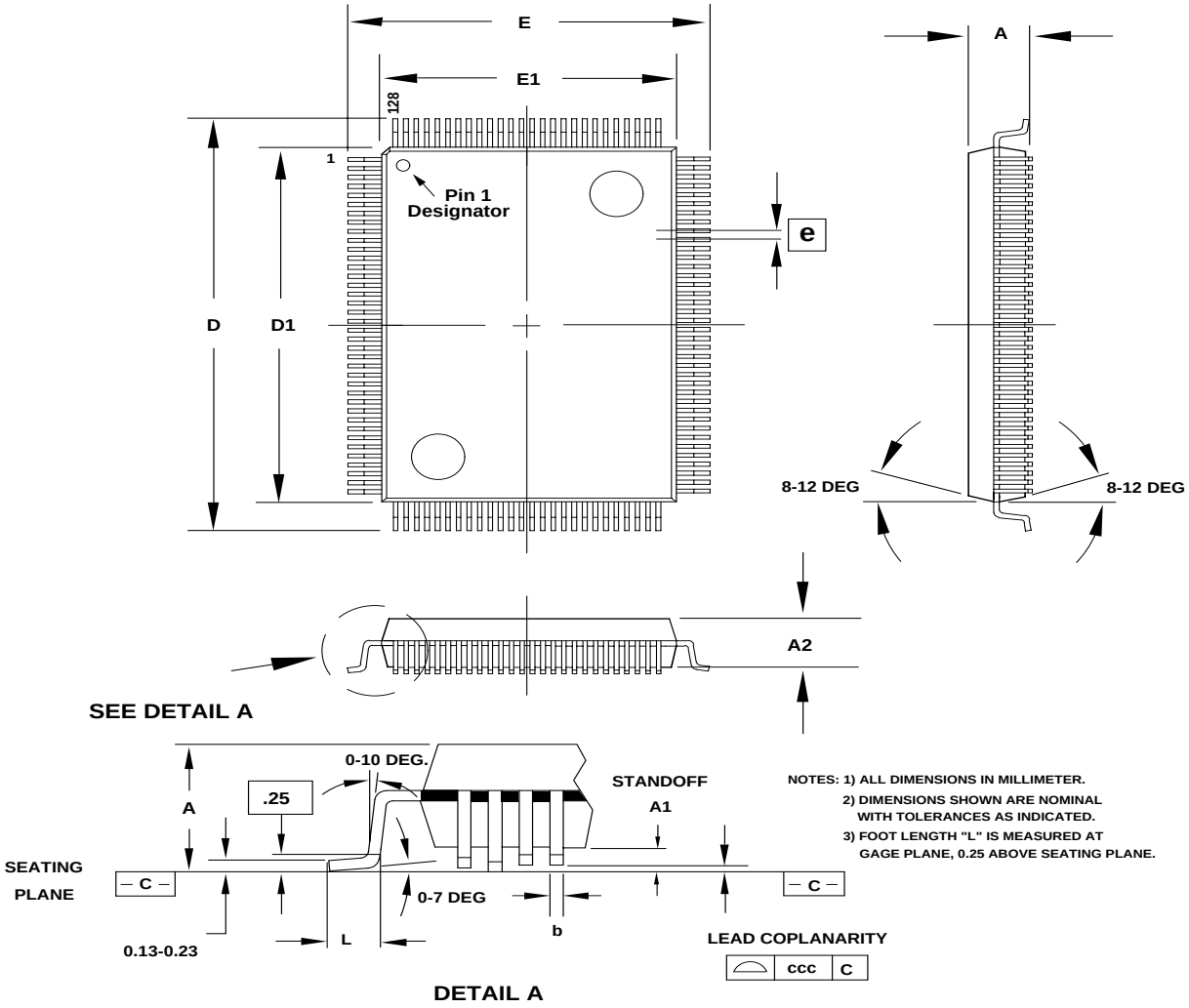
Table 26 - QDSX Ordering Information

PART NO.	DESCRIPTION
PM4314-RI	128 Plastic Quad Flat Pack (PQFP)

Table 27 - QDSX Thermal Information

PART NO.	CASE TEMPERATURE	Theta Ja	Theta Jc
PM4314-RI	-40°C to 85°C	31°C/W	11°C/W

20 MECHANICAL INFORMATION



PACKAGE TYPE: 128 PIN METRIC RECTANGULAR PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 14 x 20 x 2.7 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	2.82	0.25	2.57	22.95	19.90	16.95	13.90	0.73		0.17	
Nom.			2.70	23.20	20.00	17.20	14.00	0.88	0.50	0.22	
Max.	3.40	0.53	2.87	23.45	20.10	17.45	14.10	1.03		0.27	0.10

NOTES

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