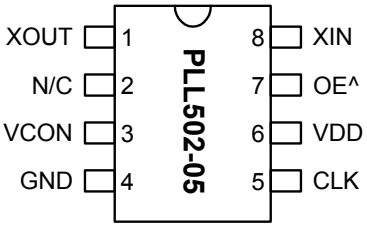
PLL502-05

Low Phase Noise VCXO (12MHz to 25MHz)

FEATURES

- Low phase noise VCXO output for the 12MHz to 25MHz range (-135 dBc at 10kHz offset).
- CMOS output.
- 12 to 25MHz crystal input.
- Integrated variable capacitors.
- Wide pull range (+/- 300 ppm).
- Low jitter (RMS): 2.2ps period.
- 2.5 or 3.3V operation voltage.
- Available in 8-Pin SOIC.

PIN CONFIGURATION



Note: ^ denotes internal pull up

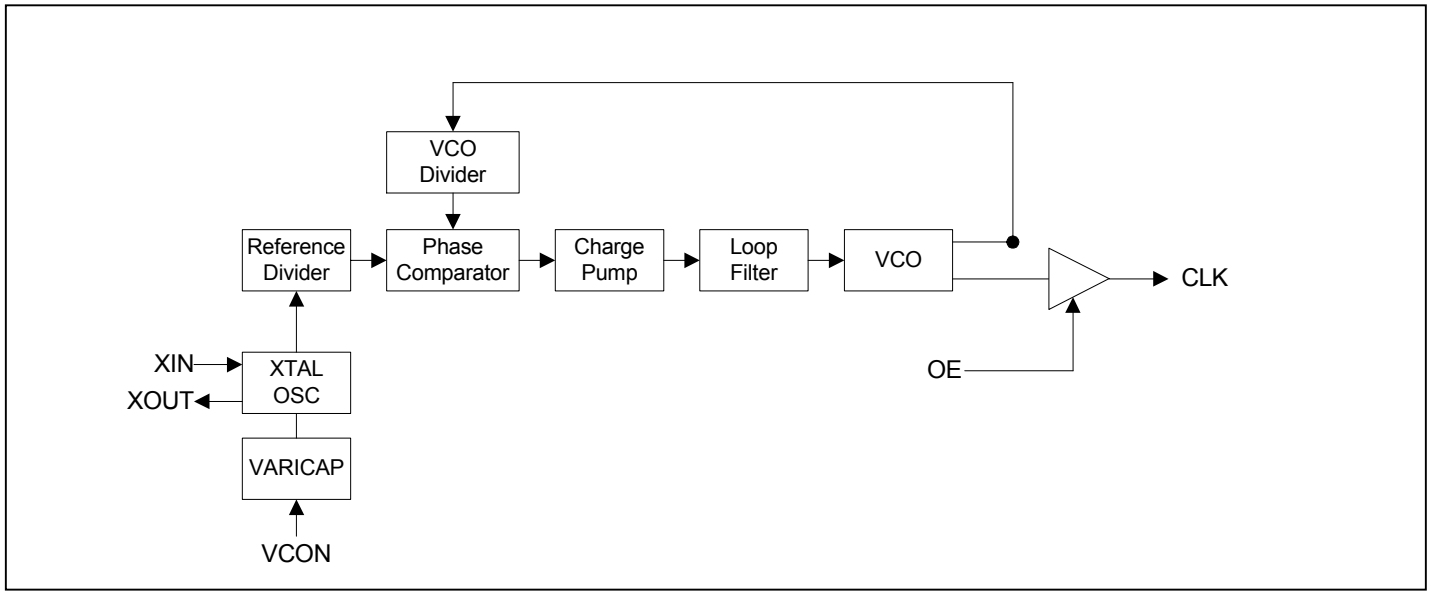
DESCRIPTION

The PLL502-05 is a low cost, high performance and low phase noise VCXO, providing less than -135dBc at 10 kHz offset in the 12MHz to 25MHz operating range. The very low jitter (2.2ps RMS period jitter) makes this chip ideal for applications requiring voltage controlled frequency sources. Input crystal can range from 12 to 25MHz (fundamental resonant mode).

OUTPUT RANGE

MULTIPLIER	FREQUENCY RANGE	OUTPUT BUFFER
No PLL	12 - 25MHz	CMOS

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
XOUT	1	I	Crystal output. See Crystal Specifications on page 3.
N/C	2	-	Not connected.
VCON	3	I	Voltage Control input.
GND	4	P	Ground.
CLK	5	O	Output clock.
VDD	6	P	VDD power supply pin.
OE	7	I	Output Enable input. Disables the output when low. Internal pull-up enables output by default if pin is not connected to low.
XIN	8	I	Crystal input. See Crystal Specifications on page 3.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. DC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	F_{XIN} = 12 - 25MHz Output load of 10pF		16	20	mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output drive current	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	10			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	10			mA
Short Circuit Current				±50		mA
VCXO Control Voltage	VCON		0		V_{DD}	V

3. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			12		25	MHz
Output Clock Rise/Fall Time		0.3V ~ 3.0V with 15 pF load		2.4		ns
Output Clock Duty Cycle		Measured @ 50% V_{DD}	45	50	55	%

4. Voltage Control Crystal Oscillator (3.3V)

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		F_{XIN} = 12 – 25MHz; XTAL C_0/C_1 < 250 0V ≤ VCON ≤ 3.3V		500		ppm
CLK output pullability		VCON=1.65V, ±1.65V	±200			ppm
VCXO Tuning Characteristic				150		ppm/V
Pull range linearity					10	%
VCON pin input impedance			2000			kΩ
VCON modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

5. Jitter and Phase Noise Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	with capacitive decoupling between VDD and GND.		2.2		ps
Phase Noise relative to carrier	25MHz @100Hz offset		-95		dBc/Hz
Phase Noise relative to carrier	25MHz @1kHz offset		-120		dBc/Hz
Phase Noise relative to carrier	25MHz @10kHz offset		-142		dBc/Hz
Phase Noise relative to carrier	25MHz @100kHz offset		-150		dBc/Hz
Phase Noise relative to carrier	25MHz @1MHz offset		-150		dBc/Hz

6. Crystal Specifications

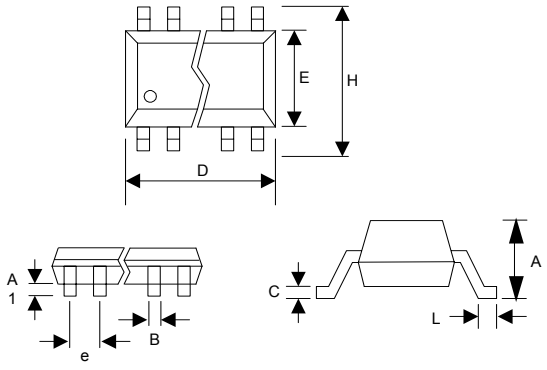
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	12		25	MHz
Crystal Loading Capacitance Rating	$C_{L\ (xtal)}$		9.5		pF
C0/C1				250	-
ESR	R_S			30	Ω

Note: Crystal Loading rating: 9.5pF is the loading the crystal sees from the VCXO chip at VCON = 1.65V. It is assumed that the crystal will be at nominal frequency at this load. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range.

PACKAGE INFORMATION

8 PIN (dimensions in mm)

	Narrow SOIC	
Symbol	Min.	Max.
A	1.47	1.73
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	4.95
E	3.80	4.00
H	5.80	6.20
L	0.38	1.27
e	1.27 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL502-05 x x

Part Number

Temperature
C=Commercial
I=Industrial

Package
S=SOIC

Order Number	Marking	Package Option
PLL502-05SC	P502-05SC	8-Pin SOIC (Tube)
PLL502-05SC-R	P502-05SC	8-Pin SOIC (Tape and Reel)

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