PLL502-00

Multiplier VCXO IC Die for 12 to 25MHz Parallel Resonant Crystals

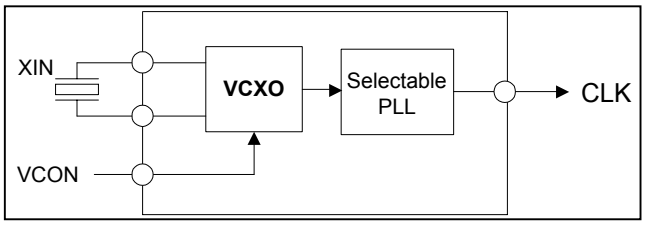
FEATURES

- Integrated voltage-controlled crystal oscillator circuitry (VCXO) (pull range 500ppm minimum).
- Low phase noise (-130dBc @ 10kHz offset at 44MHz output)
- Selectable frequency multipliers (x1, x2, x4, x8).
- 3.3V supply voltage.
- Uses inexpensive fundamental-mode parallel resonant crystals (from 12 to 25MHz).
- Selectable High Drive (30mA) or Standard Drive (10mA) output.
- Available in DIE (65 mil x 62 mil).

DESCRIPTION

The PLL502-00 is a monolithic low jitter and low phase noise (-130dBc @10kHz offset at 44MHz output), high performance CMOS VCXO IC Die, that uses a low cost crystal (12-25MHz).
The same die can be used as a VCXO with output frequencies ranging from F_{XIN} x 1 to F_{XIN} x 8 using selector pad bonding options (see Multiplier Selection Table on this page). This makes the PLL502-00 ideal for a wide range of applications from 12MHz to 190MHz (including 27MHz, 35.328MHz, 77.76MHz and 155.52MHz, etc.).

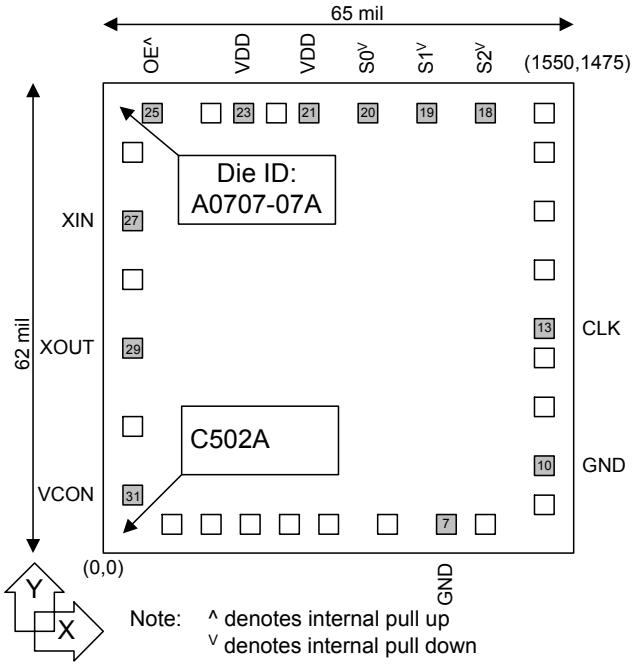
BLOCK DIAGRAM



DIE SPECIFICATIONS

Name	Value
Size	65 x 62 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

DIE CONFIGURATION



MULTIPLIER SELECTION

SELECTION			F_{XIN}	CLK (MHz)
S2	S1	S0		
0	0	0	12MHz – 25MHz	F_{XIN} x 2
0	0	1		F_{XIN} x 4
0	1	0		F_{XIN} x 1
0	1	1		F_{XIN} x 2*
1	0	0		F_{XIN} x 8
1	0	1		F_{XIN} x 1*
1	1	0		F_{XIN} x 4*
1	1	1		F_{XIN} x 8*

Note: - Selector pads default to '0', wire bond to VDD to set to '1'
- (*) High-drive output

PAD DESCRIPTION

Name	Number	Description
XIN	27	Crystal input connection.
XOUT	29	Crystal output connection.
VCON	31	Voltage Control Input.
GND	7,10	Ground.
CLK	13	Clock Output.
S[0:2]	18,19,20	Frequency selection pads
VDD	21,22,23	3.3V Power Supply.
OE	25	Output Enable: '0' to disable (tri-state output), 1' (default value when not connected) to enabled the output.

Multiplier VCXO IC Die for 12 to 25MHz Parallel Resonant Crystals

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. DC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	F_{XIN} = 12 - 25MHz Output load of 10pF		16	20	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output drive current (High Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	30			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	30			mA
Output drive current (Standard Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	10			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	10			mA
Short Circuit Current				±50		mA
VCXO Control Voltage	VCON		0		3.3	V

3. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			12		25	MHz
Output Clock Rise/Fall Time (Standard Drive)		0.3V ~ 3.0V with 15 pF load		2.4		ns
Output Clock Rise/Fall Time (High Drive)		0.3V ~ 3.0V with 15 pF load		1.2		
Output Clock Duty Cycle		Measured @ 50% V_{DD}	45	50	55	%

Multiplier VCXO IC Die for 12 to 25MHz Parallel Resonant Crystals

4. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		F_{XIN} = 12 – 25MHz; XTAL C_0/C_1 < 250 0V ≤ VCON ≤ 3.3V		500		ppm
CLK output pullability		VCON=1.65V, ±1.65V	±200			ppm
VCXO Tuning Characteristic				150		ppm/V
Pull range linearity					10	%
VCON pin input impedance			2000			kΩ
VCON modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

5. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	C_L (xtal)	At VCON = 1.65V		9.5		pF
Crystal Pullability	C_0/C_1 (xtal)	AT cut			250	-
Recommended ESR	R_E	AT cut			30	Ω

Note: Crystal Loading rating: 9.5pF is the loading the crystal sees from the VCXO chip at VCON = 1.65V. It is assumed that the crystal will be at nominal frequency at this load. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range.

6. Jitter and Phase Noise specification*

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	at 77.76MHz, with capacitive decoupling between VDD and GND.		3.5		ps
	at 155.52MHz, with capacitive decoupling between VDD and GND.		4		
Phase Noise relative to carrier	77.76MHz @100Hz offset		-100		dBc/Hz
Phase Noise relative to carrier	77.76MHz @1kHz offset		-123		dBc/Hz
Phase Noise relative to carrier	77.76MHz @10kHz offset		-130		dBc/Hz
Phase Noise relative to carrier	77.76MHz @100kHz offset		-125		dBc/Hz
Phase Noise relative to carrier	77.76MHz @1MHz offset		-125		dBc/Hz
Phase Noise relative to carrier	155.52MHz @100Hz offset		-95		dBc/Hz
Phase Noise relative to carrier	155.52MHz @1kHz offset		-120		dBc/Hz
Phase Noise relative to carrier	155.52MHz @10kHz offset		-128		dBc/Hz
Phase Noise relative to carrier	155.52MHz @100kHz offset		-122		dBc/Hz
Phase Noise relative to carrier	155.52MHz @1MHz offset		-120		dBc/Hz

* General condition: Control Voltage is 0V.

Multiplier VCXO IC Die for 12 to 25MHz Parallel Resonant Crystals

PAD ASSIGNMENT

Pad #	Name	X (µm)	Y (µm)	Description
7	GND	1042	109	Ground.
10	GND	1400	259	Ground.
13	CLK	1400	716	CMOS Clock Output.
18	S2	1232	1365	Used to select multiplication factor and Standard or High-Drive output. Internal pull down.
19	S1	1042	1365	Used to select multiplication factor and Standard or High-Drive output. Internal pull down.
20	S0	854	1365	Used to select multiplication factor and Standard or High-Drive output. Internal pull down.
21	VDD	659	1365	3.3V Power Supply.
23	VDD	459	1365	3.3V Power Supply.
25	OE	194	1365	Used to Enable/Disable the output. Internal pull up. See
27	XIN	109	1017	Crystal input. See Crystal Specifications on page 3.
29	XOUT	109	646	Crystal output. See Crystal Specifications on page 3.
31	VCON	109	181	Voltage Control Input. 0V to 3.3V.

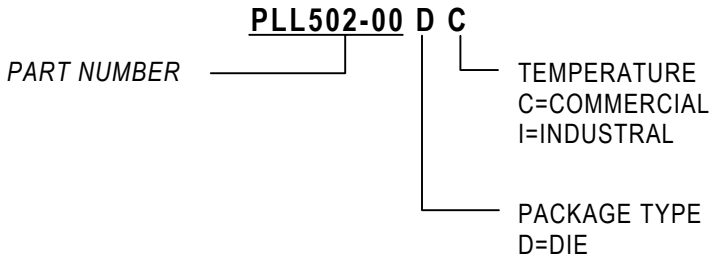
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PLL502-00DC	P502-00DC	Die (Waffle Pack)

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Phaselink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY: PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.