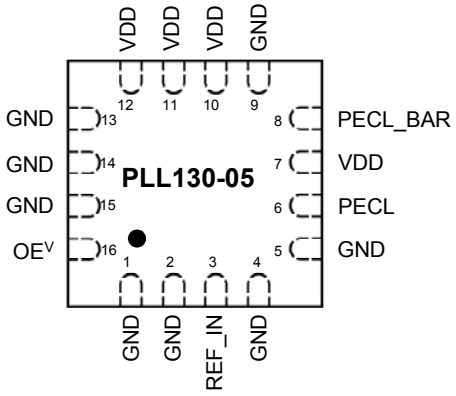
High Speed Translator Buffer to PECL (Enable Low)

FEATURES

- Differential PECL output
- Single AC coupled input (min. 100mV swing).
- Input range from DC to 1.0 GHz.
- 2.5V to 3.3V operation.
- Available in 3x3mm QFN.

PIN CONFIGURATION

(TOP VIEW)

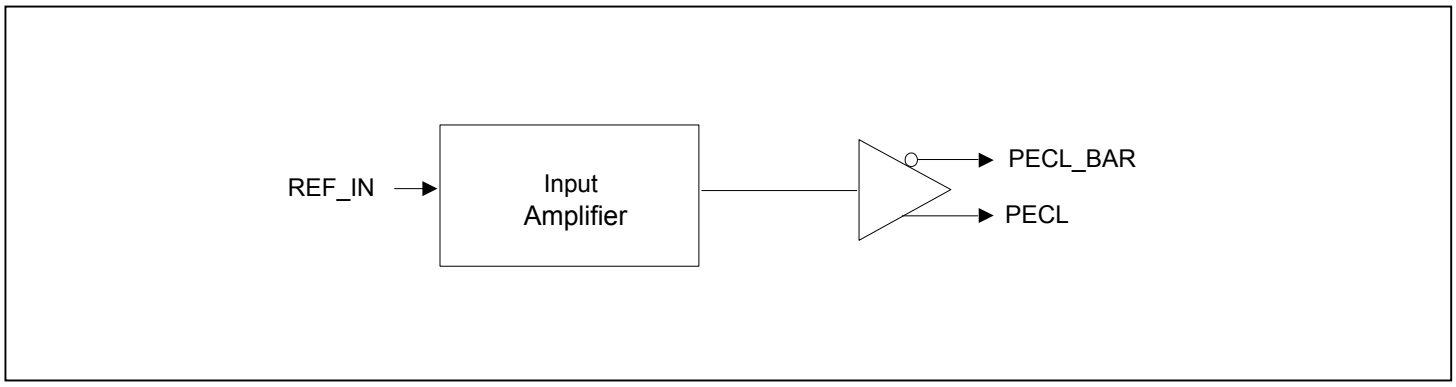


Note: ^V denotes internal pull down

DESCRIPTION

The PLL130-05 is a low cost, high performance, high speed, buffer that reproduces any input frequency from DC to 1.3GHz. It provides one pair of differential PECL outputs. Any input signal with at least 100mV swing can be used as reference signal. This chip is ideal for conversion from sine wave, TTL, CMOS, or LVDS to PECL.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	3x3mm QFN Pin number	Type	Description
GND	1,2,4,5, 9,13,14,15	P	Ground.
VDD	7,10,11,12	P	Power supply.
REF_IN	3	I	Reference input signal. The frequency of this signal will be reproduced at the output (after translation to PECL level).
PECL	6	O	PECL True output.
PECL_BAR	8	O	PECL Complementary output.
OE	16	I	Output enable ('0' for enable). Internal pull-down (default is '0').

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. AC Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency		0		1000	MHz
Input signal swing	REF_IN input	100			mV
Output Frequency		0		1000	MHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns

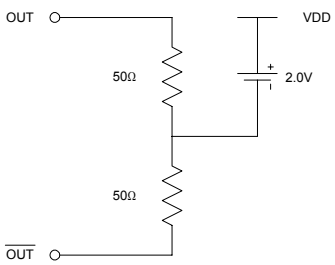
3. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

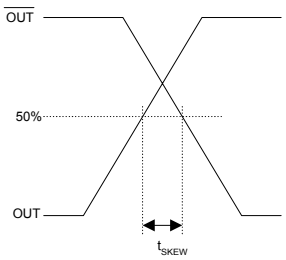
4. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

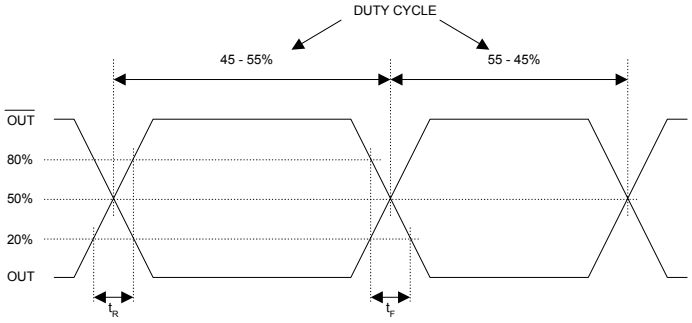
PECL Levels Test Circuit



PECL Output Skew



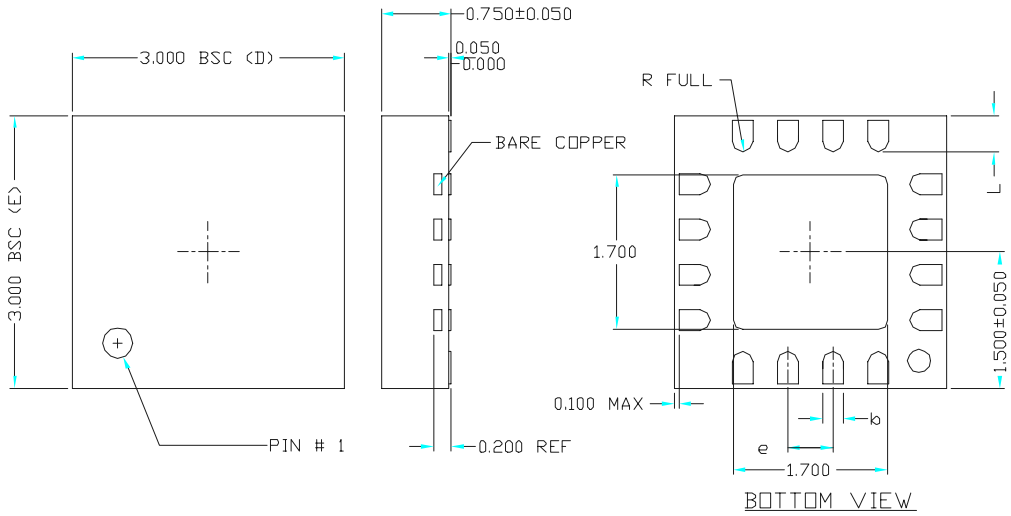
PECL Transistion Time Waveform



PACKAGE INFORMATION

VARIATIONS:

SYMBOL	16 LD		
	MIN	NOM	MAX
e	0.50 BSC		
b	0.18	0.23	0.30
L	0.30	0.40	0.50
ND	4		
NE	4		



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL130-05 S C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
I=INDUSTRAL

PACKAGE TYPE
Q=QFN

Order Number	Marking	Package Option
PLL130-05QC-R	P130-05QC	QFN - Tape and Reel
PLL130-05QC	P130-05QC	QFN - Tube

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