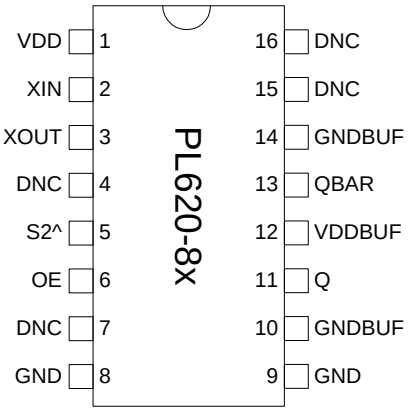
PL620-88/-89

Low Phase Noise XO (9.5-65MHz Output)

FEATURES

- Crystal input range: 19MHz to 65MHz
- Output range: 9.5MHz – 65MHz
- Very low phase noise and jitter
- Complementary outputs:
  - LVPECL (PL620-88)
  - LVDS (PL620-89)
- Supports 2.5V or 3.3V Power Supply.
- Available in 16 pin TSSOP GREEN/RoHS compliant package.

PIN CONFIGURATION



TSSOP-16L

Note: ^ denotes internal pull up

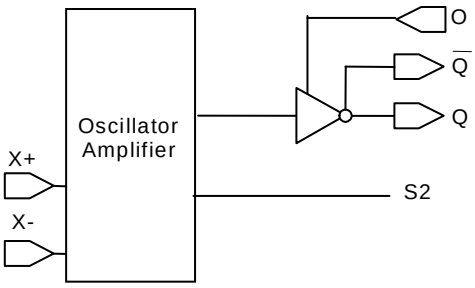
DESCRIPTION

The PL620-88 (LVPECL) and PL620-89 (LVDS) are XO ICs specifically designed to work with fundamental or 3rd OT crystals between 19MHz and 65MHz. The selectable divide by two feature extends the output range from 9.5MHz to 65MHz. They require very low current into the crystal resulting in better overall stability.

OUTPUT ENABLE LOGIC TABLE

Part Number	OE	State
PL620-88	0 (Default)	Output enabled
	1	Tri-state
PL620-89	0	Tri-state
	1 (Default)	Output enabled

BLOCK DIAGRAM



OUTPUT FREQUENCY DIVIDE BY TWO SELECTOR (S2)

S2	Output
0	Intput/2
1(Default)	Input

PACKAGE PIN ASSIGNMENT

Name	Pin#	Description
VDD	1	Power Supply.
XIN	2	Crystal input. See Crystal Specification on page 3.
XOUT	3	Crystal output. See Crystal Specification on page 3.
DNC	4, 7, 15, 16	Do Not Connect.
S2	5	Output Divide by Two selector pin. See the OUTPUT DIVIDE BY TWO SELECTOR table on page 1.
OE	6	Output Enable input. See OUTPUT ENABLE LOGIC table on page 1.
GND	8, 9	Ground.
GNDBUF	10	Ground for output buffer circuitry.
Q	11	LVPECL or LVDS output.
VDDBUF	12	Power supply for output buffer circuitry.
QBAR	13	Complementary LVPECL or LVDS output.
GNDBUF	14	Ground for output buffer circuitry.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Resonator Frequency	F_{XIN}	Fundamental	19		65	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$			8.5		pF
Interelectrode Capacitance	C_0				5	pF
Recommended ESR	R_E	AT cut			30	Ω

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Loaded Outputs)	I_{DD}	LVPECL/LVDS, 15pF Load			100/80	mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS) @ V_{DD} – 1.3V (LVPECL)	45	50	55	%
Short Circuit Current				±50		mA

4. Jitter Specifications

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Period jitter RMS at 27MHz	With capacitive decoupling between V_{DD} and GND. Over 10,000 cycles		2.3		ps
Period jitter peak-to-peak at 27MHz			18.5	20	
Accumulated jitter RMS at 27MHz	With capacitive decoupling between V_{DD} and GND. Over 1,000,000 cycles.		2.3		ps
Accumulated jitter pk-to-pk at 27MHz			24	25	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		2.3		ps

Measured on Wavecrest SIA 3000

5. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	27MHz	-75	-100	-125	-140	-145	dBc/Hz

Note: Phase Noise measured on Agilent E5500

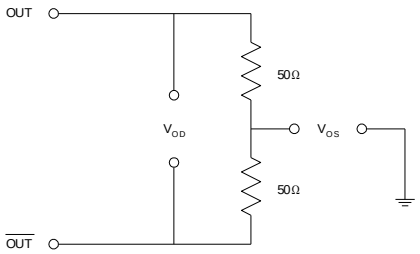
6. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

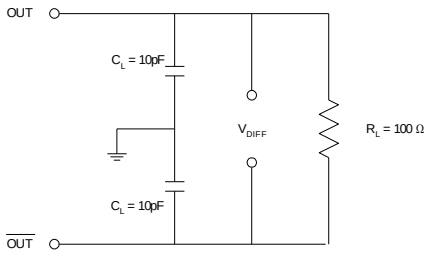
7. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

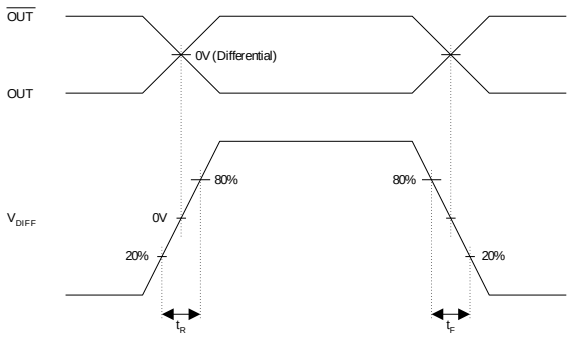
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



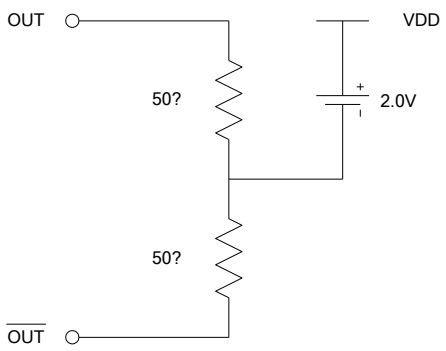
8. LVPECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage	V_{OH}	R_L = 50Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

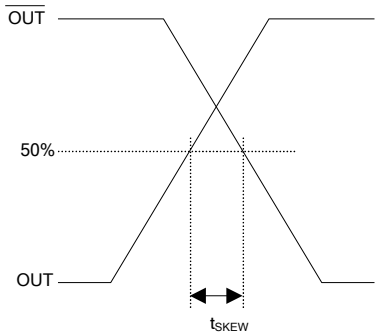
9. LVPECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Rise Time	t_r	@20/80% - LVPECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - LVPECL		0.5	1.5	ns

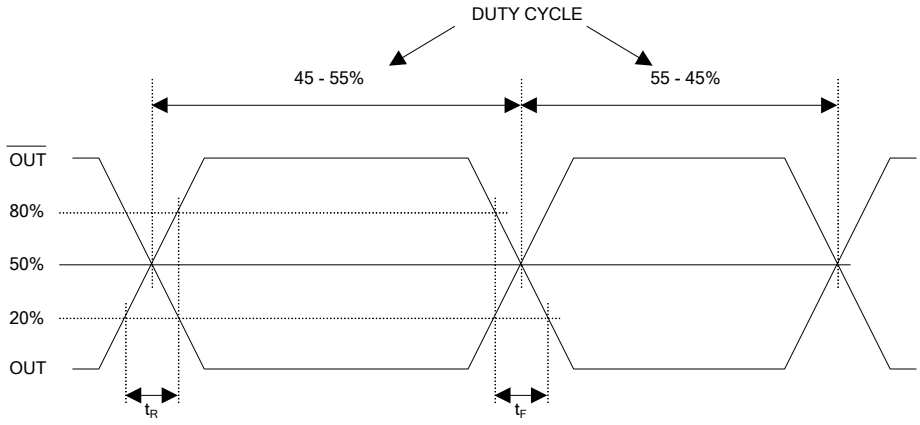
LVPECL Levels Test Circuit



LVPECL Output Skew

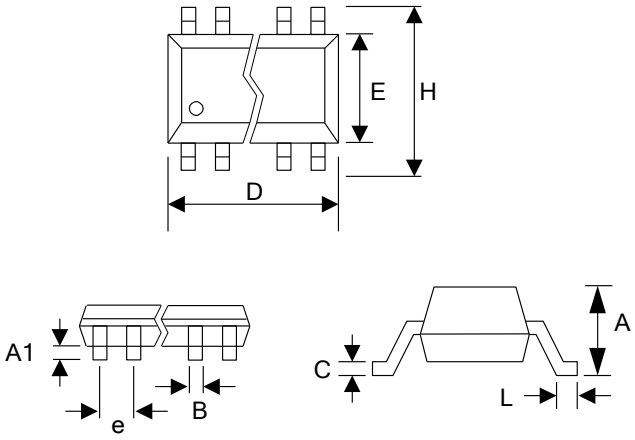


LVPECL Transistion Time Waveform



PACKAGE INFORMATION

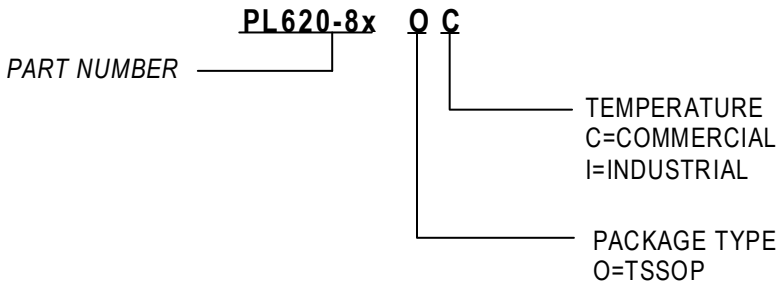
16 PIN TSSOP (mm)		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PL620-88OC-R	P620-88 OC	TSSOP – Tape and Reel
PL620-88OC	P620-88 OC	TSSOP – Tube
PL620-89OC-R	P620-89 OC	TSSOP – Tape and Reel
PL620-89OC	P620-89 OC	TSSOP – Tube

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