1.8V-3.3V PicoPLL™ KHz to MHz Programmable Clock

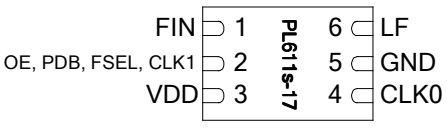
FEATURES

- Advanced Programmable PLL design for low-frequency (kHz) input applications.
- Input Frequency: 10kHz to 200MHz
- OTP selectable AC/DC Input Coupling.
- Accepts ≥0.1V reference signal input voltage
- Very low Jitter and Phase Noise
- Output Frequency:
  - ≤65MHz @ 1.8V operation
  - ≤90MHz @ 2.5V operation
  - ≤125MHz @ 3.3V operation
- Disabled outputs programmable as HiZ or Active Low.
- Offered in Tiny **GREEN**/RoHS compliant packages
  - 6-pin DFN (2.0mmx1.3mmx0.6mm)
  - 6-pin SC70 (2.3mmx2.25mmx1.0mm)
  - 6-pin SOT23 (3.0mmx3.0mmx1.35mm)
- Single 1.8V, 2.5V, or 3.3V ± 10% power supply
- Operating temperature range from -40°C to 85°C

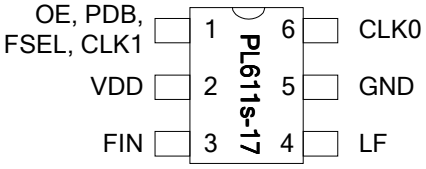
DESCRIPTION

The PL611s-17 is a low-cost general purpose frequency synthesizer and a member of PhaseLink's PicoPLL™ Factory Programmable 'Quick Turn Clock (QTC)' family. Designed to fit in a small SOT23, SC70, or DFN package for high performance, low power applications, the PL611s-17 accepts a low frequency (>10KHz) Reference input and generates up to 125MHz outputs with the best phase noise, jitter performance, and power consumption for handheld devices and notebook applications. In addition, one programmable I/O pin can be configured as Output Enable (OE), Frequency switching (FSEL), Power Down (PDB) input, or CLK1 (FOUT, FREF, FREF/2) output. Cascading the PL611s-17 with other PicoPLL ICs can result in producing all required system clocks with specific savings in board space, power consumption, and cost.

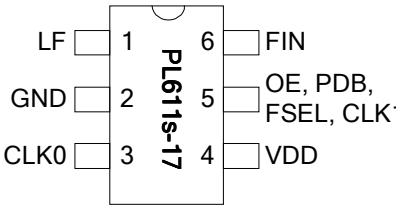
PACKAGE PIN CONFIGURATION



DFN-6L
(2.0mmx1.3mmx0.6mm)

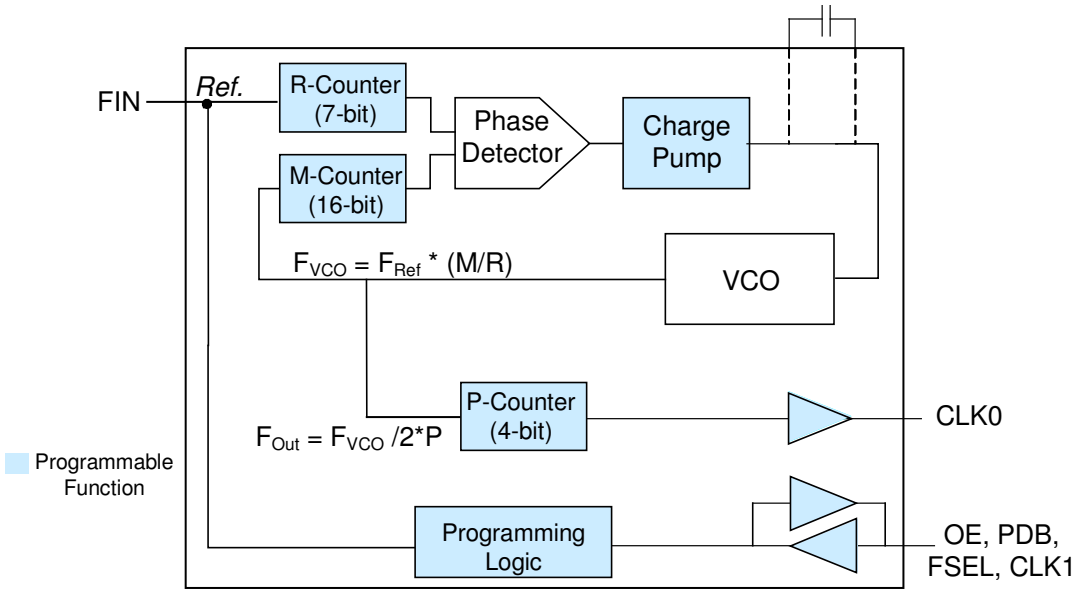


SC70-6L
(2.3mmx2.25mmx1.0mm)



SOT23-6L
(3.0mmx3.0mmx1.35mm)

BLOCK DIAGRAM



1.8V-3.3V PicoPLL™ KHz to MHz Programmable Clock

KEY PROGRAMMING PARAMETERS

CLK Output Frequency	Output Drive Strength	Programmable Input/Output
FOUT = FREF * (M / R) /(2*P) Where M=16 bit R= 7 bit P= 4 bit CLK0 = FOUT, FREF or FREF / (2*P) CLK1 = FREF, FREF/2, CLK0 or CLK0/2	Three optional drive strengths to choose from: • Low: 4mA • Std: 8mA (default) • High: 16mA	One output pin can be configured as: • OE - input • FSEL - input • PDB - input • CLK1 – output • HiZ or Active Low disabled state

PACKAGE PIN ASSIGNMENT

Name	Pin #			Type	Description
	SOT Pin#	SC70 Pin#	DFN Pin#		
VDD	1	2	3	P	VDD connection.
OE, PDB, FSEL, CLK1	2	1	2	I/O	This programmable I/O pin can be configured as Output Enable (OE) input, Power Down (PDB) input, Frequency Selector (FSEL) or CLK1 clock output. This pin has an internal 10MΩ pull up resistor (OE, PDB & FSEL Only). The OE and PDB features can be programmed to allow the output to float (Hi Z), or to operate in the 'Active low' mode.
FIN	3	3	1	I	Reference input pin.
LF	4	4	6	I	Loop Filter input pin.
GND	5	5	5	P	GND connection
CLK0	6	6	4	O	Programmable Clock Output

State	OE	PDB	FSEL
0	Disable CLK	Power Down Mode	Frequency '2'
1 (default)	Normal mode	Normal mode	Frequency '1'

FUNCTIONAL DESCRIPTION

PL611s-17 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power, small form-factor applications. The PL611s-17 accepts a reference clock input of 10kHz to 200MHz and is capable of producing two outputs up to 125MHz. This flexible design allows the PL611s-17 to deliver any PLL generated frequency, FREF (Ref Clk) frequency or FREF /(2*P) to CLK0 and/or CLK1. Some of the design features of the PL611s-17 are mentioned below:

PLL Programming

The PLL in the PL611s-17 is fully programmable. The PLL is equipped with an 7-bit input frequency divider (R-Counter), and an 16-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 4-bit post VCO divider (P-Counter). The output frequency is determined by the following formula [FOUT = FREF * (M / R) / (2 * P)].

Clock Output (CLK0)

CLK0 is the main clock output. The PL611s-17 can also be programmed to provide a second clock output, CLK1, on the programmable I/O pin (see OE/PDB/FSEL/CLK1 pin description below). The output of CLK0 can be configured as the PLL output (F_{VCO}/(2*P)), FREF (Ref Clk Frequency) output, or FREF/(2*P) output. The output drive level can be programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The maximum output frequency is 125MHz.

Clock Output (CLK1)

The CLK1 feature allows the PL611s-17 to have an additional clock output. This output can be programmed to one of the following:

FREF - Reference (Ref Clk) Frequency
FREF / 2
CLK0
CLK0 / 2

Output Enable (OE)

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 10MΩ pull up resistor giving a default condition of logic “1”.

The OE feature can be programmed to allow the output to float (Hi Z), or to operate in the ‘Active low’ mode.

Power-Down Control (PDB)

The Power Down (PDB) feature allows the user to put the PL611s-17 into “Sleep Mode”. When activated (logic ‘0’), PDB ‘Disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <10µA of power. The PDB pin incorporates a 10MΩ pull up resistor giving a default condition of logic “1”.

The PDB feature can be programmed to allow the output to float (Hi Z), or to operate in the ‘Active low’ mode.

Frequency Select (FSEL)

The Frequency Select (FSEL) feature allows the PL611s-17 to switch between two pre-programmed outputs allowing the device “On the Fly” frequency switching. The FSEL pin incorporates a 10MΩ pull up resistor giving a default condition of logic “1”.

APPLICATION RECOMMENDATIONS FOR PL611s-17

PL611s-17 can accept a reference input >10kHz and produce a clock output in the MHz range, as shown in the diagram '1', below. Also, to save costs in consumer product system designs and for greater area optimization, it is possible to use the XOUT of the RTC crystal (32.768KHz) as the reference input to the PL611s-17, as shown in diagram '2', below.

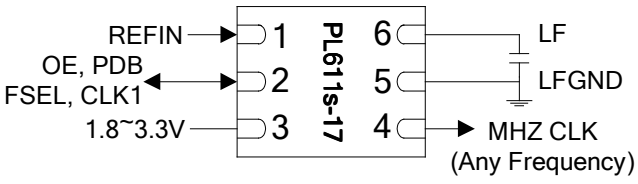


Diagram '1'

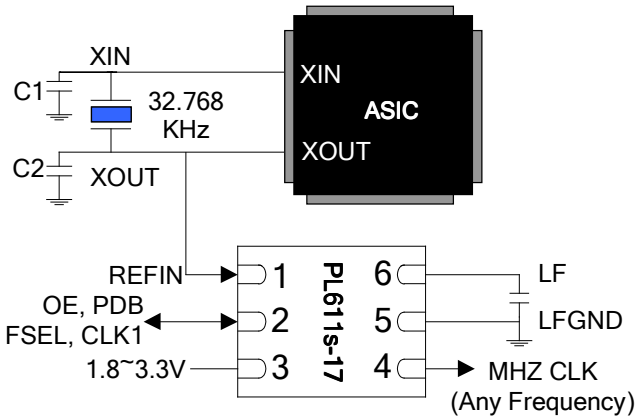


Diagram '2'

Note: An AC Coupling Cap may be required if RTC Clock amplitude is too small.

GUIDELINES FOR EXTERNAL COMPONENT SELECTION

For the optimum performance, an accurate external loop filter capacitor must be selected. A general guideline for selecting this component based on the input frequency is shown in the table below.

Input Frequency	Capacitor Value
3MHz ~ 200MHz	1.0nF
300KHz ~ 10MHz	1.0nF
30KHz ~ 1.0MHz	4.7nF
10KHz ~ 100KHz	47nF

The optimal way to choose the value is using the following formula:

C(nF) = 0.8 + M/280

Where C = Loop Filter Capacitor value (in nF)
M = M counter value. Provided by PhaseLink with device samples.

Notes:

* Find the closest commercially available value. Values in the E12 range with 5% tolerance are acceptable.
* With possible M-counter values between 1 and 65536, the capacitor value is expected in the range 820pF thru 220nF.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input (FIN) Frequency	@ V_{DD} =3.3V	10KHz		200	MHz
	@ V_{DD} =2.5V			166	
	@ V_{DD} =1.8V			133	
Input (FIN) Signal Amplitude	Internally AC/DC coupled (High Frequency)	0.9		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC/DC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz, 1.8V ≤15MHz	0.1		V_{DD}	Vpp
Output Frequency	@ V_{DD} =3.3V			125	MHz
	@ V_{DD} =2.5V			90	
	@ V_{DD} =1.8V			65	
Settling Time	At power-up (after V_{DD} increases over 1.62V)			2	ms
Output Enable Time	OE Function; Ta=25° C, 15pF Load			10	ns
	PDB Function; Ta=25° C, 15pF Load			2	ms
Output Rise Time	15pF Load, 10/90% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Output Fall Time	15pF Load, 90/10% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Duty Cycle	V_{DD} /2	45	50	55	%
Period Jitter, Pk-to-Pk* (measured from 10,000 samples)	With capacitive decoupling between V_{DD} and GND.		70		ps

* Note: Jitter performance depends on the programming parameters.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded CMOS Outputs	I_{DD}	@ V_{DD} =3.3V,30MHz, load=15pF		6.0		mA
Supply Current, Dynamic, with Loaded CMOS Outputs	I_{DD}	@ V_{DD} =2.5V,30MHz, load=15pF		3.9		mA
Supply Current, Dynamic with Loaded CMOS Outputs	I_{DD}	@ V_{DD} =1.8V,30MHz, load=5pF		2.1*		mA
Operating Voltage	V_{DD}		1.62		3.63	V
Output Low Voltage	V_{OL}	I_{OL} = +4mA Standard Drive			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Standard Drive	V_{DD} – 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Standard Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

PCB LAYOUT CONSIDERATIONS FOR PERFORMANCE OPTIMIZATION

The following guidelines are to assist you with a performance optimized PCB design:

- Keep all the PCB traces to PL611s-17 as short as possible, as well as keeping all other traces as far away from it as possible.

- When a reference input clock is generated from a crystal (see diagram above), place the PL611s-17 'FIN' as close as possible to the 'Xout' crystal pin. This will reduce the cross-talk between the reference input and the other signals.

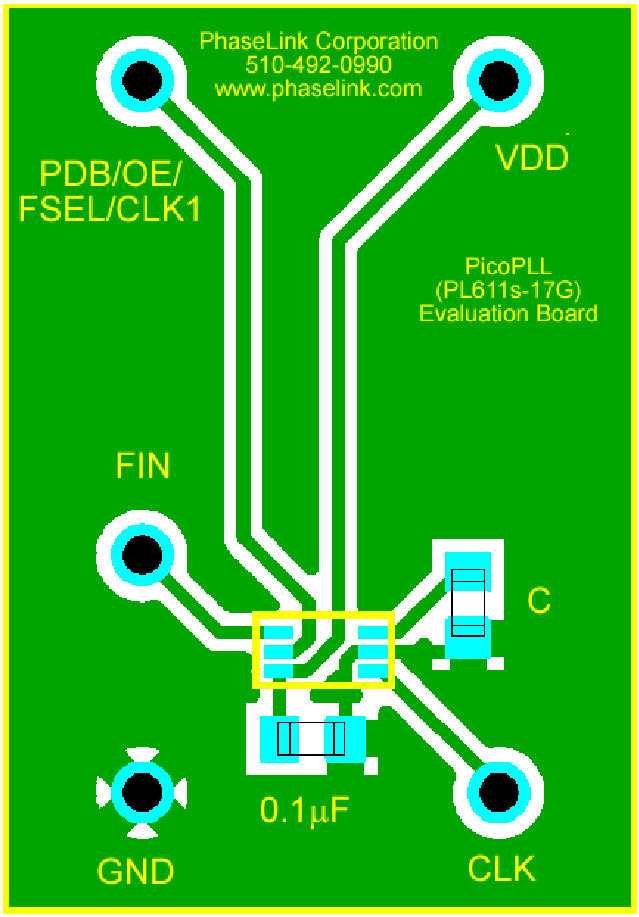
- Place the Loop Filter (LF) components as close to the package pin of PL611s-17 as possible.

- Place a 0.01µF~0.1µF decoupling capacitor between VDD and GND, on the component side of the PCB, close to the VDD pin. It is not recommended to place this component on the backside of the PCB. Going through vias will reduce the signal integrity, causing additional jitter and phase noise.

- It is highly recommended to keep the VDD and GND traces as short as possible.

- When connecting long traces (> 1 inch) to a CMOS output, it is important to design the traces as a transmission line or 'stripline', to avoid reflections or ringing. In this case, the CMOS output needs to be matched to the trace impedance. Usually 'striplines' are designed for 50Ω impedance and CMOS outputs usually have lower than 50Ω impedance so matching can be achieved by adding a resistor in series with the CMOS output pin to the 'stripline' trace.

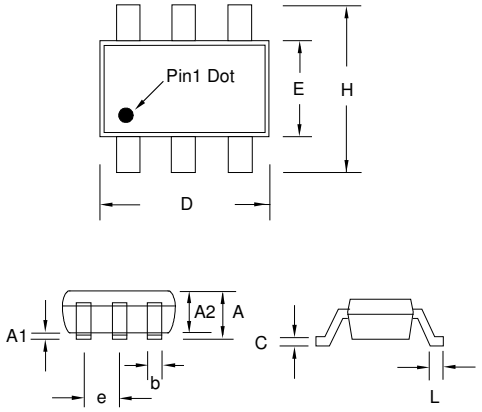
- Please contact PhaseLink for the application note on how to design outputs driving long traces or the Gerber files for the PL611s-17 layout.



PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

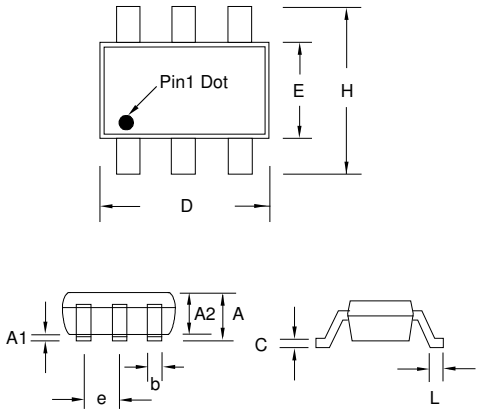
SOT23-6 L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.00
L	0.35	0.55
e	0.95 BSC	



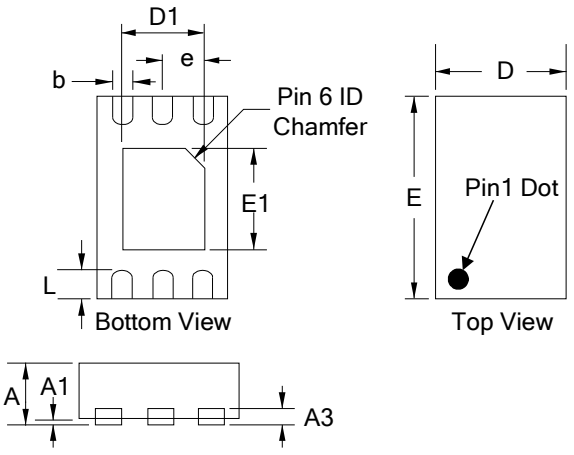
SC70-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.80	1.00
A1	0.00	0.09
A2	0.80	0.91
b	0.15	0.30
c	0.08	0.25
D	1.85	2.25
E	1.15	1.35
H	2.00	2.30
L	0.21	0.41
e	0.65BSC	



DFN-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.50	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30



ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL611s-17-XXX X X X

PART NUMBER

3 DIGIT ID Code *
(will be assigned at programming time)

PACKAGE TYPE
G=DFN-6L
U=SC70-6L
T=SOT-6L

NONE= TUBE
R=TAPE and REEL

TEMPERATURE
C=COMMERCIAL
I=INDUSTRIAL

Part/Order Number	Marking†	Package Option
PL611s-17-XXXGC-R	XXX	6-Pin DFN (Tape and Reel)
PL611s-17-XXXUC-R	XXX	6-Pin SC70 (Tape and Reel)
PL611s-17-XXXTC-R	17XXX	6-Pin SOT23 (Tape and Reel)

† Note: 'XXX' designates marking identifier that could be independent of the part number.

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Phaselink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY: PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.

Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf