Low-Power Programmable Quick Turn Clock™

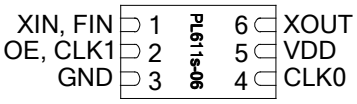
FEATURES

- Advanced low-power, space saving programmable PLL design
- Very low Jitter and Phase Noise (30-70ps Pk-Pk typical)
- Up to 2 programmable clock outputs
- CMOS output frequency up to 35MHz.
- Accepts Crystal or Ref Clock input
  - Fundamental Crystal: 10MHz to 30MHz
  - Reference Input: 1MHz to 100MHz
- Accepts >0.1V reference signal input voltage
- Single 1.8V, 2.5V, or 3.3V ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 6-pin DFN, SC70, and SOT23, **GREEN** /RoHS compliant packages

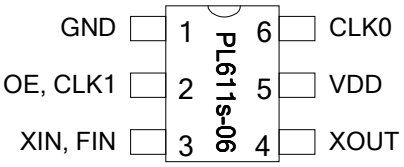
DESCRIPTION

The PL611s-06 is a low-power general purpose frequency synthesizer and a member of PhaseLink's Programmable 'Quick Turn Clock (QTC)' family. PhaseLink's PL611s-06 can generate two system clock frequencies of up to 35MHz from a 10MHz to 30MHz fundamental crystal or a 1MHz to 100MHz Reference clock source. The PL611s-06 offers the best phase noise and jitter performance, and power consumption of its rivals. Cascading of the ICs to produce additional clock frequencies is also supported.

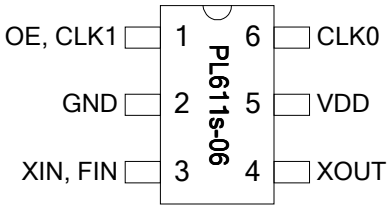
PACKAGE PIN CONFIGURATION



DFN-6L
(2.0mmx1.3mmx0.6mm)

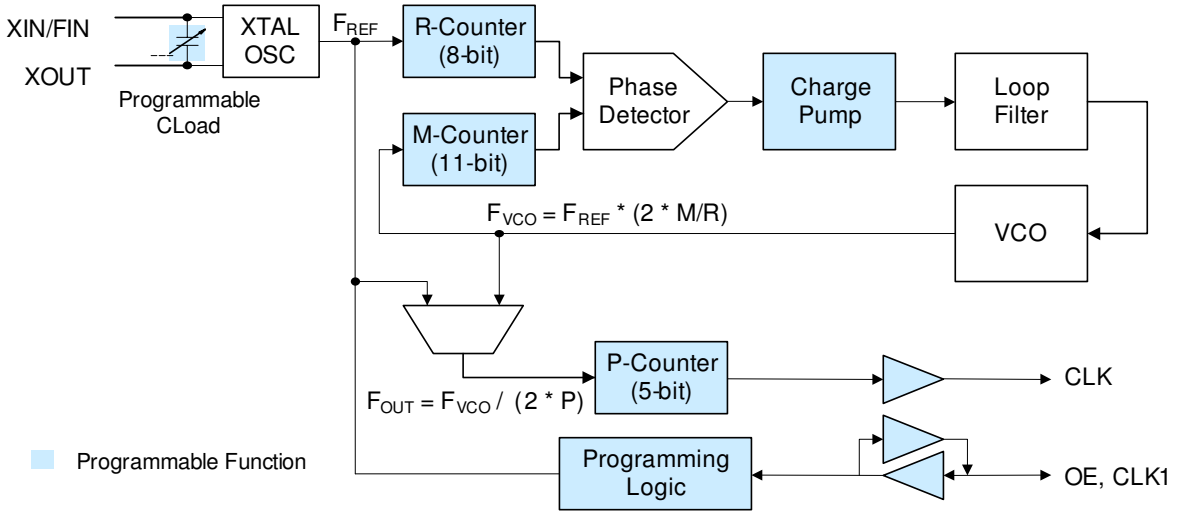


SC70-6L
(2.3mmx2.25mmx1.0mm)



SOT23-6L
(3.0mmx3.0mmx1.35mm)

BLOCK DIAGRAM



KEY PROGRAMMING PARAMETERS

CLK Output Frequency	Output Drive Strength	Programmable Input/Output
FOUT = FREF * M / (R * P) Where M = 11 bit R = 8 bit P = 5 bit CLK0 = FOUT, FREF or FREF / (2*P) CLK1 = FREF, FREF/2, CLK0 or CLK0/2	Three optional drive strengths to choose from: • Low: 4mA • Std: 8mA (default) • High: 16mA	One output pin can be configured as: • OE - input • CLK1 – output

PACKAGE PIN ASSIGNMENT

Name	Pin Assignment			Type	Description
	SOT23 Pin #	SC70 Pin#	DFN Pin#		
OE, CLK1	1	2	2	B	This programmable I/O pin can be configured as an Output Enable (OE) input, or CLK1 output. This pin has an internal 60KΩ pull up resistor (OE Function Only).
GND	2	1	3	P	GND connection
XIN, FIN	3	3	1	I	Crystal or Reference input pin
XOUT	4	4	6	O	Crystal Output pin
					Do Not Connect (DNC) when FIN is present
VDD	5	5	5	P	VDD connection
CLK0	6	6	4	O	Programmable Clock Output

FUNCTIONAL DESCRIPTION

PL611s-06 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power, small form-factor applications. The PL611s-06 accepts a fundamental crystal input of 10MHz to 30MHz or reference clock input of 1MHz to 100MHz and is capable of producing two outputs up to 35MHz. This flexible design allows the PL611s-06 to deliver any PLL generated frequency, FREF (Crystal or Ref Clk) frequency or FREF/2 to CLK0 and/or CLK1. Some of the design features of the PL611s-06 are mentioned below:

PLL Programming

The PLL in the PL611s-06 is fully programmable. The PLL is equipped with an 8-bit input frequency divider (R-Counter), and an 11-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 5-bit post VCO divider (P-Counter). The output frequency is determined by the following formula [FOUT = FREF * M / (R * P)].

Clock Output (CLK0)

CLK0 is the main clock output. The output of CLK0 can be configured as the PLL output (FVCO/(2*P)), FREF (Crystal or Ref Clk Frequency) output, or FREF/2 output. The output drive level can be programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The maximum output frequency is 35MHz.

Clock Output (CLK1)

The CLK1 feature allows the PL611s-06 to have an additional clock output. This output can be programmed to one of the following:

FREF - Reference (Crystal or Ref Clk) Frequency
FREF / 2
CLK0
CLK0 / 2

Output Enable (OE)

The Output Enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a 60kΩ pull up resistor giving a default condition of logic “1”.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency (XIN)	Fundamental Crystal	10		30	MHz
Input (FIN) Frequency	@ V_{DD} =3.3V	1		100	MHz
	@ V_{DD} =2.5V				
	@ V_{DD} =1.8V				
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.9		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz, 1.8V ≤15MHz	0.1		V_{DD}	Vpp
Output Frequency	@ V_{DD} =3.3V			35	MHz
	@ V_{DD} =2.5V				MHz
	@ V_{DD} =1.8V				MHz
Settling Time	At power-up (after V_{DD} increases over 1.62V)			2	ms
Output Enable Time	OE Function; Ta=25° C, 15pF Load			10	ns
	PDB Function; Ta=25° C, 15pF Load			2	ms
VDD Sensitivity	Frequency vs. V_{DD} +/-10%	-2		2	ppm
Output Rise Time	15pF Load, 10/90% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Output Fall Time	15pF Load, 90/10% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Duty Cycle	PLL Enabled, @ V_{DD} /2	45	50	55	%
Period Jitter,Pk-to-Pk* (measured from 10,000 samples)	With capacitive decoupling between V_{DD} and GND.		70		ps

* Note: Jitter performance depends on the programming parameters.

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded CMOS Outputs	I_{DD}	@ V_{DD} =3.3V, 27MHz, load=15pF		5.5		mA
Supply Current, Dynamic, with Loaded CMOS Outputs	I_{DD}	@ V_{DD} =2.5V, 27MHz, load=15pF		3.5		mA
Supply Current, Dynamic with Loaded CMOS Outputs	I_{DD}	@Vdd=1.8V,27MHz, load=5pF		1.8		mA
Supply Current, Dynamic, with Loaded CMOS Outputs	I_{DD}	When PDB=0			<10	µA
Operating Voltage	V_{DD}		1.62		3.63	V
Output Low Voltage	V_{OL}	I_{OL} = +4mA Standard Drive			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Standard Drive	V_{DD} – 0.4			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Standard Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

* Note: Please contact PhaseLink, if super low-power is required.

CRYSTAL SPECIFICATIONS

PARAMETERS		SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency		F_{XIN}	10		30	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)		$C_{L\ (xtal)}$	8		12	pF
Maximum Sustainable Drive Level					100	µW
Operating Drive Level				30		µW
Metal Can Crystal	Shunt Capacitance	C0			5.5	pF
	ESR Max	ESR			50	Ω
Small SMD Crystal	Shunt Capacitance	C0			2.5	pF
	ESR Max	ESR			80	Ω

LAYOUT RECOMMENDATIONS

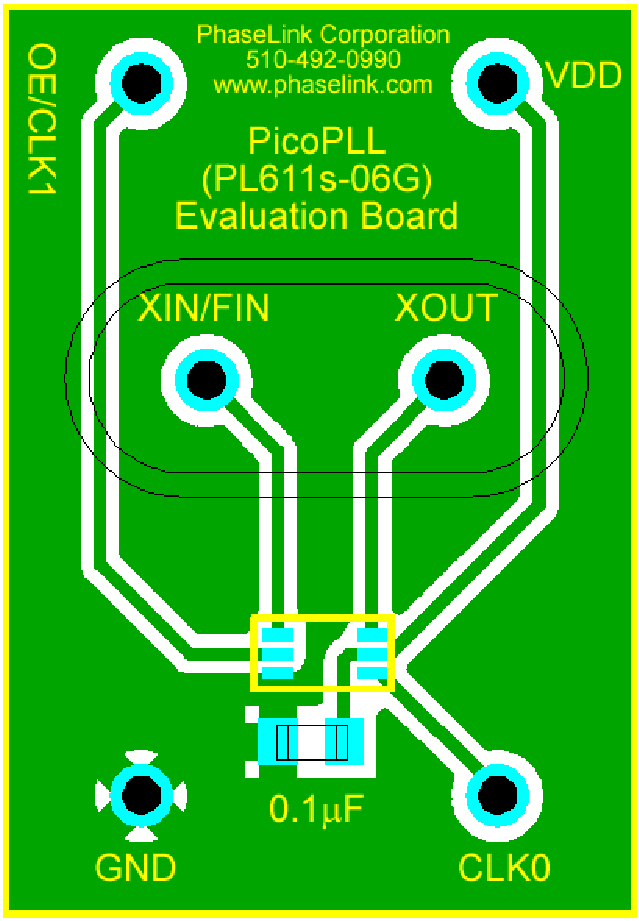
The following guidelines are to assist you with a performance optimized PCB design:

- Keep all the PCB traces to the PL611s-06 as short as possible, as well as keeping all other traces as far away from it as possible.

- Place a 0.01µF~0.1µF decoupling capacitor between VDD and GND, on the component side of the PCB, close to the VDD pin. It is not recommended to place this component on the backside of the PCB. Going through vias will reduce the signal integrity, causing additional jitter and phase noise.

- It is highly recommended to keep the VDD and GND traces as short as possible.

- When connecting long traces (> 1 inch) to a CMOS output, it is important to design the traces as a transmission line or 'stripline', to avoid reflections or ringing. In this case, the CMOS output needs to be matched to the trace impedance. Usually 'striplines' are designed for 50Ω impedance and CMOS outputs usually have lower than 50 Ω impedance so matching can be achieved by adding a resistor in series with the CMOS output pin to the 'stripline' trace.
- Please contact PhaseLink for additional information on how to design outputs driving long traces or for the Gerber files for the PL611s-06 eval board shown.

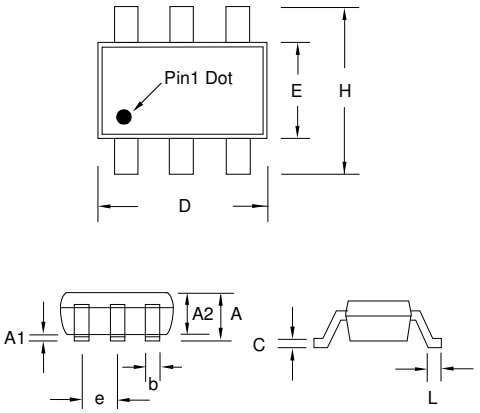


DFN-6L Evaluation Board

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

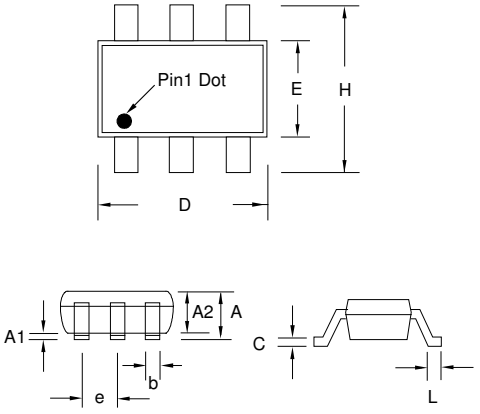
SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.0
L	0.35	0.55
e	0.95 BSC	



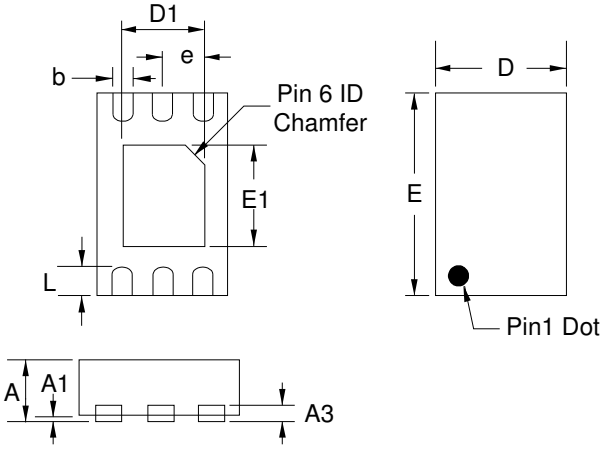
SC70-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.80	1.00
A1	0.00	0.09
A2	0.80	0.91
b	0.15	0.30
c	0.08	0.25
D	1.85	2.25
E	1.15	1.35
H	2.00	2.30
L	0.21	0.41
e	0.65BSC	



DFN-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.50	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30



ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL611s-06-XXX X X X

PART NUMBER

3 DIGIT ID Code *
(will be assigned at programming time)

PACKAGE TYPE
G=DFN-6L
U=SC70-6L
T=SOT-6L

NONE= TUBE
R=TAPE and REEL

TEMPERATURE
C=COMMERCIAL
I=INDUSTRIAL

Part Number/Order Number	Marking†	Package Option
PL611s-06-XXXGC-R	XXX	6-Pin DFN (Tape and Reel)
PL611s-06-XXXUC-R	XXX	6-Pin SC70 (Tape and Reel)
PL611s-06-XXXTC-R	06XXX	6-Pin SOT23 (Tape and Reel)

† Note: 'XXX' designates marking identifier that could be independent of the part number.

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Solder reflow profile available at www.phaselink.com/QA/solderingGreen.pdf