

Low Phase Noise XO (for 3rd O.T.) For 65-130MHz

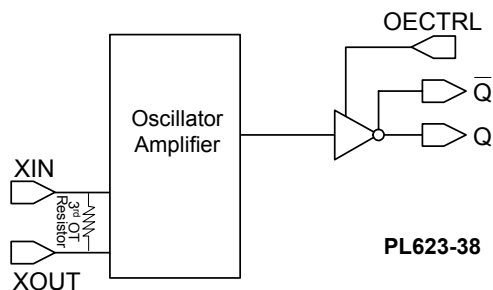
FEATURES

- Input: 65-130MHz 3rd Overtone or fundamental Crystal
- Output frequency: Up to 130MHz
- Selectable /2, /4, /8 output dividers with 60KΩ pull up resistor on the selector pins
- Available output: PECL
- Supports 2.5V or 3.3V-Power Supply
- Available in die form

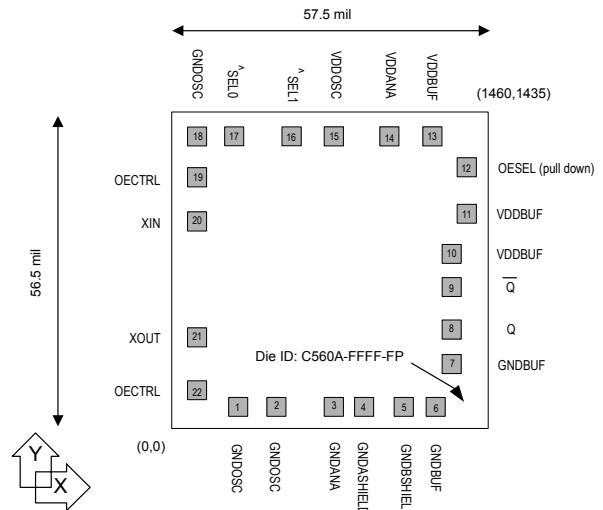
DESCRIPTION

PL623-38 is an XO IC specifically designed to work with high frequency 3rd overtone or fundamental crystals from 65MHz to 135MHz. It requires an external resistor for the 3rd overtone selection. Its design was optimized to tolerate higher limits of inter-electrodes capacitance and bonding capacitance to improve yield. It achieves very low current into the crystal resulting in better overall stability. It is ideal for XO applications requiring PECL output levels at high frequencies.

BLOCK DIAGRAM



DIE CONFIGURATION



Note: 'A' Denotes 60kΩ pull-up resistor

DIE SPECIFICATIONS

Name	Value
Size	57.5 x 56.5 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

OE SELECTION

Pad #12 OESEL	Pad #22 OECTRL	State
1	0	Tri-state
	1	Output enabled (default)
0 (default)	0	Output enabled (default)
	1	Tri-state

Pad #12: Bond to VDD to set to "1"

Pad #22: Logical states defined by PECL levels

OUTPUT DIVIDER SELECTOR LOGIC

SEL 0	SEL 1	Output
0	0	No Divider
1	0	Divide by 2
0	1	Divide by 4
1	1	Divide by 8

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DIE PAD ASSIGNMENT

Pad #	Name	X (μm)	Y (μm)	Pad Description
1	GNDOSC	329.6	110.1	GND connection for oscillator circuitry.
2	GNDOSC	498.3	110.0	GND connection for oscillator circuitry.
3	GNDANA	696.2	110.0	GND connection for analog circuitry.
4	GNDSHIELD	825.0	110.0	GND shielding connection.
5	GNDSHIELD	973.6	110.0	GND shielding connection.
6	GNDBUF	1150.0	109.1	GND connection for output buffer circuitry.
7	GNDBUF	1183.6	302.2	GND connection for output buffer circuitry.
8	Q	1183.6	452.3	PECL output.
9	QBAR	1183.6	613.5	Complementary PECL output.
10	VDDBUF	1182.4	745.9	VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
11	VDDBUF	1252.4	903.6	VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
12	OESEL	1252.4	1081.3	This is the selector input to choose the OE control logic to be applied, as presented on the OE SELECTION TABLE on page '1'.
13	VDDBUF	1058.5	1221.6	VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
14	VDDANA	864.5	1221.6	VDD connection for analog circuitry. VDDANA should be separately decoupled from other VDDs whenever possible.
15	VDDOSC	624.0	1222.7	VDD connection for oscillator circuitry. VDDOSC should be separately decoupled from other VDDs whenever possible.
16	SEL1	467.1	1222.6	Output Divider Selector pin as presented on the DIVIDER SELECTOR TABLE on page '1'.
17	SEL0	271.1	1222.6	Output Divider Selector pin as presented on the DIVIDER SELECTOR TABLE on page '1'.
18	GNDOSC	109.4	1222.9	GND connection for oscillator circuitry.
19	OCTRL	108.9	1062.1	Output Enable input pad. See OE SELECTION TABLE on page 1.
20	XIN	109.0	865.8	Crystal connector pad. This pad is the input of the crystal oscillator circuitry. The crystal should be mounted as close to the IC as possible, with minimum parasitic capacitance.
21	XOUT	108.6	358.4	Crystal connector pad. This pad is the input of the crystal oscillator circuitry. The crystal should be mounted as close to the IC as possible, with minimum parasitic capacitance.
22	OCTRL	108.6	146.5	Output Enable input pad. See OE SELECTION TABLE on page 1.

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EXTERNAL COMPONENT VALUES – 3RD OVERTONE RESISTOR SELECTIONS

This resistor is only required when a third overtone crystal is used. The chart below indicates the calculated and the nearest “E12” resistor values versus frequency for PL623-38.

Frequency (MHz)	R30T (Ω)	E12 Pick KΩ
65	2,162	2.2
67.5	2,082	2.2
70	2,008	2.2
75	1,875	1.8
77.5	1,815	1.8
80	1,758	1.8
82.5	1,705	1.8
85	1,654	1.8
87.5	1,607	1.5
90	1,563	1.5
92.5	1,520	1.5
95	1,480	1.5
97.5	1,442	1.5

Frequency (MHz)	R30T (Ω)	E12 Pick KΩ
100	1,406	1.5
102.5	1,372	1.5
105	1,339	1.2
107.5	1,308	1.2
110	1,278	1.2
112.5	1,250	1.2
115	1,223	1.2
117.5	1,197	1.2
120	1,172	1.2
122.5	1,148	1.2
125	1,125	1.2
127.5	1,103	1.2
130	1,082	1.0

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V _{DD}		4.6	V
Input Voltage, dc	V _I	V _{SS} -0.5	V _{DD} +0.5	V
Output Voltage, dc	V _O	V _{SS} -0.5	V _{DD} +0.5	V
Storage Temperature	T _S	-65	150	°C
Ambient Operating Temperature	T _A	-40	+85	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

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2. Crystal Specifications

Name	Symbol	Conditions	Min.	Max.	Units
Parallel Resonant mode		3 rd Overtone			N/A
Load capacitance (capacitance on built-in on die seen by crystal)	C _L	Die only, no bond wire, no package		5	pF
Inter-electrode capacitance	C ₀			4	pF
Equivalent Series Resistance	ESR			35	Ω
Oscillation Frequency		3 rd Overtone	65	130	MHz

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I _{DD}	PECL			85/55	mA
Operating Voltage	V _{DD}		2.25		3.63	V
Output Clock Duty Cycle		@ V _{dd} – 1.3V (PECL)	45	50	55	%
Short Circuit Current				±50		mA

4. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS at 106.25MHz	With capacitive decoupling between VDD and GND.		2.0		ps
Period jitter peak-to-peak at 106.25MHz			17.0		
Integrated jitter RMS at 106.25MHz	Integrated 12 kHz to 20 MHz		0.3*		ps

*Measured on Agilent E5500.

5. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise vs. carrier with fund. crystal.	106.25MHz	-55	-90	-110	-135	-145	dBc/Hz

*: Note: Phase noise to be measured. Based on P520-20 product (fundamental 155MHz VCXO).

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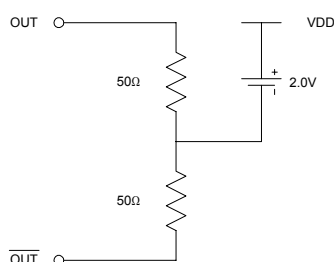
8. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	$R_L = 50\ \Omega$ to ($V_{DD} - 2V$) (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	V_{OL}			$V_{DD} - 1.620$	V

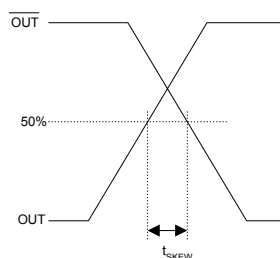
9. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.2	0.4	ns
Clock Fall Time	t_f	@80/20% - PECL		0.2	0.4	ns

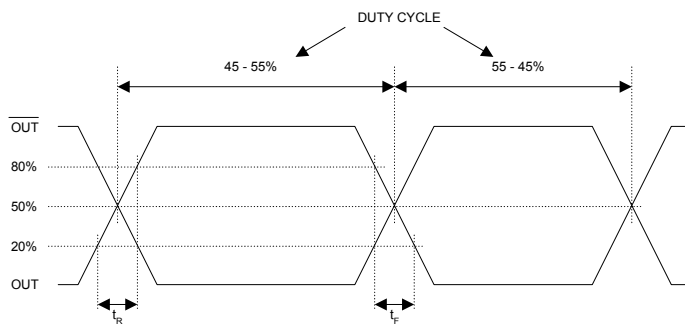
PECL Levels Test Circuit



PECL Output Skew



PECL Transition Time Waveform



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ORDERING INFORMATION

For part ordering, please contact our Sales Department:

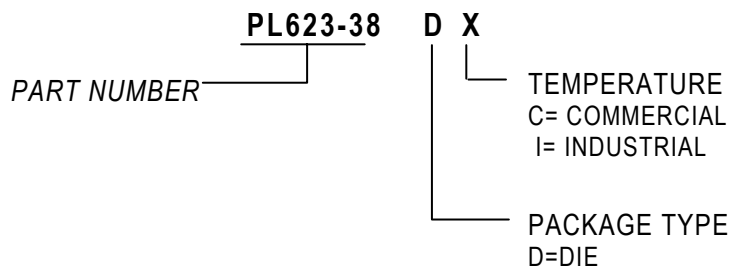
47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:

Device number, Package type and Operating temperature range



<u>Order Number</u>	<u>Marking</u>	<u>Package Option</u>
PL623-38DC	P623-38	Waffle Pack

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