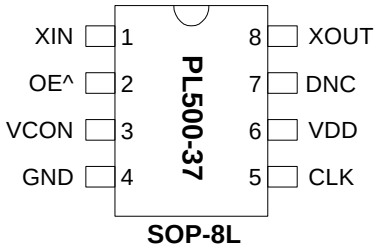
Low Phase Noise VCXO (36MHz to 130MHz)

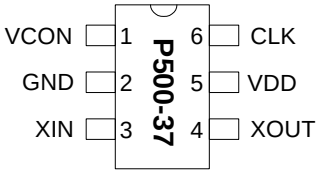
FEATURES

- VCXO output for the 36MHz to 130MHz range
- Low phase noise (-148 dBc @ 10kHz offset at 77.76MHz).
- CMOS output with OE tri-state control.
- 36 to 130MHz fundamental crystal input.
- Integrated high linearity variable capacitors.
- 8mA drive capability at TTL output.
- +/- 150 ppm pull range, max 5% linearity.
- Low jitter (RMS): 2.5ps period jitter.
- Single 2.5V ±10% or 3.3V ±10 power supply.
- Operating temperature range from -40°C to +85°C
- Available in Die or Wafer form or SOP-8L or SOT23-6L packaging.

PIN AND PAD CONFIGURATION



SOP-8L



SOT23-6L

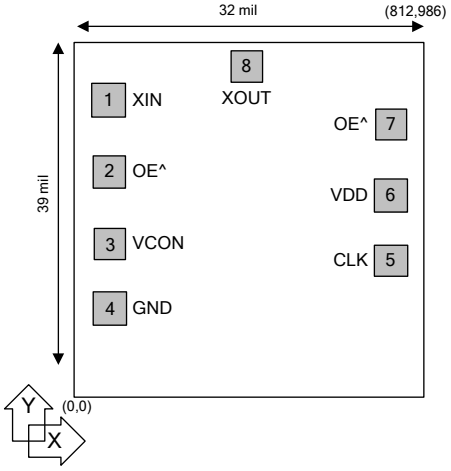
^: Denotes internal Pull-up

DESCRIPTION

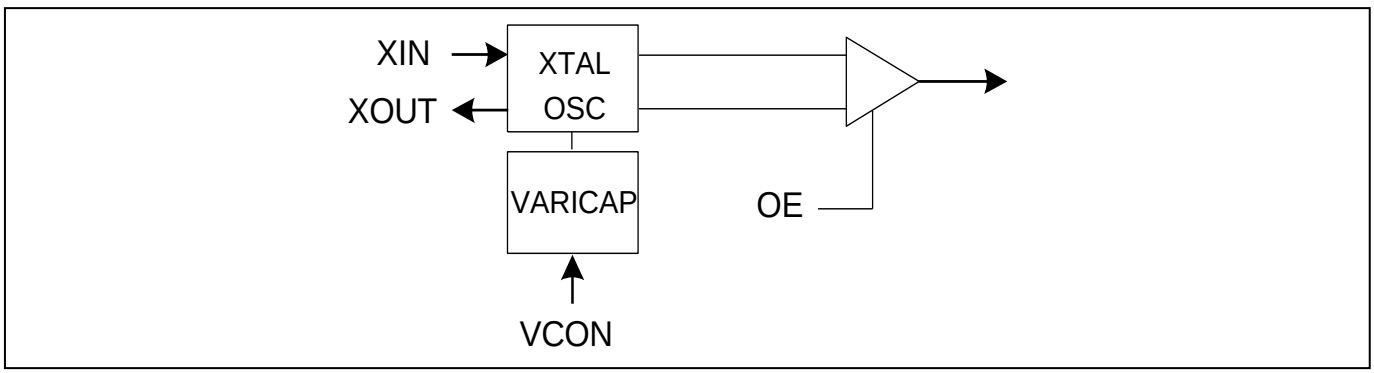
The PL500-37 is a low cost, high performance and low phase noise VCXO for the 36 to 130MHz range, providing less than -148dBc at 10kHz offset at 77.76MHz. The very low jitter (2.5 ps RMS period jitter) makes this chip ideal for applications requiring voltage controlled frequency sources. The input crystal frequency can range from 36 to 130MHz (fundamental resonant mode).

DIE SPECIFICATIONS

Name	Value
Size	39 x 32 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	8 mil



BLOCK DIAGRAM



PIN AND PAD ASSIGNMENT AND DESCRIPTION

Name	Pin#		Die Pad Position		Type	Description
	SOP-8	SOT23-6	X (µm)	Y (µm)		
XIN	1	3	94.183	768.599	I	Crystal input pin.
OE	2	-	94.157	605.029	I	Output Enable input pin. Disables the output when low. Internal pull-up enables output by default if pin is not connected to low. Use only one OE signal.
	-	-	715.472	626.716		
VCON	3	1	94.183	331.756	I	Frequency control voltage input pin.
GND	4	2	94.193	140.379	P	Ground pin.
CLK	5	6	715.472	203.866	O	Output clock pin.
VDD	6	5	715.307	455.726	P	VDD power supply pin. Only one VDD pin is necessary.
DNC	7	-	-	-	I	Do Not Connect. No Internal Connection.
XOUT	8	4	476.906	888.881	I	Crystal output pin.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			36		130	MHz
Output Clock Rise/Fall Time		0.8V ~ 2.0V, 10 pF load		1.15		ns
		0.3V ~ 3.0V, 15 pF load		3.7		
Output Clock Duty Cycle		Measured @ 1.4V	45	50	55	%
Short Circuit Current				±50		mA

3. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	78MHz, 15pF output load, 3.3V		7.2	9	mA
		78MHz, 15pF output load, 2.5V		5.2	7	
Allowable output load capacitance	C_L (Output)	8mA drive up to 100MHz			15	pF
Operating Voltage	V_{DD}		2.25		3.63	V
Output Low Voltage at CMOS level	V_{OLC}	I_{OL} = +4mA			0.4	V
Output High Voltage at CMOS level	V_{OHC}	I_{OH} = -4mA	V_{DD} – 0.4			V
Output drive current		For V_{OL}<0.4V or V_{OH}>2.4V	8			mA
Short Circuit Current				±50		mA
VCXO Control Voltage	V_{CON}		0		V_{DD}	V

4. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		F_{XIN} = 36 – 130MHz; XTAL C_0/C_1 < 250 $0V \le V_{CON} \le 3.3V$		300		ppm
CLK output pullability		V_{CON}=1.65V, ±1.65V	±150			ppm
VCXO Tuning Characteristic				100		ppm/V
Pull range linearity					5	%
Power Supply Rejection	PWSRR	Frequency change with V_{DD} varied +/- 10%	-1		+1	ppm
VCON pin input impedance			5000			kΩ
VCON modulation BW		$0V \le V_{CON} \le 3.3V$, -3dB	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

5. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}		36		130	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$ (see note below)	VCON = 1.65V, 3.3 V		5.1		pF
		VCON = 1.25V, 2.5V		5.7		
Maximum Sustainable Drive Level					200	W
Operating Drive Level				50		W
Max C0					2.5	pF
C0/C1					250	-
ESR	R_S	C0 ≤ 2.0pF, F_{XIN} up to 85MHz C0 ≤ 2.5pF, F_{XIN} up to 80MHz C0 ≤ 3.0pF, F_{XIN} up to 75MHz			30	
		C0 ≤ 2.0pF, F_{XIN} up to 95MHz C0 ≤ 2.5pF, F_{XIN} up to 90MHz C0 ≤ 3.0pF, F_{XIN} up to 85MHz			25	
		C0 ≤ 2.0pF, F_{XIN} up to 110MHz C0 ≤ 2.5pF, F_{XIN} up to 105MHz C0 ≤ 3.0pF, F_{XIN} up to 100MHz			20	
		C0 ≤ 2.0pF, F_{XIN} up to 130MHz C0 ≤ 2.5pF, F_{XIN} up to 120MHz C0 ≤ 3.0pF, F_{XIN} up to 115MHz			15	

Note: The crystal must be such that it oscillates (parallel resonant) at nominal frequency when presented a C Load as specified above.
If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range.
Note that the Cload values above are for the IC only, and do not include PCB parasitics. Crystal specifications for Cload include PCB parasitics.

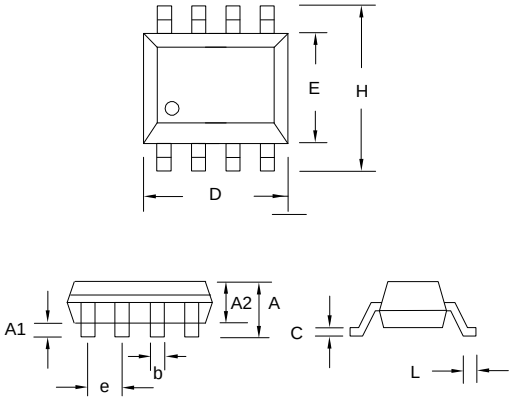
6. Jitter and Phase Noise Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	With capacitive decoupling between VDD and GND.		2.5		ps
Phase Noise relative to carrier	77.76MHz @100Hz offset		-100		dBc/Hz
Phase Noise relative to carrier	77.76MHz @1kHz offset		-125		dBc/Hz
Phase Noise relative to carrier	77.76MHz @10kHz offset		-142		dBc/Hz
Phase Noise relative to carrier	77.76MHz @100kHz offset		-150		dBc/Hz
Phase Noise relative to carrier	77.76MHz @1MHz offset		-152		dBc/Hz

PACKAGE INFORMATION (GREEN PACKAGE COMPLIANT)

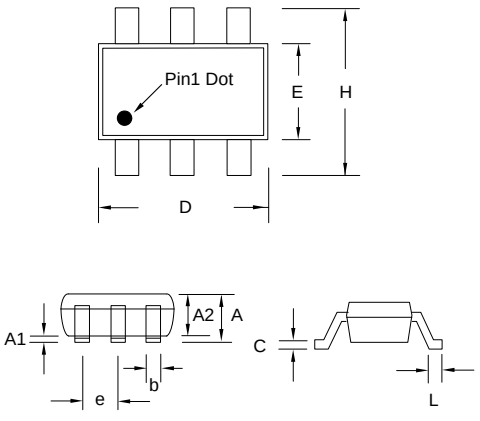
SOP-8L

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	



SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.0
L	0.35	0.55
e	0.95 BSC	



Low Phase Noise VCXO (36MHz to 130MHz)

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL500-37 X X

PART NUMBER

PACKAGE TYPE
W= Wafer
D= DIE
S=SOP-8L
T=SOT23-6L

TEMPERATURE
C=COMMERCIAL
I=INDUSTRIAL

Part / Order Number	Marking	Package Option
PL500-37DC	N/A	Die (Waffle Pack)
PL500-37WC	N/A	Wafer
PL500-37SC	P500-37 SC LLLLL	8-Pin SOP GREEN (Tube)
PL500-37SC-R		8-Pin SOP GREEN (Tape and Reel)
PL500-37TC-R	B37 LLL	6-Pin SOT GREEN (Tape and Reel)

Note: LLL / LLLLL designate Production Lot.

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