PL138-18

2.5V-3.3V Low-Skew 1:10 Differential PECL Fanout Buffer

FEATURES

- Ten differential 2.5V/3.3V LVPECL output pairs.
- Output Frequency: ≤ 700 MHz.
- Two selectable differential input pairs.
- Translates any standard single-ended or differential input format to LVPECL output. It can accept the following standard input formats and more:
  - LVPECL, LVCMOS, LVDS, HCSL, SSTL, LVHSTL, CML.
- Output Skew: 25ps (typ.).
- Part-to-part skew: 140ps (typ.).
- Propagation delay: 1.5ns (typ.).
- Additive Jitter: <100 fs (typ.).
- Operating Supply Voltage: 2.375V ~ 3.63V.
- Operating temperature range from -40°C to 85°C.
- Package availability: 32-pin LQFP.

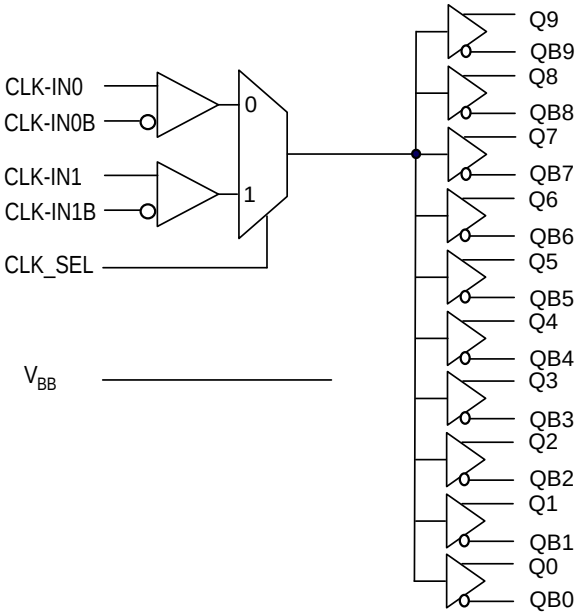
DESCRIPTION

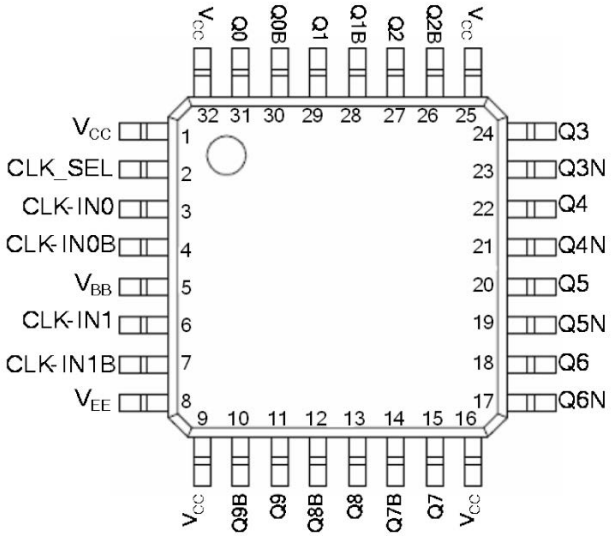
The PL138-18 family is a high performance low-cost 1: 10 outputs Differential LVPECL fanout buffer.

The family of Differential LVPECL buffers are designed to operate from a single power supply of 2.5V±5% or 3.3V±10%. The differential input pairs are designed to accept most standard input signal levels, using an appropriate resistor bias network, and produce a high quality set of outputs with the lowest possible skew on the outputs, which is guaranteed for part-to-part or lot-to lot skew.

Designed to fit in a small form-factor package, PL138 family offers up to 1GHz of output operation with very low-power consumption, and lowest additive jitter of any comparable device. The Output Enable feature, when activated, allows the IC to consume less than 10µA of current.

BLOCK DIAGRAM



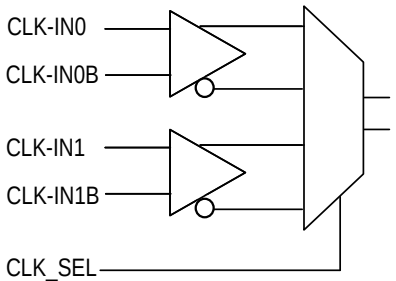


32-Pin LQFP Package

PIN DESCRIPTIONS

Name	Package Pin # LQFP-32	Type	Description
Vcc	1, 9, 16, 25, 32	P	Power Supply pin connection
CLK_SEL	2	P	Clock select input. See table below for functional spec. and Single Ended signal interface.
CLK-IN0	3	I	True part of differential clock input signal.
CLK-IN0B	4	I	Complementary part of differential clock input signal.
V_{BB}	5	O	Bias Reference Output
CLK-IN1	6	I	True part of differential clock input signal.
CLK-IN1B	7	I	Complementary part of differential clock input signal.
V_{EE}	8	P	Power Supply pin connection
Q0 ~ Q9	11, 13, 15, 18, 20, 22, 24, 27, 29, 31	O	LVPECL True output
QB0 ~ QB9	10, 12, 14, 17, 19, 21, 23, 26, 28, 30	O	LVPECL Complementary output

INPUT LOGIC BLOCK DIAGRAM



INPUT PIN CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units
Input Pulldown Resistor		75		kΩ
Pullup/Pulldown Resistors		50		kΩ

INPUT CLOCK CONTROL SELECTION

CLK_SEL	Selected Source
0	CLK-IN0, CLK-IN0B
1	CLK-IN1, CLK-IN1B

INPUT CLOCK FUNCTION

Inputs		Outputs		Input to Output Mode	Polarity
CLK-IN0 or CLK-IN1	CLK-IN0B or CLK-IN1B	Q0:Q7	QB0:QB7		
0	1	Low	High	Differential to Differential	Non Inverting
1	0	High	Low	Differential to Differential	Non Inverting
0	See page 8 for accepting SE input	Low	High	Single Ended to Differential	Non Inverting
1		High	Low	Single Ended to Differential	Non Inverting

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		110	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model	2			kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

DC CHARACTERISTICS, VCC = 3.3V; VEE = 0V

Parameter		Symbol	-40°C			25°C			80°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output High Voltage*		V_{OH}	2.215	2.320	2.420	2.275	2.350	2.420	2.275	2.35	2.420	V
Output Low Voltage*		V_{OL}	1.470	1.610	1.745	1.490	1.585	1.680	1.490	1.585	1.680	V
Input High Voltage		V_{IH}	2.075		2.420	2.135		2.420	2.135		2.420	V
Input Low Voltage		V_{IL}	1.470		1.890	1.490		1.825	1.490		1.825	V
Output Voltage Reference**		V_{BB}	1.86		1.98	1.92		2.04	1.92		2.04	V
Peak-to-Peak Input Voltage		V_{PP}	150	800	1200	150	800	1200	150	800	1200	V
Input High Voltage Common Mode Range† ††		V_{CMR}	1.2		3.3	1.2		3.3	1.2		3.3	V
Input High Current	CLK-IN0, CLK-IN1 CLK-IN0B, CLK-IN1B	I_{IH}			75			75			75	µA
Input Low Current		I_{IL}	-75			-75			-75			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.

* Outputs terminated with 50Ω to V_{CCO} – 2V.

** Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.

† Common mode voltage is defined as V_{IH}.

†† For single-ended applications, the maximum input voltage for CLK-INx, CLK-INxB is V_{CC} + 0.3V

DC CHARACTERISTICS, VCC = 2.5V; VEE = 0V

Parameter		Symbol	-40°C			25°C			80°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output High Voltage*		VOH	1.415	1.520	1.620	1.475	1.550	1.620	1.475	1.55	1.620	V
Output Low Voltage*		VOL	0.670	0.810	0.945	0.690	0.785	0.880	0.690	0.785	0.880	V
Input High Voltage		VIH	1.275		1.620	1.335		1.620	1.335		1.620	V
Input Low Voltage		VIL	0.670		1.090	0.690		1.025	0.690		1.025	V
Peak-to-Peak Input Voltage		VPP	150	800	1200	150	800	1200	150	800	1200	V
Input High Voltage Common Mode Range†		VCMR	1.2		2.5	1.2		2.5	1.2		2.5	V
Input High Current	CLK-IN0, CLK-IN1 CLK-IN0B, CLK-IN1B	IIH			60			60			60	µA
Input Low Current		IIL	-60			-60			-60			µA

Input and output parameters vary 1:1 with VCC. VEE can vary +0.925V to -0.5V.
* Outputs terminated with 50Ω to VCCO – 2V.
** Common mode voltage is defined as V_{IH}.
† For single-ended applications, the maximum input voltage for CLK-INx, CLK-INxB is V_{CC} + 0.3V

AC Electrical Characteristics

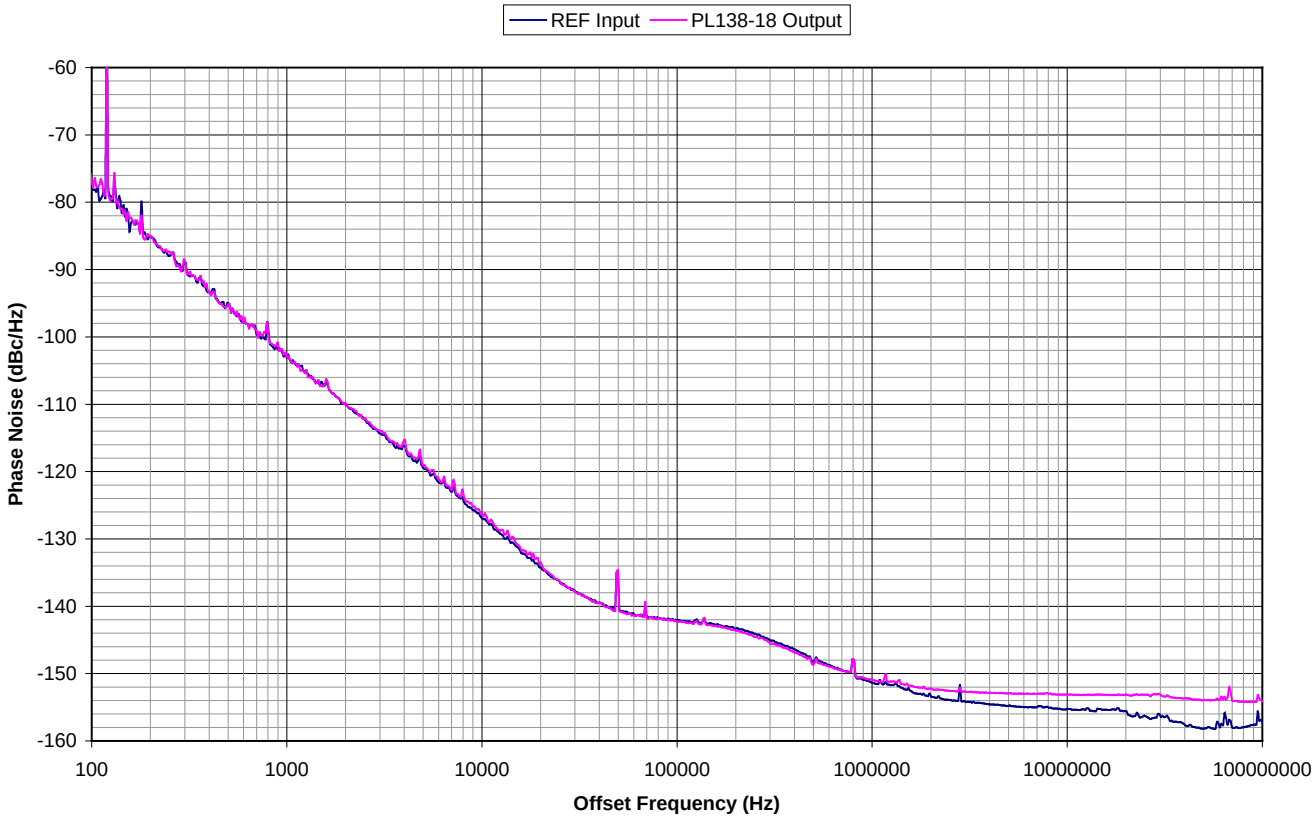
V_{CC} = -3.8V to -2.375V or, V_{CC} = 2.375V to 3.8V; V_{EE} = 0V, T_A = -40°C to 85°C

Parameter		Symbol	-40°C			25°C			80°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Frequency		f_{MAX}			700			700			700	MHz
Propagation Delay*		t_{PD}	600	680	750	650	725	790	690	790	890	ps
Output Skew ** †		tsk(o)		25	37		25	37		25	37	ps
Part-to-Part Skew *** †		tsk(pp)		85	225		85	225		85	225	ps
Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		t_{APJ}		0.10			0.10			0.10		ps
Output Rise/Fall Time	20% to 80%	t_R / t_F	200		700	200		700	200		700	ps

All parameters are measured at f ≤ 700MHz, unless otherwise noted.
* Measured from the differential input crossing point to the differential output crossing point.
** Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
*** Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
† This parameter is defined in accordance with JEDEC Standard 65.

NOISE CHARACTERISTICS (Commercial and Industrial Temperature Devices)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_{APJ}	Additive Phase Jitter	V_{CC} = 3.3V, Frequency = 622.08MHz Offset = 12KHz ~ 20MHz		21		fs

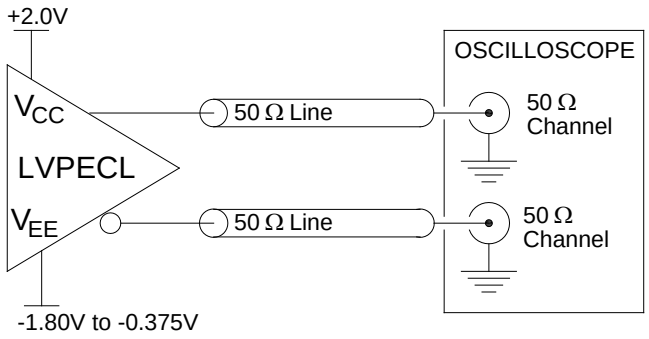


When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. To quantify the noise addition in the buffer we compare the Phase Jitter numbers from the input and the output. The difference is called "Additive Phase Jitter". The formula for the Additive Phase Jitter is as follows:

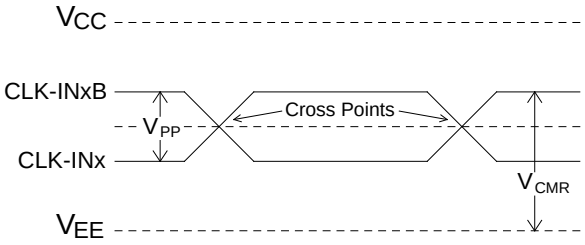
$$\text{Additive Phase Jitter} = \sqrt{(\text{Output Phase Jitter})^2 - (\text{Input Phase Jitter})^2}$$

PARAMETER MEASUREMENT INFORMATION

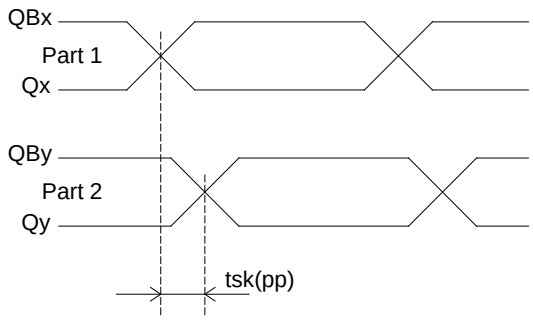
Output Waveform Test Circuit:



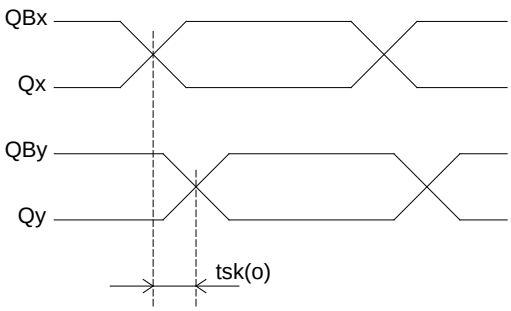
Differential Input Level:



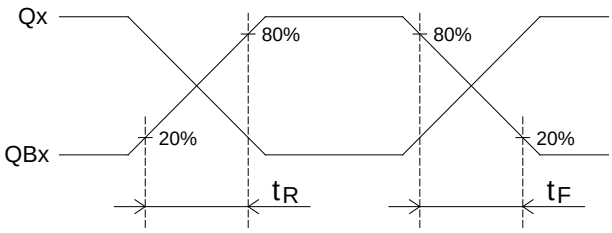
Part-to-Part Skew:



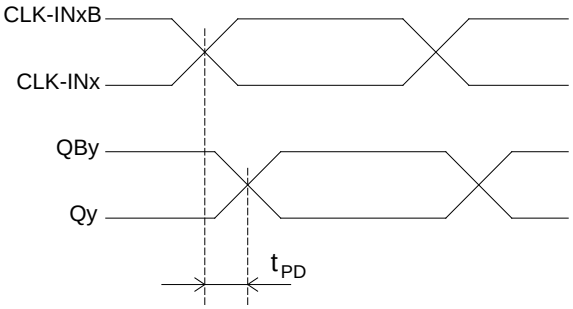
Output Skew:



Output Rise/Fall Time:



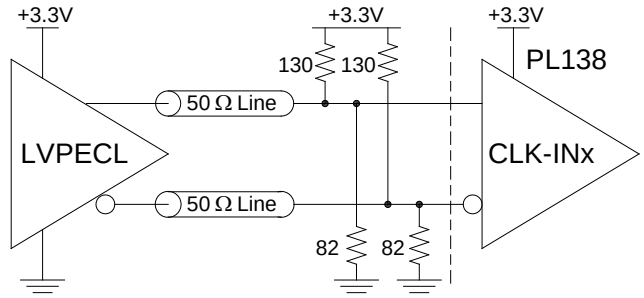
Propagation Delay:



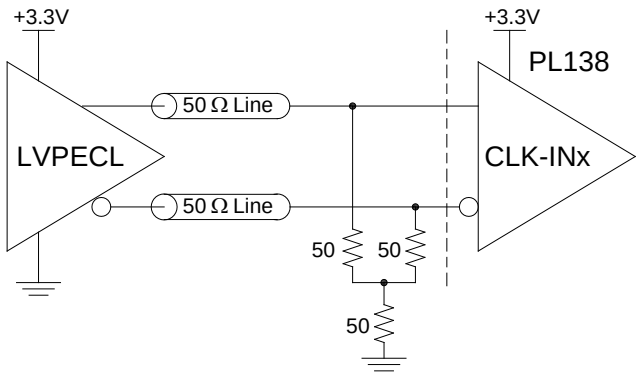
APPLICATION INFORMATION

The following circuits show different configurations for different input logic type signals. For good signal integrity at the PL138 input, the signals need to be properly terminated according to the logic type requirements. The signals need to be presented at the PL138 input according to V_{CMR}, V_{PP} and other input requirements.

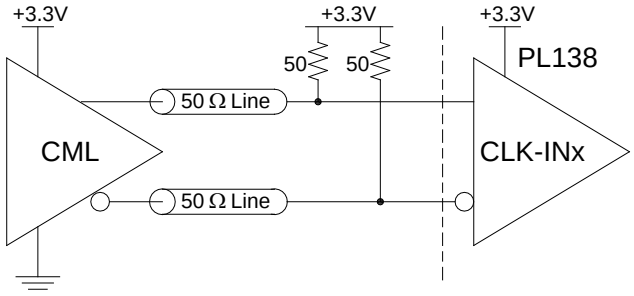
CLK-IN Input Driven by a 3.3V LVPECL Driver:



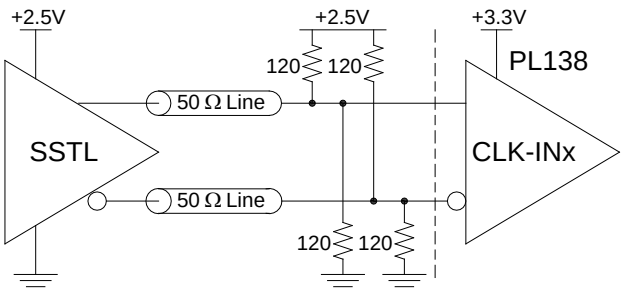
3.3V LVPECL Driver, Alternative Termination:



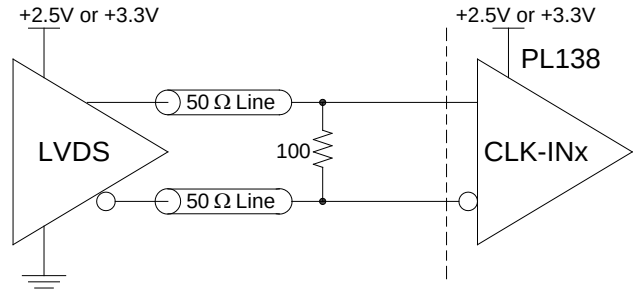
CLK-IN Input Driven by a CML Driver:



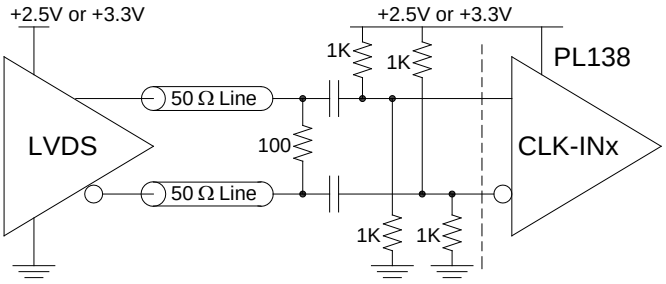
CLK-IN Input Driven by an SSTL Driver:



CLK-IN Input Driven by an LVDS Driver:



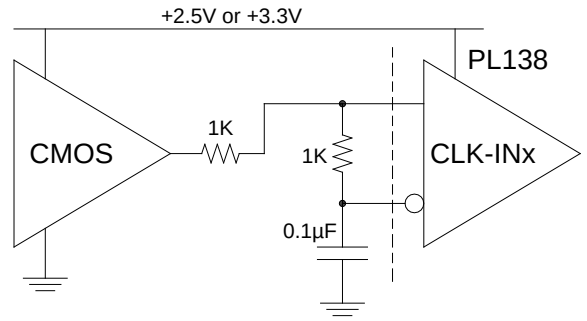
LVDS Driver, Alternative AC Coupling:



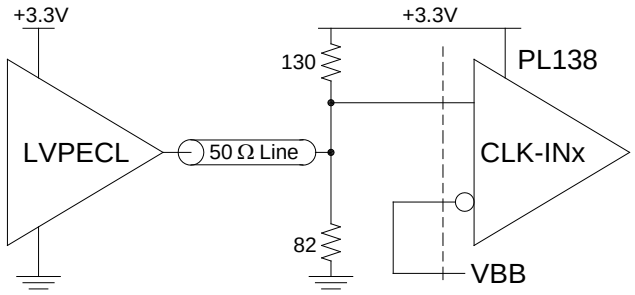
This circuit is for compatibility only. AC coupling is not really required for LVDS. The V_{CMR} range of the PL138 reaches low enough that LVDS signals can be connected directly to the PL138 input like in the circuit to the left.

2.5V-3.3V Low-Skew 1:10 Differential PECL Fanout Buffer

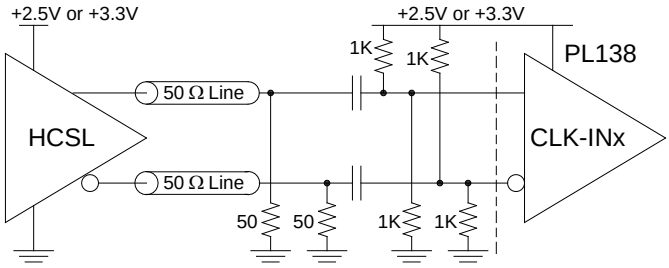
CLK-IN Input Driven by a CMOS Driver:



CLK-IN Input Driven by Single Ended LVPECL:



CLK-IN Input Driven by an HCSL Driver:

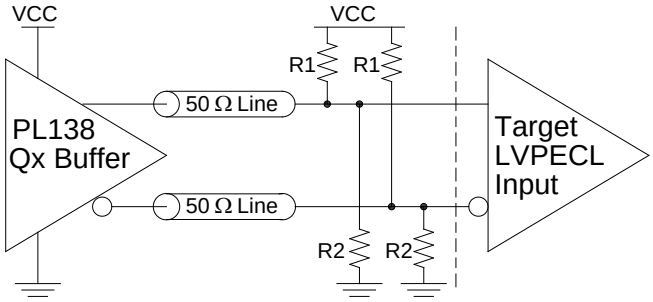


HCSL presents its signals very close to the ground rail, below the V_{CMR} range, so the HCSL signals can not be connected to the PL138 input directly. AC coupling is required for HCSL signals on the PL138 input.

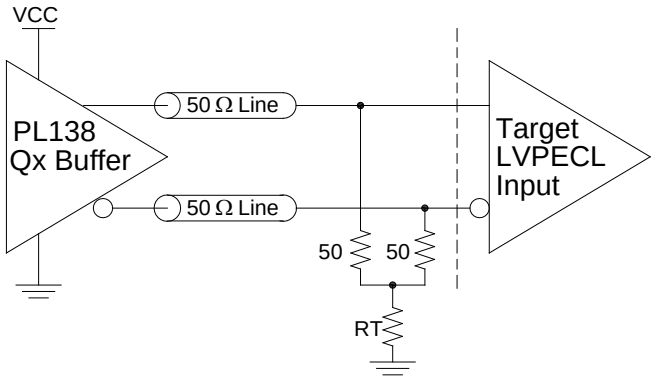
TERMINATION FOR LVPECL OUTPUTS

The required termination for LVPECL is 50Ω to a V_{CC}-2V DC voltage level. Below are two schematics to implement this termination.

LVPECL Termination Schematic #1:



LVPECL Termination Schematic #2:



VCC=3.3V, Ideal values: R1=127Ω , R2=82.5Ω
Commercial values (E24): R1=130Ω , R2=82Ω
VCC=2.5V, Ideal values: R1=250Ω , R2=62.5Ω
Commercial values (E24): R1=240Ω , R2=62Ω

Schematic #2 is an alternative simplified termination.
VCC=3.3V, Ideal value: RT=48.7Ω
Commercial value: RT=50Ω (E24: 51Ω)
VCC=2.5V, Ideal value: RT=18.7Ω
Commercial value: RT=18Ω

POWER CONSIDERATIONS

Driving LVPECL outputs requires an amount of power that can warm up the chip significantly. For driving 10 outputs we need to use the PCB as a heat sink. The LQFP package has a Thermal Relief pad on the bottom and it is advised to layout a PCB solder pad for the thermal relief pad with vias to the ground plane layer inside the PCB.

The general requirement for the chip is that the junction temperature should not exceed +110°C.

The power consumption can be divided into two parts:

1) Core power dissipation
2) Output buffers power dissipation

CORE POWER DISSIPATION

The chip core power is equal to VCC×IEE. With a worst case VCC and IEE the power dissipation in the core is 3.63V×88mA=319mW.

OUTPUT BUFFER POWER DISSIPATION

The output buffers are not exposed to the full VCC-VEE voltage. On the differential output, one line is at logic 1 with a small voltage across the buffer and a large output current. The other line is at logic 0 with a larger voltage across the buffer and a smaller output current. The power dissipation per output buffer is 32mW. Only buffers that are loaded will have power dissipation. With all 10 buffers loaded the worst case output buffer power dissipation will be 320mW.

Total Chip Power Dissipation, worst case, is 319mA + 320mW = 639mW.

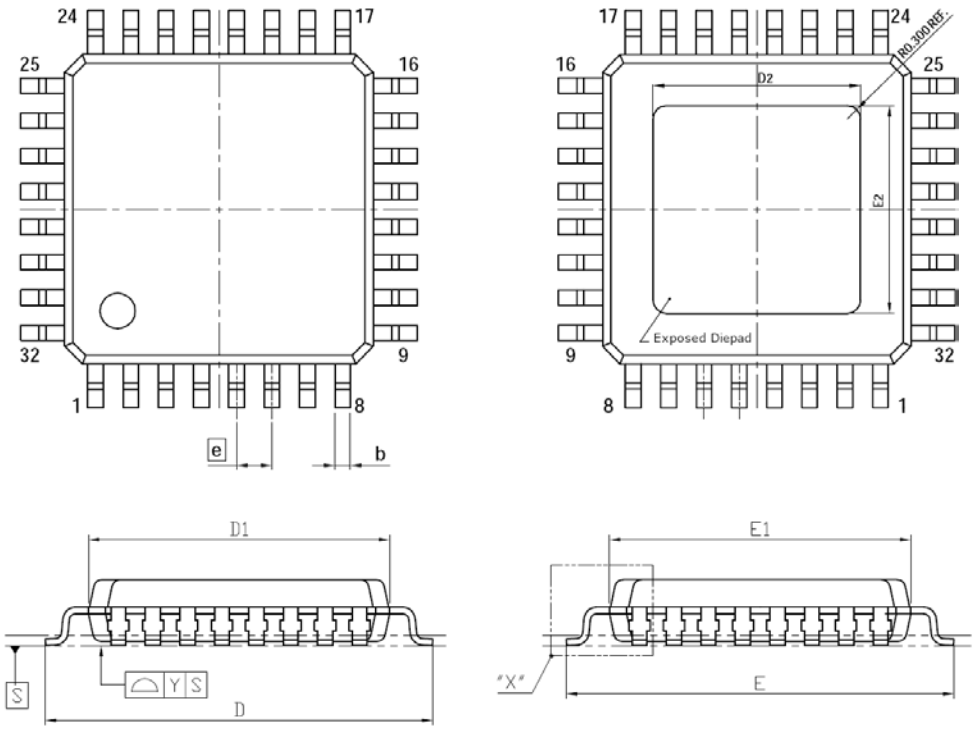
JUNCTION TEMPERATURE

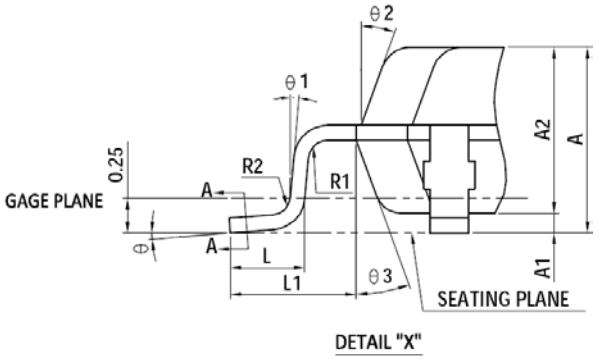
How much the chip is warmed up from the power dissipation depends upon the thermal resistance from the chip to the environment, also known as “junction to ambient”. The thermal resistance depends upon the type of package, how the package is assembled to the PCB and if there is additional air flow for improved cooling. For the LQFP package with use of the Thermal Relief pad, the thermal resistance is as follows:

LQFP-ep 32-pin Package	Air Flow Velocity in Linear Feet per Minute		
	0	200	500
JEDEC Standard Multi Layer PCB	θ_{JA} = 34.6°C/W	θ_{JA} = 29.1°C/W	θ_{JA} = 27.2°C/W

The temperature of the chip (junction) will be higher than the environment (ambient) with an amount equal to θ_{JA}× Power. For an ambient temperature of +85°C, all outputs loaded and no air flow, the junction temperature T_J = 85°C+34.6×0.639 = 107°C.

PACKAGE DRAWING (GREEN PACKAGE COMPLIANT)





SYMBOL	DIMENSION (mm)			DIMENSION (mil)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63.0
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	1.35	1.40	1.45	53.1	55.1	57.1
b	0.30	0.37	0.45	11.8	14.6	17.7
b1	0.30	0.35	0.40	11.8	13.8	15.7
c	0.09		0.20	3.5		7.9
c1	0.09		0.16	3.5		6.3
D	8.85	9.00	9.15	348.4	354.3	360.2
D1	6.90	7.00	7.10	271.7	275.6	279.5
D2	4.51	4.71	4.91	177.6	185.4	193.3
E	8.85	9.00	9.15	348.4	354.3	360.2
E1	6.90	7.00	7.10	271.7	275.6	279.5
E2	4.51	4.71	4.91	177.6	185.4	193.3
e	0.75	0.80	0.85	29.5	31.5	33.5
L	0.45	0.60	0.75	17.7	23.6	29.5
L1	0.85	1.00	1.15	33.5	39.4	45.3
R1	0.08			3.1		
R2	0.08		0.20	3.1		7.9
Y			0.10			3.9
θ	0^o	3.5^o	7^o	0^o	3.5^o	7^o
θ1	0^o			0^o		
θ2	11^o	12^o	13^o	11^o	12^o	13^o
θ3	11^o	12^o	13^o	11^o	12^o	13^o

ORDERING INFORMATION (GREEN PACKAGE)

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL138-18 X X - R

Part Number

R=Tape and Reel

Package Type
F=LQFP

Temperature Range
C= Commercial (0°C to +70°C)
I= Industrial (-40°C to +85°C)

Part/Order Number	Marking	Package Option
PL138-18FC	P138-18 FC LLLLL	32-Pin LQFP (Tray)

*Note: LLLLL designates lot number

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