PL133-27

Low-Power, 1.62V to 3.63V, 1MHz To 150MHz, 1:2 Fanout Buffer IC

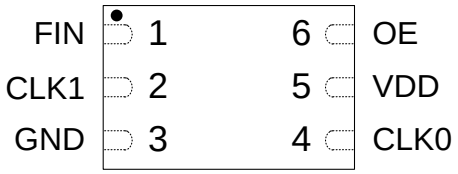
FEATURES

- 2 LVCMOS Outputs
- Input/Output Frequency: 1MHz to 150MHz
- Supports LVCMOS or Sine Wave Input Clock
- Extremely low additive Jitter
- 8 mA Output Drive Strength
- Low Current Consumption
- Single 1.8V, 2.5V, or 3.3V, ±10% Power Supply
- Operating Temperature Range
  - 0°C to 70°C (Commercial)
  - -40°C to 85°C (Industrial)
- Available in DFN-6L GREEN/RoHS Compliant Packages

DESCRIPTION

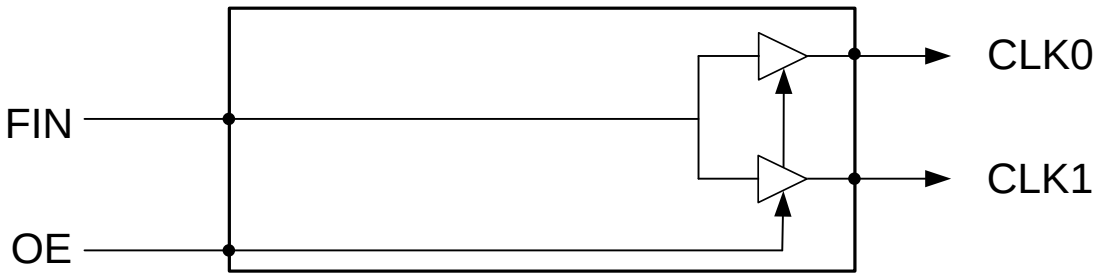
The PL133-27 is an advanced fanout buffer design for high performance, low-power, small form-factor applications. The PL133-27 accepts a reference clock input of 1MHz to 150MHz and produces two outputs of the same frequency. Reference clock inputs may be LVCMOS or sine-wave signals (the inputs are internally AC-coupled). PL133-27 is designed to fit in a small 2 x 1.3 x 0.6mm DFN package, and offers the best phase noise and jitter performance and lowest power consumption of any comparable IC.

PACKAGE PIN CONFIGURATION



DFN-6L
(2.0 x 1.3 x 0.6mm)

BLOCK DIAGRAM



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PACKAGE PIN ASSIGNMENT

Name	Package Pin # DFN-6L	Type	Description
FIN	1	I	Reference clock input
CLK1	2	O	Clock output
GND	3	P	GND connection
CLK0	4	O	Clock output
VDD	5	P	V_{DD} connection
OE	6	I	Output enable input

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces as “striplines” or “microstrips” with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply

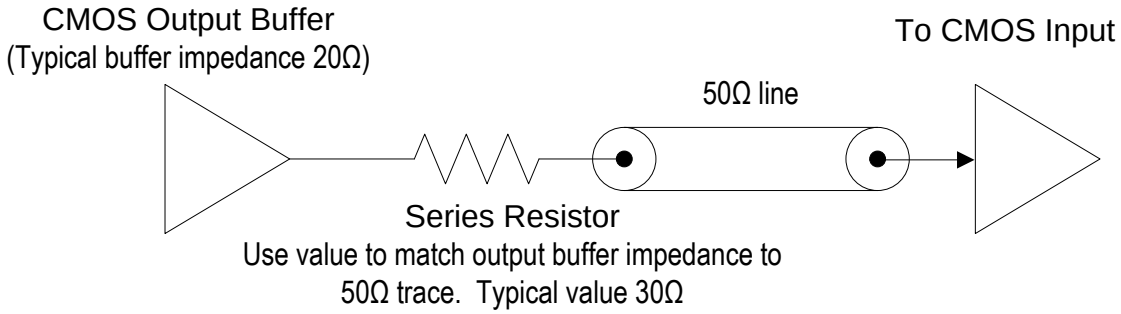
- Multiple V_{DD} pins should be decoupled separately for best performance.

- Addition of a ferrite bead in series with V_{DD} can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using crystals < 50MHz and 0.01μF for designs using crystals > 50MHz.

Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input (FIN) Frequency	@ V_{DD} = 2.5V and 3.3V	1MHz		150	MHz
	@ V_{DD} = 1.8V			65	
Input (FIN) Signal Amplitude	Internally AC coupled	0.8		V_{DD}	V_{PP}
Output Rise Time	15pF Load, 10/90%V_{DD}, 3.3V		2	3	ns
Output Fall Time	15pF Load, 90/10%V_{DD}, 3.3V		2	3	ns
Output to Output Skew				500	ps
Duty Cycle	Input Duty Cycle is 50%	45	50	55	%

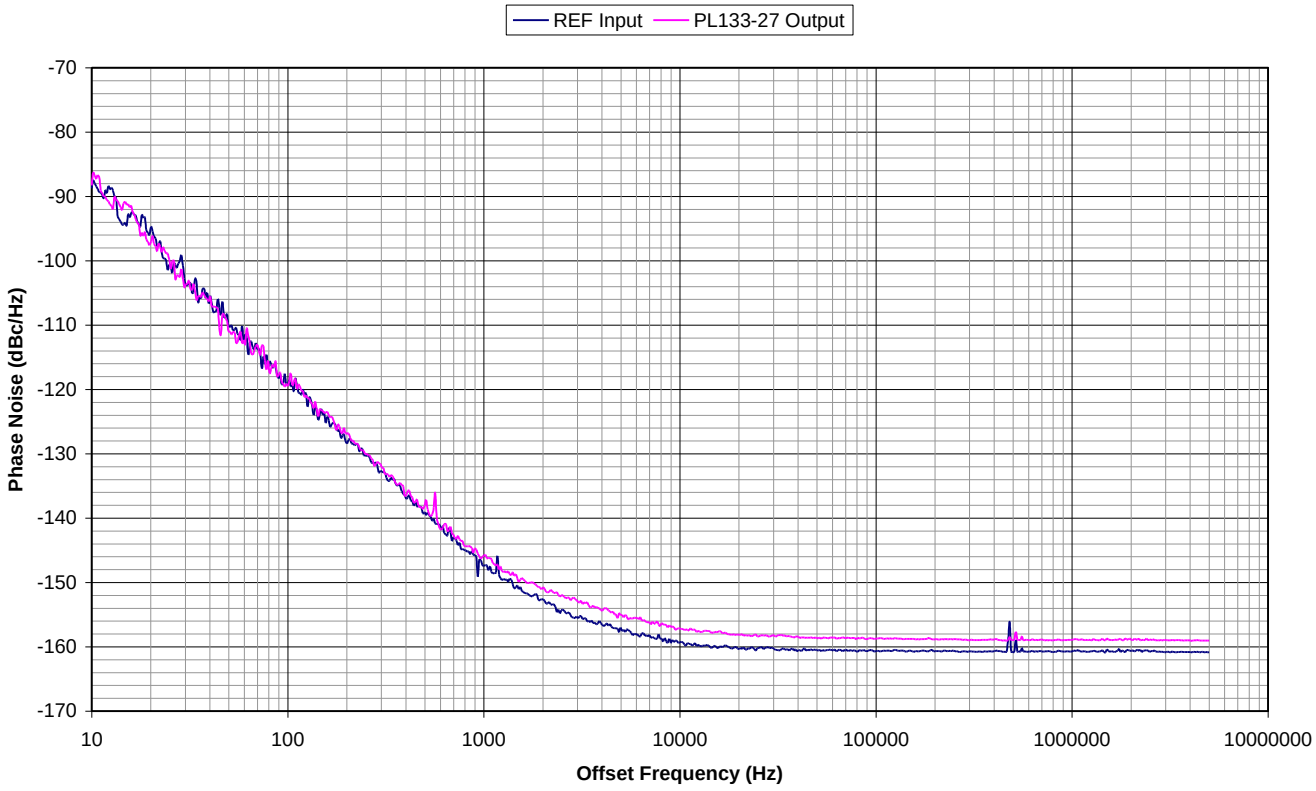
DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Dynamic	I_{DD}	V_{DD} = 3.3V, 25MHz, No Load		1.8		mA
		V_{DD} = 2.5V, 25MHz, No Load		1.3		mA
		V_{DD} = 1.8V, 25MHz, No Load		0.8		mA
Operating Voltage	V_{DD}		1.62		3.63	V
Output Low Voltage	V_{OL}	I_{OL} = +4mA, V_{DD} = 3.3V			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA, V_{DD} = 3.3V	2.4			V
Output Current	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V, V_{DD} = 3.3V	8			mA

NOISE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Additive Phase Jitter		V_{DD}=3.3V, Frequency=26MHz Offset=12KHz ~ 5MHz		130		fs
		V_{DD}=3.3V, Frequency=100MHz Offset=12KHz ~ 20MHz		150		fs

PL133-27 Additive Phase Jitter:
VDD=3.3V, CLK=26MHz, Integration Range 12KHz to 5MHz: 0.127ps typical.



When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. To quantify the noise addition in the buffer we compare the Phase Jitter numbers from the input and the output. The difference is called "Additive Phase Jitter". The formula for the Additive Phase Jitter is as follows:

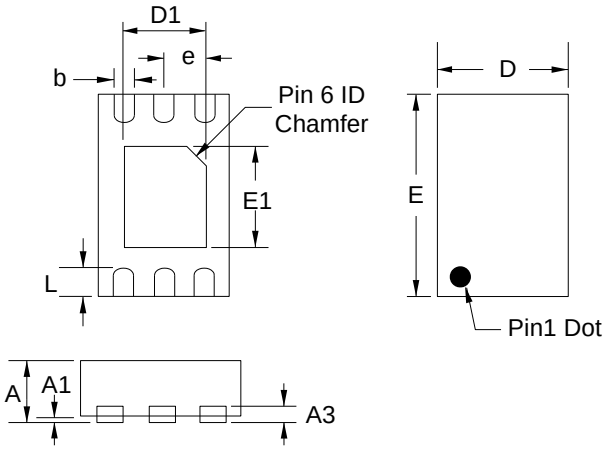
$$\text{Additive Phase Jitter} = \sqrt{(\text{Output Phase Jitter})^2 - (\text{Input Phase Jitter})^2}$$

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PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

DFN-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.45	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30



ORDERING INFORMATION (GREEN PACKAGE)

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL133-27 X X - R

Part Number

R=Tape and Reel

Package Type
G=DFN-6L

Temperature Range
C=Commercial (0°C to 70°C)
I=Industrial (-40°C to 85°C)

Part/Order Number	Marking	Package Option
PL133-27GC-R	H27 LLL	6-Pin DFN (Tape and Reel)
PL133-27GI-R		

***Note: LLL designates lot number**

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