Semiconductor Devices, Silicon
Hybrid Switching Regulators
High Reliability Types

	Test Level T_1	Test Level T_2
PIC 600/601/602	PIC 7501/7502/7503	PIC 7519/7520/7521
PIC 610/611/612	PIC 7504/7505/7506	PIC 7522/7523/7524
PIC 625/626/627	PIC 7507/7508/7509	PIC 7525/7526/7527
PIC 635/636/637	PIC 7510/7511/7512	PIC 7528/7529/7530
PIC 660/661/662	PIC 7555/7556/7557	PIC 7561/7562/7563
PIC 670/671/672	PIC 7558/7559/7560	PIC 7564/7565/7566

Contents

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Microsemi Corp.
Watertown
The diode experts

1.0 SCOPE

This specification defines the detail requirements for High Reliability Hybrid Switching Regulators. Very extensive 100% testing for parameter stability has been included in the Quality Assurance Provisions.

1.1a Absolute Maximum Ratings

	T_1 PIC7501 T_2 PIC7519 (PIC600)	T_1 PIC7502 T_2 PIC7520 (PIC601)	T_1 PIC7503 T_2 PIC7521 (PIC602)	T_1 PIC7504 T_2 PIC7522 (PIC610)	T_1 PIC7505 T_2 PIC7523 (PIC611)	T_1 PIC7506 T_2 PIC7524 (PIC612)
Input Voltage, V_{4-2}	60V	80V	100V	−60V	−80V	−100V
Output Voltage, V_{1-2}	60V	80V	100V	−60V	−80V	−100V
Drive-Input Reverse Voltage, V_{3-4}	5V	5V	5V	−5V	−5V	−5V
Output Current, I_1	5A	5A	5A	−5A	−5A	−5A
Drive Current, I_3	−0.2A	−0.2A	−0.2A	0.2A	0.2A	0.2A
Thermal Resistance						
Junction to Case, θ_{J-C}						
Power Switch	← 4.0°C/W →					
Commutating Diode	← 4.0°C/W →					
Case to Ambient, θ_{C-A}	← 60.0°C/W →					
Operating Temperature Range, T_C	← −55°C to +125°C →					
Maximum Junction Temperature, T_j	← +150°C →					
Storage Temperature Range	← −65°C to +150°C →					

1.1b Absolute Maximum Ratings

	T_1 PIC7507 T_2 PIC7525 (PIC625)	T_1 PIC7508 T_2 PIC7526 (PIC626)	T_1 PIC7509 T_2 PIC7527 (PIC627)	T_1 PIC7510 T_2 PIC7528 (PIC635)	T_1 PIC7511 T_2 PIC7529 (PIC636)	T_1 PIC7512 T_2 PIC7530 (PIC637)
Input Voltage, V_{4-2}	60V	80V	100V	−60V	−80V	100V
Output Voltage, V_{1-2}	60V	80V	100V	−60V	−80V	−100V
Drive-Input Reverse Voltage, V_{3-4}	5V	5V	5V	−5V	−5V	−5V
Output Current, I_1	15A	15A	15A	−15A	−15A	−15A
Drive Current, I_3	−0.4A	−0.4A	−0.4A	0.4A	0.4A	0.4A
Thermal Resistance						
Junction to Case, θ_{J-C}						
Power Switch	← 4.0°C/W →					
Commutating Diode	← 4.0°C/W →					
Case to Ambient, θ_{C-A}	← 60.0°C/W →					
Operating Temperature Range, T_C	← −55°C to +125°C →					
Maximum Junction Temperature, T_j	← +150°C →					
Storage Temperature Range	← −65°C to +150°C →					

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1.1c Absolute Maximum Ratings

	Positive Output			Negative Output		
	T_1 PIC7555 T_2 *PIC7561* (PIC660)	T_1 PIC7556 T_2 *PIC7562* (PIC661)	T_1 PIC7557 T_2 *PIC7563* (PIC662)	T_2 PIC7558 T_2 *PIC7564* (PIC670)	T_2 PIC7559 T_2 *PIC7565* (PIC671)	T_2 PIC7560 T_2 *PIC7566* (PIC672)
Input Voltage, V_{4-1}	60V	80V	100V	−60V	−80V	−100V
Output Voltage, V_{1-2}	60V	80V	100V	−60V	−80V	−100V
Drive-Input Reverse Voltage, V_{3-1}	5V	5V	5V	−5V	−5V	−5V
Peak Output Current, I_{1pk}	10A	10A	10A	−10A	−10A	−10A
Drive Current, I_3	−0.4A	−0.4A	−0.4A	0.4A	0.4A	0.4A
Thermal Resistance						
Junction to Case, θ_{J-C}						
Power Switch	← 4.0°C/W →					
Commutating Diode	← 4.0°C/W →					
Case to Ambient, θ_{C-A}	← 60.0°C/W →					
Operating Temperature Range, T_C	← −55°C to +125°C →					
Maximum Junction Temperature, T_j	← +150°C →					
Storage Temperature Range	← −65°C to +150°C →					

1.1d Electrical Specifications (at 25°C unless noted)

	Test	Symbol	PIC7501-3 PIC7519-21 Min.	Typ.	Max.	PIC7504-6 PIC7522-24 Min.	Typ.	Max.	Units	Conditions
1	*Current Delay Time*	t_{di}	—	20	40	—	20	40	ns	V_{in} = 25V (−25V)
2	Current Rise Time	t_{ri}	—	50	75	—	50	75	ns	V_{out} = 5V (−5V)
3	Voltage Rise Time	t_{rv}	—	30	50	—	30	50	ns	I_{out} = 2A (−2A)
4	Voltage Storage Time	t_{sv}	—	900	—	—	900	—	ns	I_3 = −20mA (20mA) (Note 5)
5	Voltage Fall Time	t_{fv}	—	50	75	—	50	75	ns	See Figure 1
6	Current Fall Time	t_{fi}	—	70	150	—	70	150	ns	See Notes 1, 2, 4
7	Efficiency (Notes 2 and 4)	η	—	85	—	—	85	—	%	
8	On-State Voltage (Note 3)	$V_{4-1\,(on)}$	—	1.0	1.5	—	−1.0	−1.5	V	I_4 = 2A (−2A), I_3 = −0.02A (0.02A)
9	On-State Voltage (Note 3)	$V_{4-1\,(on)}$	—	2.5	3.5	—	−2.5	−3.5	V	I_4 = 5A (−5A), I_3 = −0.02A (0.02A)
10	Diode Fwd. Voltage (Note 3)	$V_{2-1\,(on)}$	—	0.8	1.0	—	−0.8	−1.0	V	I_2 = 2A (−2A)
11	Diode Fwd. Voltage (Note 3)	$V_{2-1\,(on)}$	—	1.0	1.5	—	−1.0	−1.5	V	I_2 = 5A (−5A)
12	Off-State Current	I_{4-1}	—	0.1	10	—	−0.1	−10	μA	V_4 = Rated input voltage
13	Off-State Current	I_{4-1}	—	0.01	1.0	—	−0.1	−1.0	mA	V_4 = Rated input voltage, T_A = 100°C
14	Diode Reverse Current	I_{1-2}	—	1.0	10	—	−1.0	−10	μA	V_1 = Rated output voltage
15	*Diode Reverse Current*	I_{1-2}	—	0.5	1.0	—	−0.5	−1.0	*mA*	V_1 = *Rated output voltage, T_A = 100°C*

Notes:

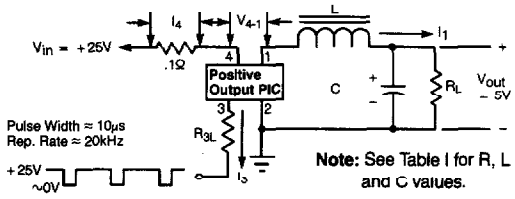
1. In switching an inductive load, the current will lead the voltage on turn-on and lag the voltage on turn-off (see Figure 1). Therefore, Voltage Delay Time (t_{DV}) ≅ t_{di} + t_{ri} and Current Storage Time (t_{si}) ≅ t_{sv} + t_{fv}.
2. The efficiency is a measure of internal power losses and is equal to Output Power divided by Input Power. The switching speed circuit of Figure 1, in which the efficiency is measured, is representative of typical operating conditions for the PIC600 series switching regulators.
3. Pulse test: Duration = ≤ 400μs. Duty Cycle ≤2%.
4. As can be seen from the switching waveforms shown in Figure 1, no reverse or forward recovery spike is generated by the commutating diode during switching! This reduces self-generated noise, since no current spike is fed through the switching regulator. It also improves efficiency and reliability, since the power switch only carries current during turn-on.
5. To insure safe operation, absolute value of I_3 should be a minimum of 20mA during $t_{(on)}$. Operation with I_3 below 20mA can permanently damage the device.
6. To insure safe operation, absolute value of I_3 should be a minimum of 30mA during $t_{(on)}$. Operation with I_3 below 30mA can permanently damage the device.

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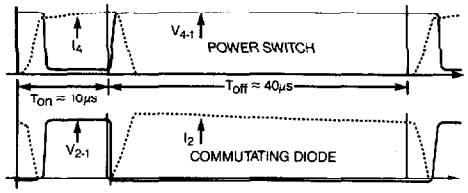
	Test	Symbol	PIC7507-9 PIC7525-27 Min.	Typ.	Max.	PIC7510-12 PIC7528-30 Min.	Typ.	Max.	Units	Conditions
1	Current Delay Time	t_{di}	—	35	60	—	35	60	ns	V_{in} = 25V (−25V)
2	Current Rise Time	t_{ri}	—	65	150	—	65	175	ns	V_{out} = 5V (−5V)
3	Voltage Rise Time	t_{rv}	—	40	60	—	40	60	ns	I_{out} = 7A (−7A)
4	Voltage Storage Time	t_{sv}	—	1200	—	—	1200	—	ns	I_3 = −30mA (30mA) (Note 6)
5	Voltage Fall Time	t_{fv}	—	70	175	—	100	300	ns	See Figure 1
6	Current Fall Time	t_{fi}	—	175	300	—	175	300	ns	See Notes 1, 2, 4
7	Efficiency (Notes 2 and 4)	η	—	85	—	—	85	—	%	
8	On-State Voltage (Note 3)	$V_{4-1\,(on)}$	—	1.0	1.5	—	−1.0	−1.5	V	I_4 = 7A (−7A), I_3 = −0.03A (0.03A)
9	On-State Voltage (Note 3)	$V_{4-1\,(on)}$	—	2.5	3.5	—	−2.5	−3.5	V	I_4 = 15A (−15A), I_3 = −0.03A (0.03A)
10	Diode Fwd. Voltage (Note 3)	$V_{2-1\,(on)}$	—	0.85	1.25	—	−0.85	−1.25	V	I_2 = 7A (−7A)
11	Diode Fwd. Voltage (Note 3)	$V_{2-1\,(on)}$	—	0.95	1.75	—	−0.95	−1.75	V	I_2 = 15A (−15A)
12	Off-State Current	I_{4-1}	—	0.1	10	—	−0.1	−10	μA	V_4 = Rated input voltage
13	Off-State Current	I_{4-1}	—	0.01	1.0	—	−0.1	−1.0	mA	V_4 = Rated input voltage, T_A = 100°C
14	Diode Reverse Current	I_{1-2}	—	1.0	10	—	−1.0	−10	μA	V_1 = Rated output voltage
15	Diode Reverse Current	I_{1-2}	—	0.5	1.0	—	−0.5	−1.0	mA	V_1 = Rated output voltage, T_A = 100°C

	Test	Symbol	PIC7555-7 PIC7561-3 Min.	Typ.	Max.	PIC7558-60 PIC7564-6 Min.	Typ.	Max.	Units	Conditions
1	Current Delay Time	t_{di}	—	35	60	—	35	60	ns	V_{in} = 25V (−25V)
2	Current Rise Time	t_{ri}	—	65	150	—	65	175	ns	V_{out} = 5V (−5V)
3	Voltage Rise Time	t_{rv}	—	40	60	—	40	60	ns	I_{out} = 5A (−5A)
4	Voltage Storage Time	t_{sv}	—	1200	—	—	1200	—	ns	I_3 = 30mA (−30mA) (Note 6)
5	Voltage Fall Time	t_{fv}	—	70	175	—	100	300	ns	See Figure 1
6	Current Fall Time	t_{fi}	—	175	300	—	175	300	ns	See Notes 1, 2, 4
7	Efficiency	η	—	85	—	—	85	—	%	See Notes 2 and 4
8	On-State Voltage	$V_{4-1\,(on)}$	—	1.0	1.5	—	−1.0	−1.5	V	I_4 = 5A (−5A), I_3 = −30mA (30mA), Notes 3, 5
9	On-State Voltage	$V_{4-1\,(on)}$	—	2.5	3.5	—	−2.5	−3.5	V	I_4 = 10A (−10A), I_3 = −30mA (30mA), Notes 3,5
10	Diode Fwd. Voltage	$V_{2-1\,(on)}$	—	0.85	1.25	—	−0.85	−1.25	V	I_2 = 5A (−5A)
11	Diode Fwd. Voltage	$V_{2-1\,(on)}$	—	0.95	1.75	—	−0.95	−1.75	V	I_2 = 10A (−10A)
12	Off-State Current	I_{4-1}	—	0.1	10	—	−0.1	−10	μA	V_4 = Rated input voltage
13	Off-State Current	I_{4-1}	—	.01	1	—	−.01	−1	mA	V_4 = Rated input voltage, T_A = 100°C
14	Diode Reverse Current	I_{1-2}	—	1.0	10	—	−1.0	−10	μA	V_1 = Rated output voltage
15	Diode Reverse Current	I_{1-2}	—	0.5	1.0	—	−0.5	−1.0	mA	V_1 = Rated output voltage, T_A = 100°C



Note: See Table I for R, L and C values.

Positive Output Switching Speed Circuit



Note: No Diode Reverse or Forward Recovery Spike (See note 4.).

Positive Output Switching Waveforms

Note: Negative test circuit and waveforms are identical but of opposite polarity (V_{in} = −25V, V_{out} = −5V).

Figure 1.

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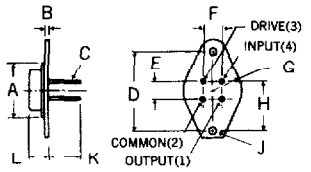
Table I.
Component Values for Switching Speed Circuit

I_3 required	R_{3L}
20mA	1.2 kohms ±5% tolerance
30mA	820 ohms ±5% tolerance

I_4 current	R_L	L	C
2A	2.5 ohms ±1% 10 watt	300 μH	50 μF 100V electrolytic
5A	1 ohm ±1% 50 watt	150 μH	150μF 100V electrolytic
7A	0.714 ohms ±1% 35 watt	150 μH	150μF 100V electrolytic

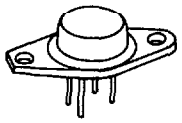
MECHANICAL SPECIFICATIONS

Notes: 1. Case is electrically isolated.
2. Loads may be soldered to within 1/16" of base provided temperature-time exposure is less than 260°C for 10 seconds.

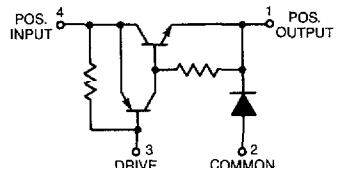


	ins.	mm
A	.600 MAX.	15.75 MAX.
B	.050-.075	1.27-1.91
C	.028-.034	0.71-0.86
D	.958-.962	24.33-24.43
E	.190-.210	4.83-5.33
F	.190-.210	4.83-5.33
G	.350 MAX. RAD.	8.89 MAX. RAD.
H	.570-.590	14.48-14.98
J	.142-.152 DIA.	3.61-3.86 DIA.
K	.360 MIN.	9.14 MIN.
L	.250-.340	6.35-8.64

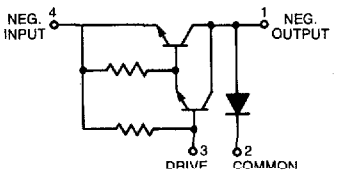
4-Pin TO-66



SCHEMATIC



PIC7501-3, PIC7519-21
PIC7507-9, PIC7525-27
PIC7555-57, PIC7561-65



PIC7504-6, PIC7522-24
PIC7510-12, PIC7528-30
PIC7558-60, PIC7564-66

Figure 2. Physical Dimensions and Biasing Diagrams

2.0 APPLICABLE DOCUMENTS

The following documents of the issue in effect on the date of invitations for bids, form a part of this specification to the extent specified herein.

MIL-S-19500 — General Specifications for Semiconductor Devices

MIL-S-19491 — Preparation for Delivery of Semiconductor Devices

3.0 REQUIREMENTS

3.1 Design and Construction

The Hybrid devices supplied under this specification shall have a design and construction such that they will meet all of the requirements specified herein. The dimensions and physical characteristics shall be as specified in Figure 2.

3.2 Performance Characteristics

The performance characteristics of the Hybrid device supplied under this specification shall be as specified in Group A inspection defined in Table III.

3.3 Quality Assurance

The Quality Assurance Provisions shall be as defined in paragraph 4.0.

3.4 Test Methods

Test methods shall be as specified herein.

3.5 Marking

The markings on the devices supplied shall be permanent and legible and shall include the Manufacturer's name or trademark, a Manufacturing Date Code in accordance with MIL-S-19500 and the specific device type number.

3.6 Preparation for Delivery

The Hybrid devices supplied under this specification shall be prepared for delivery in accordance with level C of MIL-S-19491 unless otherwise directed in the specific contract or *purchase order.*

3.7 Ordering Data

Procurement documents should specify the following:

a. Specific item type number
b. Number and date of this specification
c. Quality Assurance Test level required
d. Any special packaging if required

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General Provisions

4.1.1 Inspection Responsibility — The supplier is responsible for the performance of all inspection requirements and acceptability of results as specified herein for the Test Level identified in the contract or purchase order.

4.1.2 Controlled Manufacture — The devices supplied under this specification shall be manufactured under controlled conditions using formally defined quality assurance methods *and systems.*

4.1.3 Manufacturing Traceability — Each device supplied under this specification shall be traceable to a specific process group, to permit tracing of its full manufacturing history. Process group records shall indicate the exact date that each manufacturing operation was performed and identify materials and process procedures which were used. The manufacturer shall keep these records on file for at least five years.

4.1.4 Definitions

4.1.4.1 Inspection Lot — An "inspection lot" is a collection of devices from which a sample is withdrawn and inspected to determine compliance with the acceptibility criterion. It shall consist of one or more "inspection sublots" of the device types defined in this specification. The maximum inspection lot size shall be 5000 units.

4.1.4.2 Inspection Sublot — An "inspection sublot" shall consist of a collection of devices of a single type which have been manufactured under the same conditions and with the same materials.

4.1.4.3 Shipment Lot — A "shipment lot" shall consist of devices taken from an accepted inspection lot for the purpose *of shipment on a specific contract or order.*

4.1.4.4 Group A Inspection — Group A inspection shall consist of the examinations and tests specified in Table I, and shall be performed on a sublot basis.

4.1.4.5 Controlled Inventory — The controlled inventory shall consist of lots which have successfully passed the acceptance inspection and are being held in storage prior to actual shipment. A controlled inventory shall have adequate safeguards to insure that no defective or untested devices can be included in it. It shall be accessible only to those individuals who are formally identified as *authorized personnel.*

4.2 Acceptance Inspection

The acceptance inspection requirements shall be as defined by the applicable test level. The procedures of MIL-S-19500 shall apply to Group A inspection. Inspection lots which have been inspected and accepted shall be kept in a controlled inventory. Shipment lots shall be formed using devices taken from accepted inspection lots.

4.2.1 Test Level T2 Requirements — Test level T2 shall consist of the following requirements.

4.2.1.1 The supplier shall perform the Parameter Stability Testing defined in paragraph 4.3 on each device to be supplied. Prior to starting the Blocking Stability test defined in paragraph 4.3.6, each device shall be serialized for individual identity. Variables test data for the controlled electrical parameters shall be recorded before and after stressing. The same procedure shall apply for the Power Stress stability test defined in paragraph 4.3.8.

4.2.1.2 The supplier shall perform the Group A inspections in *accordance with the defined LTPD requirements on each in*spection sublot. Electrical parameter testing as specified shall be performed by variables with test data recorded.

4.2.1.3 With each shipment lot, the supplier shall provide a Certificate of Compliance to test level T2 of this specification.

4.2.2 Test Level T1 Requirements — Test level T1 shall consist of the following requirements.

4.2.2.1 The supplier shall perform the Parameter Stability *Testing defined in paragraph* 4.3 on each device to be supplied. Electrical parameter testing as specified shall be performed by attributes.

4.2.2.2 The supplier shall perform the Group A inspections in accordance with the defined LTPD requirements on each inspection sublot. Electrical parameter testing as specified shall be performed by attributes with test data recorded.

4.2.2.3. With each shipment lot, the supplier shall provide a Certification of Compliance to test level T1 of this specification.

4.3 Parameter Stability Tests

Each hybrid device to be supplied under this specification shall receive the following tests in addition to other standard testing performed by the manufacturer.

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4.3.1 Temperature Storage — Each Hybrid device shall be subjected, in a non-operating state, to a temperature of 150°C for a minimum period of 40 hours.

4.3.2 Temperature Cycling — Each Hybrid device shall be temperature cycled from −55°C to 150°C for a minimum of 10 cycles. Each cycle shall consist of at least 15 minutes at each temperature extreme with a maximum transition time of 5 minutes between each temperature extreme.

4.3.3 Hermetic Seal Test — Fine Leak — Each Hybrid device shall be tested for a case leakage rate of 1×10^{-8} cc/sec or smaller using a helium mass spectrometer or equivalent method. Devices with a case leakage rate greater than specified shall be removed from the lot.

4.3.4 Hermetic Seal Test — Gross Leak — Each Hybrid device shall be tested for gross leaks using fluorocarbon gross leak test or equivalent method. Devices with any indication of case leakage shall be removed from the lot.

4.3.5 Reverse Bias Clamp Inductive Test —

V_{4-2} = Rated Input Voltage
$f \approx 25kHz$, $E_{out} = 5V$
$T_C = 25°C$, see Figure 4
I_{out} — See Table II
$t \approx 1$ sec max

4.3.6 High Temperature Reverse Bias — Each Hybrid device will be high temperature reversed biased in the circuit shown in Figure 3. The conditions of this test are as follows:

$T_A = +125°C$
Time = 16 hours $^{+8}_{-0}$ hours
Circuit and voltages as shown in Figure 3.

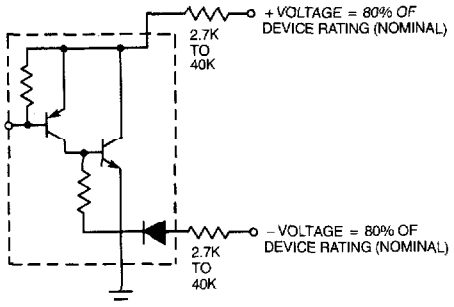


Figure 3. High Temperature Reverse Bias Circuit

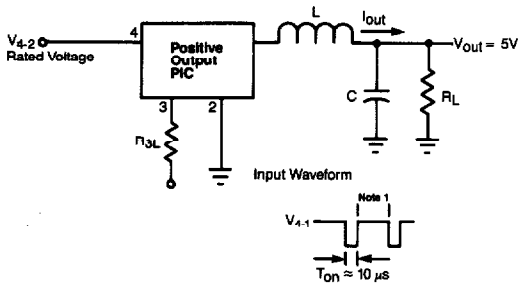
4.3.7 The following measurements will be made before and after the high temperature reverse bias test. The unit measurements shall be recorded or the devices will be celled in order to compare and guarantee the delta (△) requirements depending on the test level to which the lot is being prepared.

Part Type	Test 1.1.D	Maximum Readings Initial & Final	Delta Change	Symbol
PIC7501/7502/7503/7519/7520/7521	8	1.5V	±0.3V	$V_{4-1\ (on)}$
PIC7507/7508/7509/7525/7526/7527	8	1.5V	±0.3V	$V_{4-1\ (on)}$
PIC7555/7556/7557/7561/7562/7563	8	1.5V	±0.3V	$V_{4-1\ (on)}$
PIC7504/7505/7506/7522/7523/7524	8	−1.5V	±0.3V	$V_{4-1\ (on)}$
PIC7507/7508/7509/7528/7529/7530	8	−1.5V	±0.3V	$V_{4-1\ (on)}$
PIC7558/7559/7560/7564/7565/7655	8	−1.5V	±0.3V	$V_{4-1\ (on)}$
PIC7501/7502/7503/7519/7520/7521	10	1.0V	±0.25V	$V_{2-1\ (on)}$
PIC7507/7508/7509/7525/7526/7527	10	1.25V	±0.3V	$V_{2-1\ (on)}$
PIC7555/7556/7557/7561/7562/7563	10	1.25V	±0.3V	$V_{2-1\ (on)}$
PIC7504/7505/7506/7522/7523/7524	10	−1.0V	±0.25V	$V_{2-1\ (on)}$
PIC7507/7508/7509/7528/7529/7530	10	−1.25V	±0.3V	$V_{2-1\ (on)}$
PIC7558/7559/7560/7564/7565/7655	10	−1.25V	±0.3V	$V_{2-1\ (on)}$
PIC7501/7502/7503/7519/7520/7521	12	10μA	±1.0 or ±100%*	I_{4-1}
PIC7507/7508/7509/7525/7526/7527	12	10μA	±1.0 or ±100%*	I_{4-1}
PIC7555/7556/7557/7561/7562/7563	12	10μA	±1.0 or ±100%*	I_{4-1}
PIC7504/7505/7506/7522/7523/7524	12	−10μA	±1.0 or ±100%*	I_{4-1}
PIC7507/7508/7509/7528/7529/7530	12	−10μA	±1.0 or ±100%*	I_{4-1}
PIC7558/7559/7560/7564/7565/7655	12	−10μA	±1.0 or ±100%*	I_{4-1}
PIC7501/7502/7503/7519/7520/7521	14	10μA	±2.0 or ±100%*	I_{2-1}
PIC7507/7508/7509/7525/7526/7527	14	10μA	±2.0 or ±100%*	I_{2-1}
PIC7555/7556/7557/7561/7562/7563	14	10μA	±2.0 or ±100%*	I_{2-1}
PIC7504/7505/7506/7522/7523/7524	14	−10μA	±2.0 or ±100%*	I_{2-1}
PIC7507/7508/7509/7528/7529/7530	14	−10μA	±2.0 or ±100%*	I_{2-1}
PIC7558/7559/7560/7564/7565/7655	14	−10μA	±2.0 or ±100%*	I_{2-1}

* Whichever is greater.

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Note 1: Adjust T_{off} to obtain specified I_{out}.

Note 2: Negative output test circuits and waveforms are identical but of opposite polarity.

Note 3: See Table II for component values.

Figure 4. Reverse Bias Clamp Inductive Test Circuit

4.3.8 Power Stress — Each Hybrid device shall be burned-in using the circuit shown in Figure 5. The conditions are as follows:

T_A = +25°C

Time = 40 hours minimum

Circuit and conditions as shown in Figure 5.

4.3.9 The readings before and after burn-in shall be as specified in paragraph 4.3.7 above.

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Table II.
Component Values for Clamped Inductive Test
(Refer to Figure 4)

Device Type	R_{3L}	L/C	R_L	I_{OUT}
PIC 7501, 7504 PIC 7519, 7522	3K	300/100	2.5	2
PIC 7502, 7505 PIC 7520, 7523	4K	300/100	2.5	2
PIC 7503, 7506 PIC 7521, 7524	5K	300/100	2.5	2
PIC 7507, 7525 PIC 7510, 7528 PIC 7555, 7561 PIC 7558, 7564	2K	150/100	1	5
PIC 7508, 7526 PIC 7511, 7529 PIC 7556, 7562 PIC 7559, 7565	2.7K	150/100	1	5
PIC 7509, 7527 PIC 7512, 7530 PIC 7557, 7563 PIC 7560, 7566	3.3K	150/100	1	5

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Table III. Group A Inspection

Examination or Test	Symbol	Electrical Spec Test Number	Sample Size (LTPD)	Max. Acc. No.
Subgroup 1				
Visual and Mechanical	—	—	22 (10)	0
Subgroup 2 25°C Tests				
On-State Voltage	$V_{4\text{-}1\ on}$	8	45	0
On-State Voltage	$V_{4\text{-}1\ on}$	9	(5)	
Diode Forward Voltage	$V_{2\text{-}1\ on}$	10		
Diode Forward Voltage	$V_{2\text{-}1\ on}$	11		
Off-State Current	$I_{4\text{-}1}$	12		
Diode Reverse Current	$I_{1\text{-}2}$	14		
Subgroup 3 T_A = +100°C Tests				
Off-State Current	$I_{4\text{-}1}$	13	45	0
Off-State Current	$I_{1\text{-}2}$	15	(5)	
Subgroup 4 *25°C Tests*				
Current Delay Time	t_{dl}	1		
Current Rise Time	t_{rl}	2		
Voltage Rise Time	t_{rv}	3	45	0
Voltage Fall Time	t_{fv}	5	(5)	
Current Fall Time	t_{fi}	6		

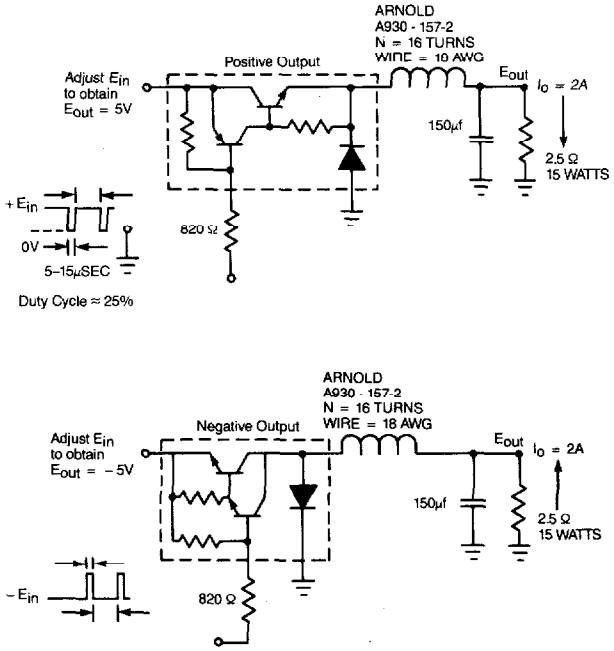


Figure 5. Burn-in Circuits