PIC24FJ128GA010

PIC24FJ128GA010 Family Rev. A4 Silicon Errata

The PIC24FJ128GA010 family Rev. A4 parts you have received conform functionally to the Device Data Sheet (DS39747**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC24FJ128GA010 Family will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC24FJ128GA010 devices with these Device/ Revision IDs:

Part Number	Device ID	Revision ID
PIC24FJ128GA010	040Dh	04h
PIC24FJ96GA010	040Ch	04h
PIC24FJ64GA010	040Bh	04h
PIC24FJ128GA008	040Ah	04h
PIC24FJ96GA008	0409h	04h
PIC24FJ64GA008	0408h	04h
PIC24FJ128GA006	0407h	04h
PIC24FJ96GA006	0406h	04h
PIC24FJ64GA006	0405h	04h

The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format “DEVID DEVREV”.

1. Module: Core

With Doze mode enabled, DOZEN (CLKDIV<11>) set, and the CPU Peripheral Clock Ratio Select bits (CLKDIV<14:12>) configured to any value except 0b000, writes to SFR locations can not be performed.

Work around

Disable Doze mode, or select 1:1 CPU peripheral clock ratio before modifying stated SFR locations, or avoid writing stated locations while Doze mode is enabled and CPU peripheral clock ratio other than 1:1 is selected. Configure the device prior to entering Doze mode and use the mode only to monitor applications activity.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: JTAG

The current JTAG programming implementation is not compatible with third party programmers using SVF (Serial Vector Format) description language. JTAG boundary scan is supported by third party JTAG solutions and is not affected.

Work around

Program devices with In-Circuit Serial Programming™. JTAG programming can be accomplished using custom JTAG software. The current implementation may not be supported in future PIC24F revisions. JTAG boundary scan is supported.

Date Codes that pertain to this issue:

All engineering and production devices.

3 Module: PMP

In Master mode (MODE<1:0> = 11 or 10), back-to-back operations may cause the $\overline{\text{PMRD}}$ signal to not be generated. This limitation occurs when the peripheral is configured for zero wait states (WAITM<3:0> = 0000).

Work around

The $\overline{\text{PMRD}}$ signal will be generated correctly if a minimum of one instruction cycle delay is inserted between the back-to-back operations. A NOP instruction, or any other instruction, is adequate. Selecting a delay other than zero will also permit the $\overline{\text{PMRD}}$ signal to be generated.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Interrupts

The device may not exit Doze mode if certain trap conditions occur. Address error, stack error and math error traps are affected. Oscillator failure and all interrupt sources are not affected and can cause the device to correctly exit Doze mode.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

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5. Module: Output Compare

The output compare module may output a single glitch for one TCY after the module is enabled (OCM<2:0> = 000). This issue occurs when the output state of the associated Data Latch register (LATx) is in the opposite state of the Output Compare mode when the peripheral is enabled. It can also occur when switching between two Output Compare modes with opposite output states.

Work around

If the output glitch must be avoided, verify that the associated data latch value of the OCx pin matches the initial state of the desired Output Compare mode. For example, if Output Compare 5 is configured for mode, OCM<2:0> = 001, ensure that the LATD<4> bit is clear prior to writing the OCM bits. The port latch output value will match the initial output state of the OC5 pin and avoid the glitch when the peripheral is enabled.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: UART

The timing for transmitting a Sync Break has changed for this revision of silicon. The Sync Break is transmitted as soon as the UTXBRK bit is set. A dummy write to UxTXREG is still required and must be performed before the Sync Break has finished transmitting. Otherwise, the UxTX may be held in the active state until the write has occurred.

Work around

Set the UTXBRK bit when a Sync Break is required and perform a dummy UxTXREG immediately following. This sequence will avoid holding the UxTX pin in the active state.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: UART

When the UART is in High-Speed mode, BRGH (UxMODE<3>) is set, some optimal UxBRG values can cause reception to fail.

Work around

Test UxBRG values in the application to find a UxBRG value that works consistently for more high-speed applications. User should verify that the UxBRG baud rate error does not exceed the application limits.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: UART

UART1 and UART2 hardware flow control options are not available for the 64-pin variants of the PIC24FJ128GA010 product family. As a result, the UxCTS and UxRTS pins not available and the UEN<1:0> control bits are read as '0' (unimplemented). UART2 hardware flow control is not available for the 80-pin PIC24FJ128GA010 variants. Therefore associated pins and bits are not available for these devices.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: UART

When the UART is in High-Speed mode (BRGH = 1), the auto-baud sequence can calculate the baud rate as if it were in Low-Speed mode.

Work around

The calculated baud rate can be modified by the following equation:

New BRG Value = (Auto-Baud BRG + 1) * 4 – 1

The user should verify baud rate error does not exceed application limits.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: UART

With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the Sync Break character from being loaded into the FIFO, load the UxBRG register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature (ABAUD = 1).

Date Codes that pertain to this issue:

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11. Module: A/D

Gain error may be as high as 5 LSbs for external references (V_{REF+} and V_{REF-}) and 6 LSbs for internal reference (AV_{DD} and AV_{SS}).

Work around

Determine gain error from a known reference voltage and compensate the A/D result in software.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: A/D

With the External Interrupt 0 (INT0) selected to start an A/D conversion (SSRC<2:0> = 001), the device may not wake-up from Sleep or Idle mode if more than one conversion is selected per interrupt (SMPI<3:0> <> 0000). Interrupts are generated correctly if the device is not in a Sleep or Idle mode.

Work around

Configure the A/D to generate an interrupt after every conversion (SMPI<3:0> = 0000). Use another wake-up source, such as the WDT or another interrupt source, to exit the Sleep or Idle mode. Alternatively, perform A/D conversions in Run mode.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: SPI

The Enhanced SPI modes, selected by setting the Enhanced Buffer Enable bit, SPIBEN (SPIxCON2<0>), are not available.

Work around

Use Standard SPI mode by clearing the SPI Enhanced Buffer Enable bit, SPIBEN.

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: SPI

Master mode receptions using the SPI1 and SPI2 modules may not function correctly for bit rates above 8 Mbps if the master has the SMP bit (SPIxCON1<9>) cleared (master samples data at the middle of the serial clock period).

In this case, the data transmitted by the slave is received, shifted right by one bit, by the master. For example, if the data transmitted by the slave was 0xAAAA, the data received by the master would be 0x5555 (0xAAAA shifted right by one bit).

Work around

Users may set up the SPI module so that the bit rate is 8 Mbps or lower.

Alternatively, the bit rate can be configured higher than 8 Mbps, but the SMP bit (SPIxCON1<9>) of the SPI master must be set (master samples data at the end of the serial clock period).

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: SPI

A frame synchronization pulse may not be output in SPI Master mode if the pulse is selected to coincide with the first bit clock (SPIFE = 1). SCKx and SDOx waveforms are not affected.

Work around

Select the frame sychronization pulses to proceed the first bit clock (SPIFE = 0). The frame pulses will output correctly as described in the product data sheet.

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: SPI

In SPI Slave mode (MSTEN = 0), with the slave select option enabled (SSEN = 1), the peripheral may accept transfers regardless of the $\overline{SSx}$ pin state. The received data in SSPxBUF will be accurate but not intended for the device.

Work around

If the Slave select option is required (e.g., device one of multiple SPI slave nodes on an SPI network), two potential work arounds exist:

1. Configure the port associated with $\overline{SSx}$ to an input and periodically read the PORT register. If the pin is read '0', disable the SPI peripheral (SPIEN = 0). Enable the peripheral (SPIEN = 1) if the pin is read as a logic '1'.
2. Read the pin associated with $\overline{SSx}$ after a transfer is complete, indicated by the SPIxF bit being set. If the port pin is read as a digital '1', read SSPxBUF and discard the contents.

Date Codes that pertain to this issue:

All engineering and production devices.

17. Module: Oscillator

The Two-Speed Start-up feature may not be available on exit from Sleep mode with the IESO (Internal/External Switchover mode) enabled. Upon wake-up, the device will wait for the clock source used prior to entering Sleep mode to become ready.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

18. Module: Core

The CLKDIV register Reset value is incorrect. The register will reset with unimplemented bits equal to '1' for all Resets.

Work around

Mask out unimplemented bits to maintain software compatibility with future device revisions.

Date Codes that pertain to this issue:

All engineering and production devices.

19. Module: Core

If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine. Instead, the device will simply wake-up from Idle mode and continue code execution if the Fail-Safe Clock Monitor (FSCM) is enabled.

Work around

Whenever the device wakes up from Idle (assuming the FSCM is enabled), the user software should check the status of the OSCFAIL bit (INTCON1<1>) to determine whether a clock failure occurred and then perform an appropriate clock switch operation.

Date Codes that pertain to this issue:

All engineering and production devices.

20. Module: Core

On a Brown-out Reset, both the BOR and POR bits may be set. This may cause the Brown-out Reset condition to be indistinguishable from the Power-on Reset.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

21. Module: Ports

RC15 may output a digital '0' after a Reset until the Configuration Word settings are processed. The duration of time for this effect is TRST which is nominally 20 µs.

After the Configuration Word is processed, RC15 is put into its reset state as a digital input.

Work around

Connect components not adversely affected by a digital 0 signal to RC15.

Date Codes that pertain to this issue:

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22. Module: I²C™

During I²C Slave mode transactions, the Data/Address bit, D/A, may not update during the data frame. This affects both 7 and 10-Bit Addressing modes.

I²C slave receptions are not affected by this issue.

Work around

Use the Read/Write bit, R/W, and the Transmit Buffer Full Status Bit, TBF, to determine whether address or data information is being received.

For more information, see Figure 24-30 and Figure 24-31 in ***"Section 24. Inter-Integrated Circuit™ (I²C™)"*** (DS39702A).

Date Codes that pertain to this issue:

All engineering and production devices.

23. Module: I²C

When the I²C module is operating in Slave mode, after the ACKSTAT bit is set when receiving a NACK from the master, it may be cleared by the reception of a Start or Stop bit.

Work around

Store the value of the ACKSTAT bit immediately after receiving a NACK from the master.

Date Codes that pertain to this issue:

All engineering and production devices.

24. Module: UART

When an auto-baud is detected, the receive interrupt may occur twice. The first interrupt occurs at the beginning of the Start bit and the second after reception of the Sync field character.

Work around

If a receive interrupt occurs, check the URXDA bit (UxSTA<0>) to ensure that valid data is available. On the first interrupt, no data will be present. The second interrupt will have the Sync field character (55h) in the receive FIFO.

Date Codes that pertain to this issue:

All engineering and production devices.

25. Module: UART

The auto-baud may miscalculate for certain baud rates and clock speed combinations, resulting in a BRG value that is 1 greater or less than the expected value. When UxBRG is less than 50, this can result in transmission and reception failures due to introducing error greater than 1%.

Work around

Test auto-baud calculations at various clock speed and baud rate combinations that would be used in applications. If an inaccurate UxBRG value is generated, manually correct the baud rate in user code.

Date Codes that pertain to this issue:

All engineering and production devices.

26. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

Date Codes that pertain to this issue:

All engineering and production devices.

27. Module: SPI

In SPI Master mode, the Disable SCK Pin bit, DISSCK, may not disable the SPI clock. As a result, the PIC® microcontroller must provide the SPI clock in Master mode.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

28. Module: Output Compare

In PWM mode, the output compare module may miss a compare event when the current duty cycle register (OCxRS) value is 0x0000 (0% duty cycle) and the OCxRS register is updated with a value of 0x0001. The compare event is only missed the first time a value of 0x0001 is written to OCxRS and the PWM output remains low for one PWM period. Subsequent PWM high and low times occur as expected.

Work around

If the current OCxRS register value is 0x0000, avoid writing a value of 0x0001 to OCxRS. Instead, write a value of 0x0002. In this case, however, the duty cycle will be slightly different from the desired value.

Date Codes that pertain to this issue:

All engineering and production devices.

29. Module: RTCC

The RTCC alarm repeat will generate an incorrect number of pin toggles. If the repeat count (x) is even, it will toggle the alarm pin 'x' times. If the repeat count is odd, one less than x toggles will be observed (x – 1).

Work around

None at this time.

Date Codes that pertain to this issue:

All engineering and production devices.

30. Module: RTCC

When performing writes to the ALCFGRPT register, some bits may become corrupted. The error occurs because of desynchronization between the CPU clock domain and the RTCC clock domain. The error causes data from the instruction *following* the ALCFGRPT instruction to overwrite the data in ALCFGRPT.

Work around

Always follow writes to the ALCFGRPT register with an additional write of the same data to a dummy location. These writes can be performed to RAM locations, W registers or unimplemented SFR space.

The optimal way to perform the work around:

1. Read ALCFGRPT into a RAM location.
2. Modify the ALCFGRPT data, as required, in RAM.
3. Move the RAM value into ALCFGRPT and a dummy location in back-to-back instructions.

Date Codes that pertain to this issue:

All engineering and production devices.

31. Module: CRC

If a CRC FIFO overflow occurs, the VWORD indicator will reset to '1' instead of '0'. Further writes to the FIFO will cause the VWORD indicator to reset to '0' after seven writes are performed.

Work around

Poll the CRCFUL bit (CRCCON<7>) to ensure that no writes are performed on the FIFO when it is full.

Date Codes that pertain to this issue:

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32. Module: I/O Pins

The I/O pin output, VOL, meets the specifications in Table 1 below:

TABLE 1: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage**					
DO10		All I/O Pins	—	—	.55	V	IOL = 8.5 mA, VDD = 3.6V
			—	—	.4	V	IOL = 7.8 mA, VDD = 3.6V
			—	—	.55	V	IOL = 6.0 mA, VDD = 2.0V
			—	—	.4	V	IOL = 5.0 mA, VDD = 2.0V

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

Work around

None.

REVISION HISTORY

Rev A Document (9/2007)

Initial release of this document. Includes silicon issues 1 (Core), 2 (JTAG), 3 (PMP), 4 (Interrupts), 5 (Output Compare), 6-10 (UART), 11-12 (A/D), 13-16 (SPI), 17 (Oscillator), 18-20 (Core), 21 (Ports), 22-23 (I^2C™), 24-26 (UART), 27 (SPI), 28 (Output Compare), 29-30 (RTCC), 31 (CRC) and 32 (I/O Pins).

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