PIC18FXX8

PIC18FXX8 Rev. C0 Silicon Errata Sheet

The PIC18FXX8 Rev. C0 parts you have received conform functionally to the Device Data Sheet (DS41159**D**), except for the anomalies described below.

The following silicon errata apply only to PIC18FXX8 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F248	00 1000 000	00101
PIC18F258	00 1000 010	00101
PIC18F448	00 1000 001	00101
PIC18F458	00 1000 011	00101

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Core (Program Memory Space)

Performing table read operations above the user program memory space (addresses over 1FFFFFh) may yield erroneous results at the extreme low end of the device's rated temperature range (-40°C).

This applies specifically to addresses above 1FFFFFh, including the user ID locations (200000h-200007h), the configuration bytes (300000h-30000Dh) and the device ID locations (3FFFFEh and 3FFFFFh). User program memory is unaffected.

Work around

Two possible work arounds are presented. Other solutions may exist.

1. Do not perform table read operations on areas above the user memory space at -40°C.
2. Insert NOP instructions (specifically, literal FFFFh) around any table read instructions. The suggested optimal number is 4 instructions before and 8 instructions after each table read. This may vary depending upon the particular application and should be optimized by the user.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Data EEPROM

When reading the data EEPROM, the contents of the EEDATA register may be corrupted if the $\overline{RD}$ bit (EECON1<0>) is set immediately following a write to the address byte (EEADR). The actual contents of the data EEPROM remain unaffected.

Work around

Do not set EEADR immediately before the execution of a read. Write to EEADR at least one instruction cycle before setting the $\overline{RD}$ bit. The instruction between the write to EEADR and the read can be any valid instruction, including a NOP.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: A/D (External Voltage Reference) and Comparator Voltage Reference

When the external voltage reference, V_{REF}-, is selected for use with either the A/D or comparator voltage reference, AV_{SS} is connected to V_{REF}- in the comparator module. If V_{REF}- is a voltage other than AV_{SS} (which must be tied externally to V_{SS}), excessive current will flow into the V_{REF}- pin.

Work around

If external V_{REF}- is used with a voltage other than 0V, enable the comparator voltage reference by setting the CVREN bit in the CVRCON register. This disconnects V_{REF}- and AV_{SS} within the comparator module.

4. Module: Core (Instruction Set)

The Decimal Adjust W register instruction, DAW, may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added using an instruction such as INCFSZ (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80        ; .80 (BCD)
ADDLW   0x80        ; .80 (BCD)

BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB
DAW
BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB

This is repeated for each DAW instruction.
```

5. Module: CAN

CAN Disable mode change request is not confirmed. A CAN Disable mode request by writing '001' to the REQOP bits (CANCON<7:5>) immediately changes the OPMODE bits (CANSTAT<7:5>), implying that Disable mode is accepted. This occurs even though the CAN module itself may not have switched its state.

Work around

Switch to Configuration mode instead. Wake-up from CAN bus activity will continue to work even in Configuration mode.

6. Module: MSSP (All I²C™ and SPI Modes)

The Buffer Full (BF) flag bit of the SSPSTAT register (SSPSTAT<0>) may be inadvertently cleared even when the SSPBUF register has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = 1111); and
- Any instruction that contains C9h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh.

In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select all GPR Banks.
2. If accessing a part of Bank 15 is required, and the use of Access Banking is not possible, consider using Indirect Addressing mode.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain C9h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: CAN

An incoming CAN message may not be saved properly to a CAN receive buffer if one of the following conditions is met:

1. Bank 15 is selected and the firmware attempts to read the RXB0 or RXB1 registers while a CAN message reception is in progress.
2. Bank 15 is selected and an instruction is executed whose lower 8 bits match with one of the CAN receive buffer addresses (RXBn addresses in the range of 0xF61 to 0xF6E and 0xF51 to 0xF5D) while a CAN message reception is in progress. Some of the instruction examples are:
   - 0xFF68 (`NOP`)
   - 0xEE68 (first half of `GOTO 0xD0`)
   - 0x0E6A (`MOVLW 0x6A`)
   - 0x6055 (`MOVF 0xF66, W`)

   Other instruction combinations exist.
3. The firmware attempts to access the GPR (General Purpose Register) addresses between addresses 0x51 and 0x5D in the Access Bank while a CAN message reception is in progress. Some of the instruction examples are:
   - `MOVWF 0x57, A`
   - `ADDWF 0x57, A`
   - `MOVF  0x57, W, A`

Work around

1. Once in normal CAN mode, never select Bank 15. Always use Access Bank RAM to access the CAN buffers. The RXB0 buffer is already available in the Access Bank. All other transmit and receive buffers are available in Access Bank RAM, via the RXB0 registers, using the WIN bits available in the CANCON register.
2. Always make sure that the RXFUL bit is set before attempting to access any of the Receive Buffer registers.
3. Do not access/use any of the registers in the Access Bank address range of 0x051 to 0x05D. If using assembly language, do not allocate any of your application variables in this address range. If using a C compiler, make sure that the compiler does not allocate any variable in the specified address range.

8. Module: Reset

It has been observed that in certain Reset conditions, including power-up, the first `GOTO` instruction at address 0x0000 may not be executed. This occurrence is rare and affects very few applications.

To determine if your system is affected, test a statistically significant number of applications across the operating temperature, voltage and frequency ranges of the application. Affected systems will repeatedly fail normal testing. Systems not affected will continue to not be affected over time.

Work around

Insert a `NOP` instruction at address 0x0000.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: Program Memory

A very small number of applications are experiencing a low failure rate when using self-write through code types of applications. The most common of these are bootloader operations. This failure mechanism is characterized by a few bytes in program memory not being written as expected.

If this failure is going to occur, it will occur during a self-write operation. If a failure is not immediately observed, then there will be no data retention issues. The failure does not occur when using an external programmer through In-Circuit Serial Programming™ (ICSP™).

This failure mechanism is dependent on the sequence of instructions executed after self-writes. Good power supply decoupling minimizes this issue. It is recommended that you use a 0.1 μF decoupling capacitor with each power pin pair. The decoupling capacitor should be placed very close to the power pins.

It is recommended that you perform statistically significant testing within your application's operating range (i.e., temperature and voltage) with devices from multiple lots.

Work around

1. This work around only applies to PIC18F258 and PIC18F458 devices. The program memory is divided into discrete panels and the failure has only been observed when a table write is executed from the same panel it is programming. The table write (self-write) within the same memory panel (0x0000 to 0x3FFF and 0x4000 to 0x7FFF) initiates a condition that can cause a failure. The firmware work around is to duplicate the partial bootloader (two instantiations of write functions) in two panels and ensure that the bootloader code always programs a different panel from where it resides. To accomplish this, do the following:
   - Receive data from communication channel (normal operation for the bootloader).
   - Identify address to be written.
   - If writing to an address within the same memory panel that you are executing from (0x0000 to 0x3FFF and 0x4000 to 0x7FFF), then jump to the opposite memory panel. If the bootloader resides between location 0x0000 to 0x3FFF, and if writing to an address between 0x0000 to 0x3FFF, then jump to another instantiation of the code located between 0x4000 to 0x7FFF and vice versa.
   - Always load holding latches (loading of TABLAT and then use `TBLWT*`) from the opposite panel. This will require duplicate code in each panel to load data.
   - Always initiate write from the opposite panel. This will require duplicate code in each panel for the unlocking sequence and setting up the write bit.
   - At the end of the successful write, code can return to the primary panel to get the next data.
2. Use a similar device from the PIC18F4580 family.

10. Module: CAN

Under specific conditions, the first five bits of a transmitted identifier may not match the value in the Transmit Buffer ID register, TXBxSIDH. If the CAN peripheral detects a Start-of-Frame (SOF) in the third bit of interframe space, and if a message to be transmitted is pending, the first five bits of the transmitted identifier may be corrupted.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41159**D**), the following clarifications and corrections should be noted.

None.

REVISION HISTORY

Rev A Document (07/2003)

First revision of this document, silicon issues 1 (Core – Program Memory Space), 2 (Data EEPROM), 3 (A/D (External Voltage Reference) and Comparator Voltage Reference) and 4 (Core – Instruction Set) and data sheet clarification issues 1 (A/D – VREF+ and VREF- References) and 2 (DC Characteristics Table).

Rev B Document (03/2004)

Removed “Extended Temperature” from the title of the Errata. Added silicon issues 5 (CAN), 6 (MSSP – All I^2C and SPI Modes) and 7 (MSSP – SPI, Slave Mode). Added data sheet clarification issues 3 (External Clock Timing Requirements – Table 27-6), 4 (A/D Converter Characteristics – Table 27-23) and 5 (Comparator Voltage Reference Module).

Rev C Document (06/2004)

Data Sheet Clarification issue 2 (DC Characteristics Table) was updated to include parameter D005 (Brown-out Reset Voltage) and added Data Sheet Clarification issue 6 (Low-Voltage Detect (LVD) Characteristics).

Rev D Document (07/2004)

Clarifications/Corrections to the Data Sheet; Added Data Sheet Clarification issue 7 (PSP Waveforms).

Module 2: DC Characteristics Table, Section 27.1 Param. No. D005, corrected trip-point values for PIC18LFXX8.

Rev E Document (09/2004)

Added silicon issue 8 (CAN).

Rev F Document (11/2004)

Updated silicon issue 8 (CAN) and removed all Data Sheet Clarification issues.

Rev G Document (05/2005)

Added silicon issue 9 (Reset).

Rev H Document (05/2006)

Removed previous silicon issue 7 (MSSP – SPI, Slave Mode) which is covered in global MSSP Errata. Added silicon issue 9 (Program Memory).

Rev J Document (08/2006)

Added silicon issue 10 (CAN).

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