



MICROCHIP

PIC18F2585/2680/4585/4680

PIC18F2585/2680/4585/4680 Rev. B1 Silicon Errata

The PIC18F2585/2680/4585/4680 Rev. B1 parts you have received conform functionally to the Device Data Sheet (DS39625C), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2585/2680/4585/4680 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2585/2680/4585/4680 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2585	0000 1110 111	0 0111
PIC18F2680	0000 1110 110	0 0111
PIC18F4585	0000 1110 101	0 0111
PIC18F4680	0000 1110 100	0 0111

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F2585/2680/4585/4680 silicon.

1. Module: Master Synchronous Serial Port (MSSP)

The MSSP module when configured for I²C™ slave reception, in extremely rare cases, the data received may not be correct. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature.

This is done by setting the SEN bit (SSPCON2<0>).

- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Date Codes that pertain to this issue:

All engineering and production devices.

PIC18F2585/2680/4585/4680

REVISION HISTORY

Rev A Document (10/2008)

Original errata document for this device. Includes silicon issue 1 (Master Synchronous Serial Port (MSSP)).

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