

**MICROCHIP****PIC18F6393/6493/8393/8493**

PIC18F6393/6493/8393/8493 Family Silicon Errata and Data Sheet Clarification

The PIC18F6393/6493/8393/8493 family devices that you have received conform functionally to the current Device Data Sheet (DS39896B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F6393/6493/8393/8493 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (C1).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICKit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICKit™ 3.
2. From the main menu in MPLAB IDE, select Configure>Select Device, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (Debugger>Select Tool).
4. Perform a "Connect" operation to the device (Debugger>Connect). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F6393/6493/8393/8493 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾		
		C0	C1	
PIC18F6393	1A0h	5h	6h	
PIC18F6493	070h			
PIC18F8393	1A2h			
PIC18F8493	072h			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the "*Programming Specifications for PIC18F6393/6493/8393/8493 Family Flash MCUs*" (DS39624) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾		
				C0	C1	
MSSP	SPI	1.	In SPI Slave mode, the MSSP will generate a write collision if SSPBUF is updated and that register's contents have not been transferred to the shift register.	X	X	
MSSP	SPI	2.	A flag, collision detect and indicator bit are not reset when the SPI module is disabled.	X	X	
MSSP	I ² C™	3.	In 10-Bit Slave mode, the I ² C mode does not work correctly.	X	X	
MSSP	I ² C	4.	The MSSP may not receive the correct data if there is a delay in reading SSPBUF after an SSPIF interrupt.	X	X	
MSSP	I ² C	5.	When the module is configured for the I ² C Master mode and the device is operating below 3V, the I ² C transmission will not work correctly.	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**C1**).

1. Module: Master Synchronous Serial Port (MSSP)

Configured in SPI slave mode, the MSSP will generate a write collision if SSPBUF is updated and the previous SSPBUF contents have not been transferred to the shift register.

Reinitializing the MSSP – by clearing and setting the SSPEN bit (SSPCON1<5>) prior to rewriting SSPBUF – will *not* prevent the error condition.

Work around

Prior to updating the SSPBUF register with a new value, verify that the previous contents have been transferred by reading the BF bit (SSPSTAT<0>). If the previous byte has *not* been transferred:

- Update SSPBUF
- If necessary, clear the WCOL bit (SSPCON1<7>)

Affected Silicon Revisions

C0	C1						
X	X						

2. Module: Master Synchronous Serial Port (MSSP) – Serial Peripheral Interface (SPI)

In SPI mode, the Buffer Full flag (BF bit in the SSPSTAT register), the Write Collision Detect bit (WCOL in SSPCON1) and the Receive Overflow Indicator bit (SSPOV in SSPCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPCON1 register).

For example, if SSPBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

Work around

If the buffer is full, before disabling the MSSP module, ensure that:

- SSPBUF is read (thus clearing the BF flag)
- WCOL is clear

If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

Affected Silicon Revisions

C0	C1						
X	X						

3. Module: Master Synchronous Serial Port (MSSP) – I²C™

In 10-Bit Slave mode, the I²C™ mode does not work correctly.

Work around

None.

Affected Silicon Revisions

C0	C1						
X	X						

4. Module: MSSP – I²C

When configured for I²C slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either one of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature.
This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

C0	C1						
X	X						

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5. Module: MSSP – I²C

The I²C transmission will not work correctly in the MSSP module when it is configured for the I²C Master mode and the device is operating below 3V. The failure can be that the I²C data and clock are not coming out, or a false Acknowledgement will be received, ACKSTAT = 0 (SSPCON2<7>, even if no slave was addressed on the bus.

Work around

None.

Affected Silicon Revisions

C0	C1						
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39896B):

Note: Corrections are shown in bold . Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (9/2007)

First release of this document. Includes silicon issues 1-3 (MSSP).

Rev B Document (11/2009)

Revised silicon revision C0 errata to the new format for all silicon revisions and data sheet clarifications. Added silicon issues 4-5 (MSSP – I²C).

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