PIC18F8720/8620/6720/6620 Rev. A4 Silicon/Data Sheet Errata

The PIC18F8720/8620/6720/6620 parts you have received conform functionally to the Device Data Sheet (DS39609**B**), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC18F8720/8620/6720/6620 silicon.

The following silicon errata apply only to PIC18F8720/8620/6720/6620 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F6620	00 0110 011	00100
PIC18F6720	00 0110 001	00100
PIC18F8620	00 0110 010	00100
PIC18F8720	00 0110 000	00100

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Core (Program Memory Space)

Performing table read operations above the user program memory space (addresses over 1FFFFFh) may yield erroneous results at the extreme low end of the device's rated temperature range (-40°C).

This applies specifically to addresses above 1FFFFFh, including the user ID locations (200000h-200007h), the configuration bytes (300000h-30000Dh) and the device ID locations (3FFFFEh and 3FFFFFh). User program memory is unaffected.

Work around

Two possible work arounds are presented. Other solutions may exist.

1. Do not perform table read operations on areas above the user memory space at -40°C.
2. Insert `NOP` instructions (specifically, literal FFFFh) around any table read instructions. The suggested optimal number is 4 instructions before and 8 instructions after each table read. This may vary depending upon the particular application and should be optimized by the user.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: External Memory Interface (PIC18F8620 only)

In Extended Microcontroller mode, or Microprocessor mode, the external memory interface is inactive from 20000h to 2FFFFh. ALE and $\overline{WRL}$ signals are inactive between 20000h and 2FFFFh.

Work around

Shift RAM space to 30000h and above, or as an alternate solution, the PIC18F8720 device can be used.

This issue will be resolved in a future version of silicon.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: I/O Ports (Parallel Slave Port)

While operating in Parallel Slave Port mode, the OBF bit (PSPCON<6>) is supposed to be set when a byte is written to either PORTD or LATD. It has been noted that OBF may not be correctly set when a byte is written to LATD. If the byte is written to PORTD, then the OBF bit is set correctly.

Work around

To ensure the OBF bit is set correctly, write to PORTD rather than LATD.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: A/D (External Voltage Reference) and Comparator Voltage Reference

When the external voltage reference, V_{REF}-, is selected for use with either the A/D or comparator voltage reference, AV_{SS} is connected to V_{REF}- in the comparator module. If V_{REF}- is a voltage other than AV_{SS} (which must be tied externally to V_{SS}), excessive current will flow into the V_{REF}- pin.

Work around

If external V_{REF}- is used with a voltage other than 0V, enable the comparator voltage reference by setting the CVREN bit in the CVRCON register. This disconnects V_{REF}- and AV_{SS} within the comparator module.

Date Codes that pertain to this issue:

All engineering and production devices.

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5. Module: DAW Instruction

The DAW instruction may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added, using an instruction such as INCFSZ (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80        ; .80 (BCD)
ADDLW   0x80        ; .80 (BCD)

BTFSC   STATUS,C    ; test C
INCFSZ  byte2       ; inc next higher LSB
DAW
BTFSC   STATUS,C    ; test C
INCFSZ  byte2       ; inc next higher LSB

This is repeated for each DAW instruction
```

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: External Memory Interface (PIC18F8720 and PIC18F8620 only)

When performing writes on the external memory interface, a short glitch is present on the $\overline{LB}$ and $\overline{UB}$ lines. The length of the glitch is proportional to FOSC and also may vary with process, voltage and temperature. The glitch occurs well before the $\overline{WRH}$ line is asserted and no adverse affect on the operation of the external memory interface has been observed.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: MSSP (All I²C™ and SPI™ Modes)

The Buffer Full (BF) flag bit of the SSPSTAT register (SSPSTAT<0>) may be inadvertently cleared even when the SSPBUF register has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = 1111); and
- Any instruction that contains C9h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh.

In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select all GPR Banks.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain C9h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

Date Codes that pertain to this issue:

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8. Module: Reset

It has been observed that in certain Reset conditions, including power-up, the first GOTO instruction at address 0x0000 may not be executed. This occurrence is rare and affects very few applications.

To determine if your system is affected, test a statistically significant number of applications across the operating temperature, voltage and frequency ranges of the application. Affected systems will repeatably fail normal testing. Systems not affected will continue to not be affected over time.

Work around

Insert a NOP instruction at address 0x0000.

Date Codes that pertain to this issue:

All engineering and production devices.

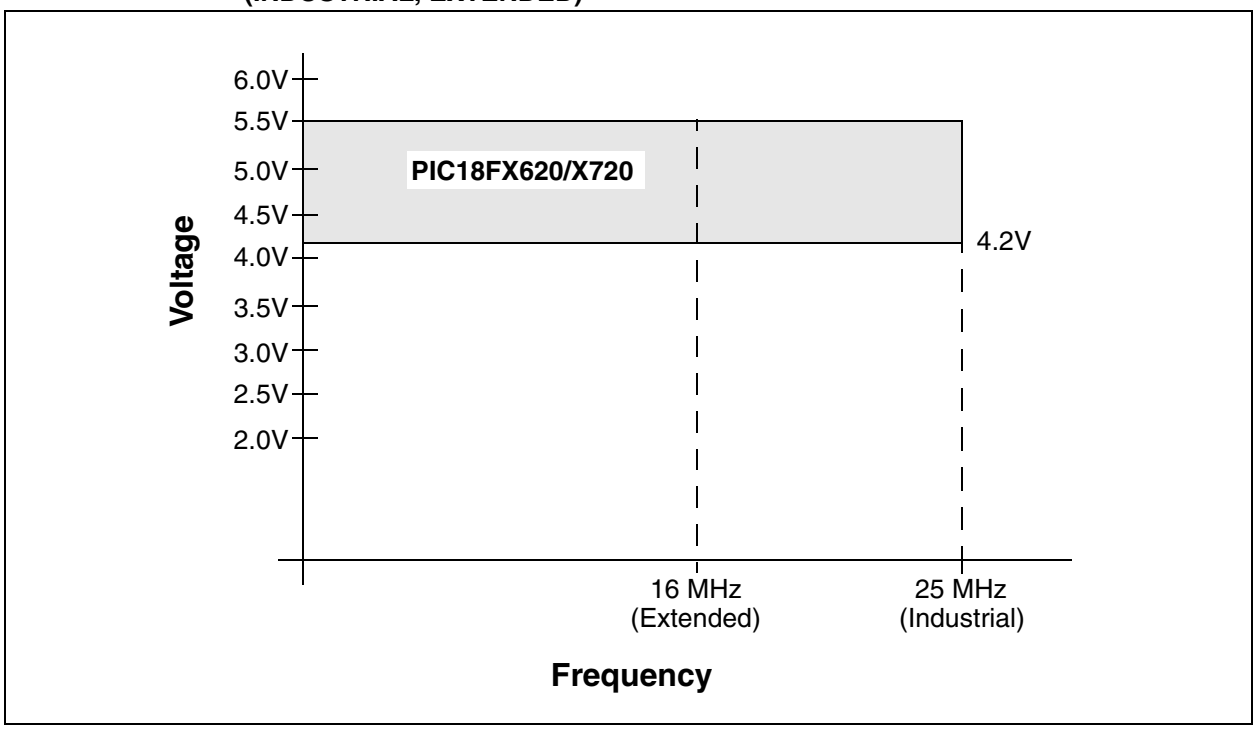
Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39609**B**), the following clarifications and corrections should be noted.

1. Module: Voltage-Frequency Graph

In **Section 26.0 "Electrical Characteristics"**, the following figure has been updated to clarify the voltage frequency for Extended devices.

FIGURE 26-3: PIC18F6620/6720/8620/8720 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL, EXTENDED)



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2. Module: Timing Diagrams and Specifications

Table 26-6: External Clock Timing Requirements for PIC18FX620/X720 devices (page 322) has been revised (changes and additions are shown in **bold** text).

TABLE 26-6: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	FOSC	External CLKI Frequency(1)	DC	25	MHz	EC, ECIO oscillator, PIC18FX620/X720 (Industrial)
			DC	**16**	**MHz**	**EC, ECIO oscillator, PIC18FX620/X720 (Extended)**
		Oscillator Frequency(1)	DC	4	MHz	RC oscillator
			0.1	4	MHz	XT oscillator
			4	25	MHz	HS oscillator (Industrial)
			4	**16**	**MHz**	**HS oscillator (Extended)**
			4	6.25	MHz	HS + PLL oscillator, PIC18FX620/X720 (Industrial)
			4	**4**	**MHz**	**HS + PLL oscillator, PIC18FX620/X720 (Extended)**
			5	33	kHz	LP Oscillator mode
1	TOSC	External CLKI Period(1)	40	—	ns	EC, ECIO oscillator, PIC18FX620/X720 (Industrial)
			62.5	**—**	**ns**	**EC, ECIO oscillator, PIC18FX620/X720 (Extended)**
		Oscillator Period(1)	250	—	ns	RC oscillator
			250	10,000	ns	XT oscillator
			40	250	ns	HS oscillator (Industrial)
			62.5	**250**	**ns**	**HS oscillator (Extended)**
			160	250	ns	HS + PLL oscillator, PIC18FX620/X720 (Industrial)
			250	**250**	**ns**	**HS + PLL oscillator, PIC18FX620/X720 (Extended)**
			30	200	µs	LP Oscillator mode

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

3. Module: CCP

In **Section 23.3.1 "Wake-up From Sleep"**, the list of peripheral interrupts which can wake the device from Sleep has been updated. From the list of 11 events, item 4 has been clarified and item 5 has been removed. The list now reads as follows:

1. PSP read or write.
2. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
3. TMR3 interrupt. Timer3 must be operating as an asynchronous counter.
4. CCP Capture mode interrupt (Capture will not occur).
5. MSSP (Start/Stop) bit detect interrupt.
6. MSSP transmit or receive in Slave mode (SPI/I^2C).
7. USART RX or TX (Synchronous Slave mode).
8. A/D conversion (when A/D clock source is RC).
9. EEPROM write operation complete.
10. LVD interrupt.

4. Module: Voltage Reference Specifications

In Table 26-2: Voltage Reference Specifications (page 317), parameter D311, VRAA, should be replaced with the following:

TABLE 26-2: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 3.0V < VDD < 5.5V, -40°C < TA < +125°C (unless otherwise stated).							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D311	VRAA	Absolute Accuracy	—	—	1/2	LSb	

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

5. Module: Memory Programming Requirements

In Table 26-4: Memory Programming Requirements (page 319), specification D124 (TREF) and Note 4 have been added:

TABLE 26-4: MEMORY PROGRAMMING REQUIREMENTS

DC Characteristics			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Data EEPROM Memory					
D124	TREF	Total Number of Erase/Write Cycles before Refresh **(Note 4)**	1M 100K	10M 1M	— —	E/W E/W	-40°C to +85°C -40°C to +125°C

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications are for programming the on-chip program memory through the use of table write instructions.

2: The pin may be kept in this range at times other than programming, but it is not recommended.

3: Retention time is valid, provided no other specifications are violated.

4: Refer to **Section 7.8 "Using the Data EEPROM"** for a more detailed discussion on data EEPROM endurance.

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6. Module: DC Characteristics

In **Section 26-3 "DC Characteristics"** (page 315), the specifications for VIL and VIH have been clarified and now read as follows (changes and additions are shown in **bold** text):

26.3 DC Characteristics PIC18F8720/8620/6720/6620 (Industrial, Extended) PIC18LF6620/8620/6720/8720 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended			
Param No.	**Sym**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		I/O ports:				
D030		with TTL buffer	VSS	0.15 VDD	V	VDD < 4.5V
D030A			—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D031		with Schmitt Trigger buffer	VSS	0.2 VDD	V	
		RC3 and RC4	VSS	0.3 VDD	V	
D032		$\overline{MCLR}$	VSS	0.2 VDD	V	
D032A		OSC1 (in XT, HS and LP modes) and T1OSI	VSS	0.2 VDD	V	
D033		**OSC1**	**VSS**	**0.3 VDD**	**V**	**HS, HSPLL modes**
D033A		**OSC1**	**VSS**	**0.2 VDD**	**V**	**RC, EC modes(1)**
D033B		**OSC1**	**VSS**	**0.3**	**V**	**XT, LP modes**
D034		**T13CKI**	**VSS**	**0.3**	**V**	
	VIH	**Input High Voltage**				
		I/O ports:				
D040		with TTL buffer	0.25 VDD + 0.8V	VDD	V	VDD < 4.5V
D040A			2.0	VDD	V	4.5V ≤ VDD ≤ 5.5V
D041		with Schmitt Trigger buffer	0.8 VDD	VDD	V	
		RC3 and RC4	0.7 VDD	VDD	V	
D042		$\overline{MCLR}$, OSC1 (EC mode)	0.8 VDD	VDD	V	
D042A		OSC1 and T1OSI	1.6	VDD	V	LP, XT, HS, HSPLL modes(1)
D043		**OSC1**	**0.7 VDD**	**VDD**	**V**	**HS, HSPLL modes**
D043A		**OSC1**	**0.8 VDD**	**VDD**	**V**	**EC mode**
D043B		**OSC1**	**0.9 VDD**	**VDD**	**V**	**RC mode(1)**
D043C		**OSC1**	**1.6**	**VDD**	**V**	**XT, LP modes**
D044		**T13CKI**	**1.6**	**VDD**	**V**	

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PICmicro® device be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Parameter is characterized but not tested.

7. Module: Instruction Set (BTG)

In Table 24-1: PIC18FXXXX Instruction Set (page 262), the BTG instruction has been changed (change shown in **bold** text).

TABLE 24-1: PIC18FXXXX INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word		Status Affected	Notes
			MSb	LSb		
BIT-ORIENTED FILE REGISTER OPERATIONS						
BTG f, **b**, a	Bit Toggle f	1	0111 bbba	ffff ffff	None	1, 2

8. Module: OSCCON Register

In the OSCCON register (Register 2-1, page 25), the Reset value for the SCS bit (OSCCON<0>) was incorrectly stated as R/W-1 and has been changed to R/W-0.

9. Module: A/D Converter Characteristics

In Table 26-25: A/D Converter Characteristics (page 340), specification A40 and Note 6 have been added:

TABLE 26-25: A/D CONVERTER CHARACTERISTICS: PIC18FXXXX (INDUSTRIAL, EXTENDED) PIC18LFXX20 (INDUSTRIAL)

Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
A01	NR	Resolution		—	—	10	bit	
A03	EIL	Integral Linearity Error		—	—	<±1	LSb	VREF = VDD = 5.0V
A04	EDL	Differential Linearity Error		—	—	<±1	LSb	VREF = VDD = 5.0V
A05	EG	Gain Error		—	—	<±1	LSb	VREF = VDD = 5.0V
A06	EOFF	Offset Error		—	—	<±1.5	LSb	VREF = VDD = 5.0V
A10	—	Monotonicity		guaranteed(2)			—	VSS ≤ VAIN ≤ VREF
A20 A20A	VREF	Reference Voltage (VREFH – VREFL)		1.8V 3V	— —	— —	V V	VDD < 3.0V VDD ≥ 3.0V
A21	VREFH	Reference Voltage High		AVSS	—	AVDD + 0.3V	V	
A22	VREFL	Reference Voltage Low		AVSS – 0.3V(5)	—	VREFH	V	
A25	VAIN	Analog Input Voltage		AVSS – 0.3V(5)	—	AVDD + 0.3V(5)	V	VDD ≥ 2.5V **(Note 3)**
A30	ZAIN	Recommended Impedance of Analog Voltage Source		—	—	2.5	kΩ	**(Note 4)**
A40	IAD	A/D Current from VDD	PIC18FXXXX	—	180	—	μA	Average current during conversion.
			PIC18LFXX20	—	90	—	μA	
A50	IREF	VREF Input Current **(Note 1)**		— —	— —	5 150	μA μA	During VAIN acquisition. During A/D conversion cycle.

Note 1: VSS ≤ VAIN ≤ VREF

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: For VDD < 2.5V, VAIN should be limited to <.5 VDD.

4: Maximum allowed impedance for analog voltage source is 10 kΩ. This requires higher acquisition times.

5: IVDD – AVDDI must be <3.0V and IAVSS – VSSI must be <0.3V.

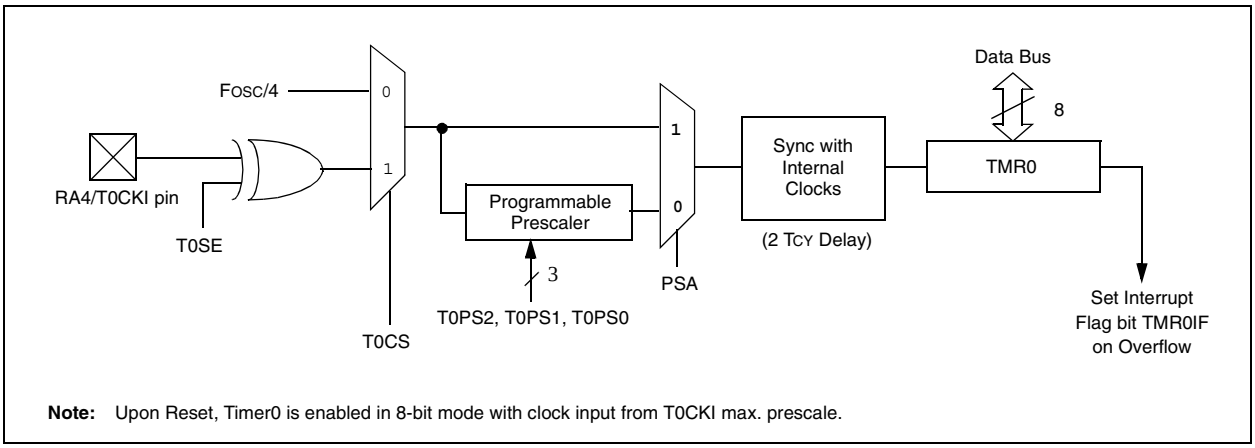
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10. Module: Timer0 Block Diagram in 8-Bit and 16-Bit Modes

The PSA multiplexor bit values in Figures 11-1 and 11-2 do not match the text description of the Timer0 PSA bit in the T0CON register.

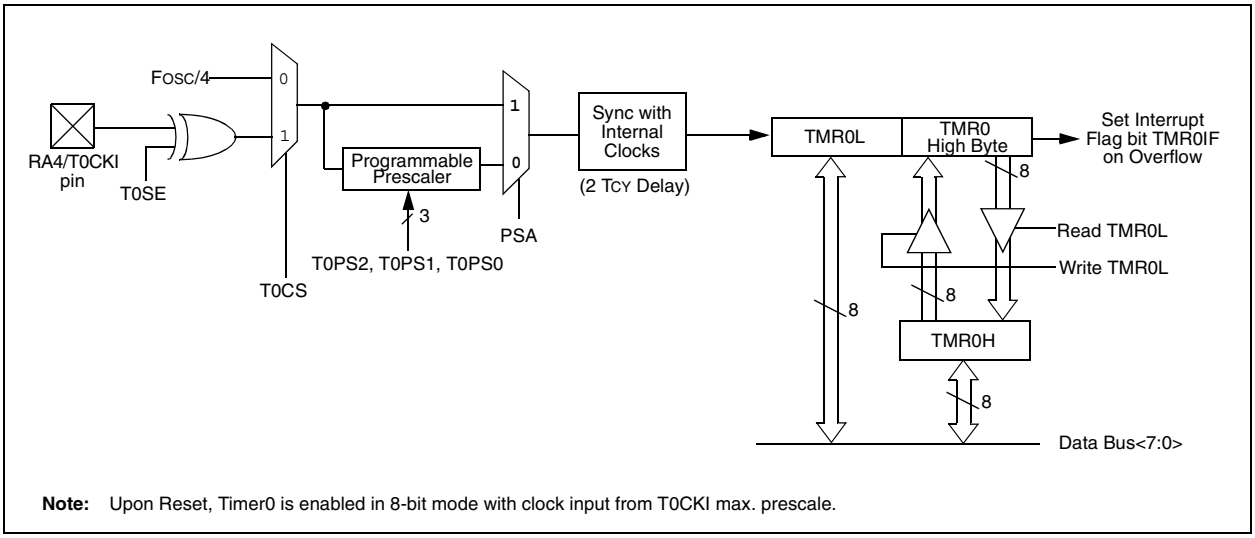
The bit values have been corrected by swapping the values as shown below (correct values are shown in **bold** text):

FIGURE 11-1: TIMER0 BLOCK DIAGRAM IN 8-BIT MODE



Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

FIGURE 11-2: TIMER0 BLOCK DIAGRAM IN 16-BIT MODE



Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

REVISION HISTORY

Rev A Document (10/2003)

First revision of this document. Listed silicon issue 1 (Core – Program Memory Space), 2 (External Memory Interface), 3 (I/O Ports), 4 (A/D), 5 (DAW Instruction), 6 (External Memory Interface), 7 (MSSP – All I^2C and SPI Modes) and 8 (MSSP – SPI, Slave Mode). Listed Data Sheet Clarification issue 1 (Comparator Voltage Reference), 2 (A/D), 3 (Data EEPROM), 4 (Memory), 5 (Timer0), 6 (Pin Diagrams), 7 (Voltage-Frequency Graph), 8 (A/D Converter Characteristics) and 9 (Electrical Characteristics).

Rev B Document (12/2004)

Updated device and revision ID information. Removed silicon issue 8 (MSSP – SPI, Slave Mode). Removed previous Data Sheet clarifications (1-6). Updated Data Sheet clarification 7 (Voltage-Frequency Graph), renumbered clarification 1 and added Data Sheet clarification 2 (Timing Diagrams and Specifications), 3 (CCP), 4 (Voltage Reference Specifications), 5 (Memory Programming Requirements), 6 (DC Characteristics), 7 (Instruction Set (BTG)), 8 (OSCCON Register), 9 (A/D Converter Characteristics) and 10 (Timer0 Block Diagram in 8-Bit and 16-Bit Modes).

Rev C Document (05/2005)

Added silicon issue 8 (Reset).

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