



PIC18F87J11 FAMILY

PIC18F87J11 Family Rev. A2 Silicon Errata

The PIC18F87J11 Family parts you have received conform functionally to the Device Data Sheet (DS39778B), except for the anomalies described below.

Any Data Sheet Clarification issues related to the PIC18F87J11 Family devices will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F87J11 Family devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F66J11	0100 0100 010	0 0010
PIC18F66J16	0100 0100 011	0 0010
PIC18F67J11	0100 0100 100	0 0010
PIC18F86J11	0100 0100 111	0 0010
PIC18F86J16	0100 0101 000	0 0010
PIC18F87J11	0100 0101 001	0 0010

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

1. Module: Oscillator Configurations (PLL)

When Phase Lock Loop (PLL) is enabled, if the PLL input frequency is higher than 8 MHz, there may be problems accessing the RAM.

Work around

Limit the PLL input frequency from 4 MHz to 8 MHz. This will cause the system clock to operate from 16 MHz to 32 MHz.

If it is necessary to run the device above 32 MHz, do not enable PLL and use the EC mode.

Date Codes that pertain to this issue:

All engineering and production devices.

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REVISION HISTORY

Rev A Document (9/2007)

First revision of this document. Silicon issue 1 (Oscillator Configurations – PLL).

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09/10/07