

**MICROCHIP****PIC18F6585/8585/6680/8680****PIC18F6585/8585/6680/8680 Data Sheet Errata****Clarifications/Corrections to the Data Sheet:**

In the Device Data Sheet (DS30491C), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F6585/8585/6680/8680 will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Device Overview (Pinout Descriptions)

The last page of Table 1-2 changes the pin count for the TQFP package, for the pins indicated in bold text.

TABLE 1-2: PIC18F6585/8585/6680/8680 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PIC18F6X8X		PIC18F8X8X			
	TQFP	PLCC	TQFP			
RJ5/CE CE	—	—	40	I/O O	ST TTL	Digital I/O External memory chip enable.
RJ6/LB RJ6 LB	—	—	41	I/O O	ST TTL	Digital I/O. External memory low byte select.
RJ7/UB RJ7 UB	—	—	42	I/O O	ST TTL	Digital I/O. External memory high byte select.
Vss	9, 25, 41, 56	19, 36, 53, 68	11, 31, 51, 70	P	—	Ground reference for logic and I/O pins.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)

- Note 1:** Alternate assignment for CCP2 in all operating modes except Microcontroller – applies to PIC18F8X8X only.
2: Default assignment when CCP2MX is set.
3: External memory interface functions are only available on PIC18F8X8X devices.
4: CCP2 is multiplexed with this pin by default when configured in Microcontroller mode; otherwise, it is multiplexed with either RB3 or RC1.
5: PORTH and PORTJ are only available on PIC18F6585 (80-pin) devices.
6: PSP is available in Microcontroller mode only.
7: On PIC18F8X8X devices, these pins can be multiplexed with RH7/RH6 by changing the ECCPMX configuration bit.

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2. Module: Master Synchronous Serial Port Module (SPI Slave Mode)

The pin number of the Serial Pin Select (SPI) mode's slave select signal ($\overline{SS}$) is changed to the following:

- PIC18F6X8X, TQFP package – Pin 27
- PIC18F6X8X, PLCC package – Pin 38
- PIC18F8X8X, TQFP package – Pin 33

The $\overline{SS}$ signal is on the same pin as the RA5/AN4/LVDIN signals, not on the pin with the RF7 signal.

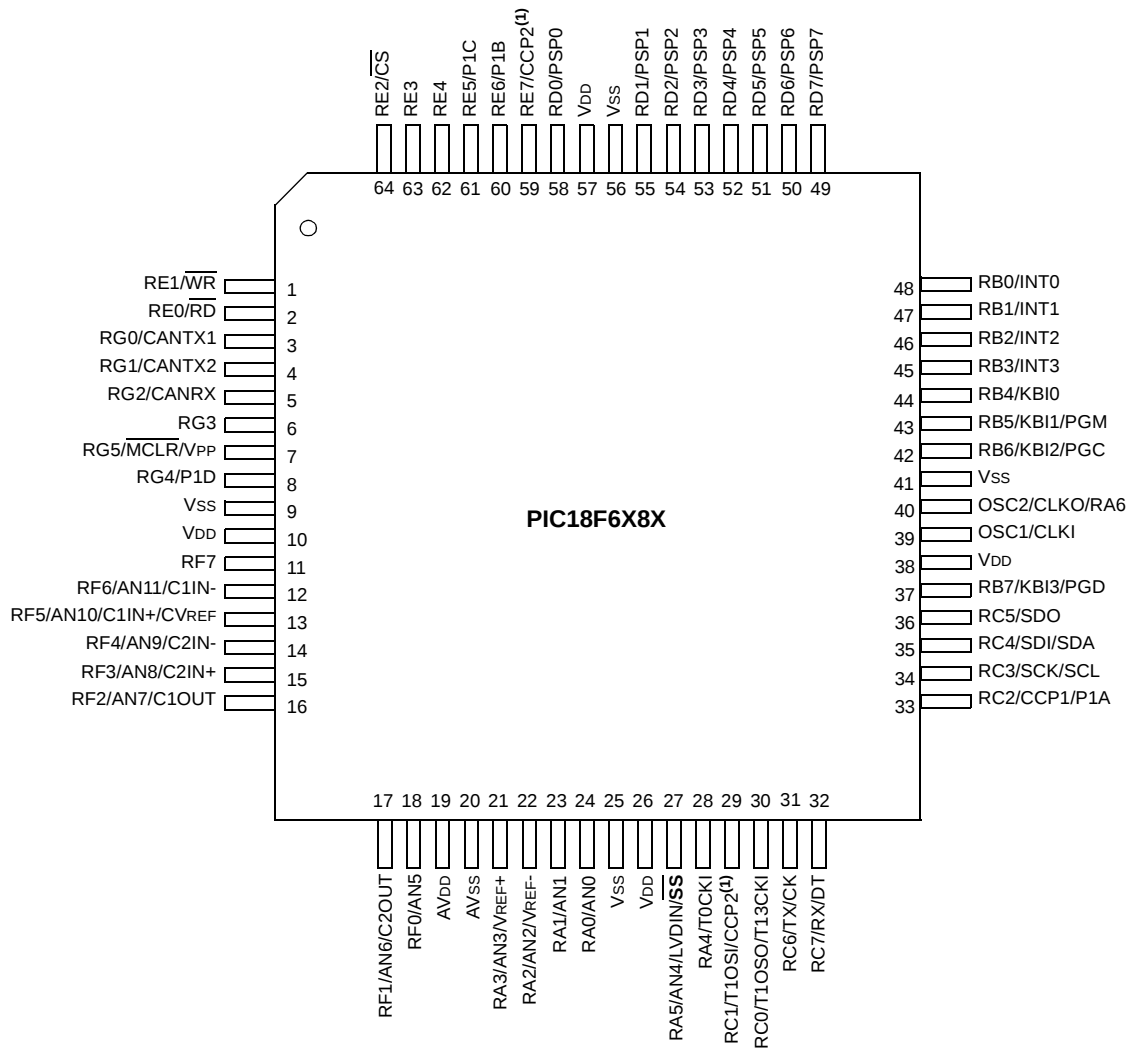
This change is made in the following locations, each indicated by bold text:

- Pin Diagram, PIC18F6X8X, 64-Pin TQFP package – Page 3
- Pin Diagram, PIC18F6X8X, 68-Pin PLCC package – Page 4
- Pin Diagram, PIC18F8X8X, 80-Pin TQFP package – Page 5
- Block diagram, PIC18F6X8X – Page 6
- Block diagram, PIC18F8X8X – Page 7
- Table 1-2, PIC18F6585/8585/6680/8680 Pinout I/O Descriptions – Page 8
- Figure 10-2, Block Diagram of RA3:RA0 and RA5/ $\overline{SS}$ Pins – Page 9
- Figure 10-15, RF7 Pin Block Diagram – Page 9
- Table 10-11, PORTF Functions – Page 9
- **Section 17.3 “SPI Mode”** – Page 10
- Figure 17-1, MSSP Block Diagram (SPI Mode) – Page 10

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Pin Diagrams

64-Pin TQFP

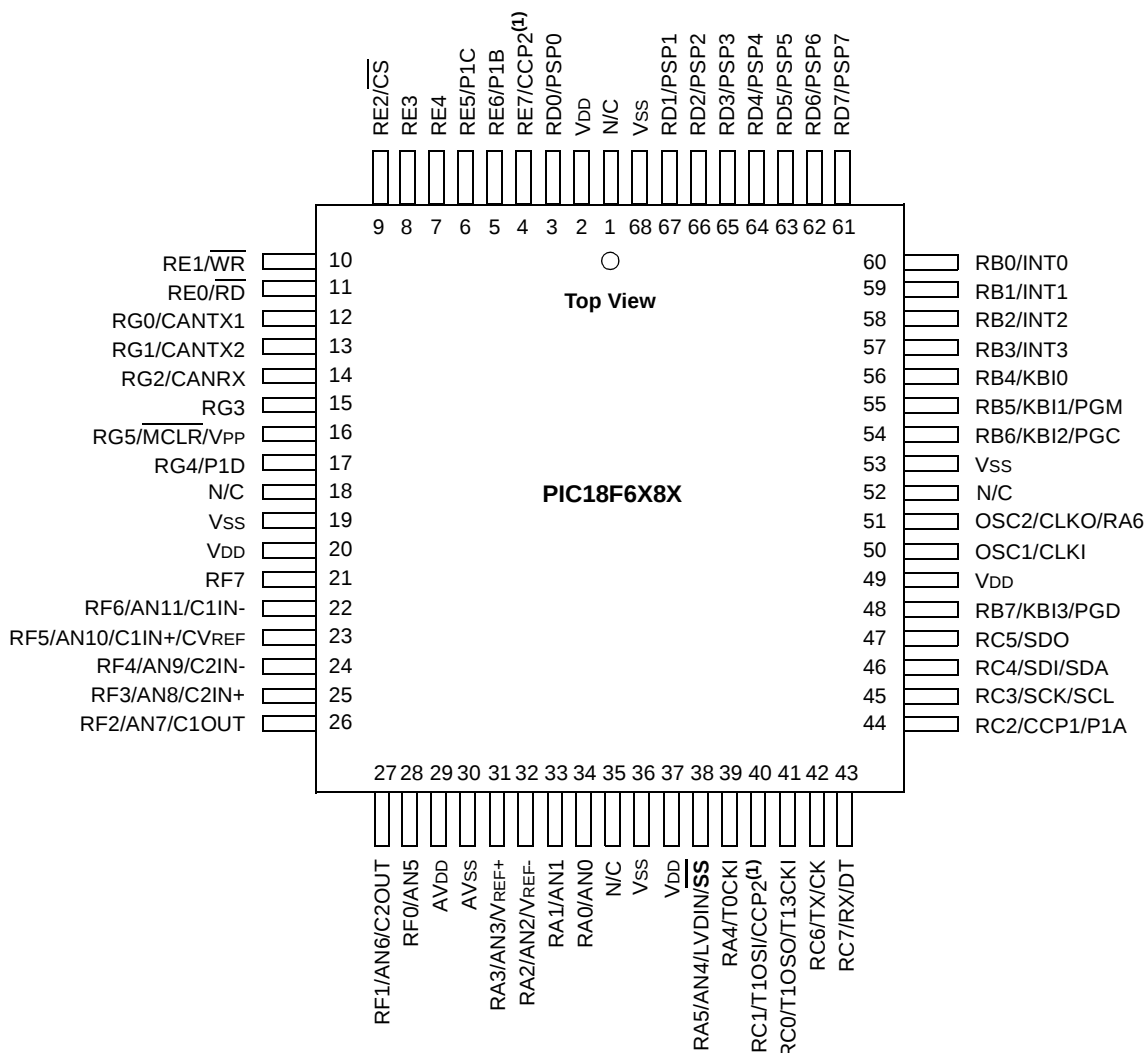


Note 1: CCP2 pin placement depends on CCP2MX setting.

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Pin Diagrams (Continued)

68-Pin PLCC

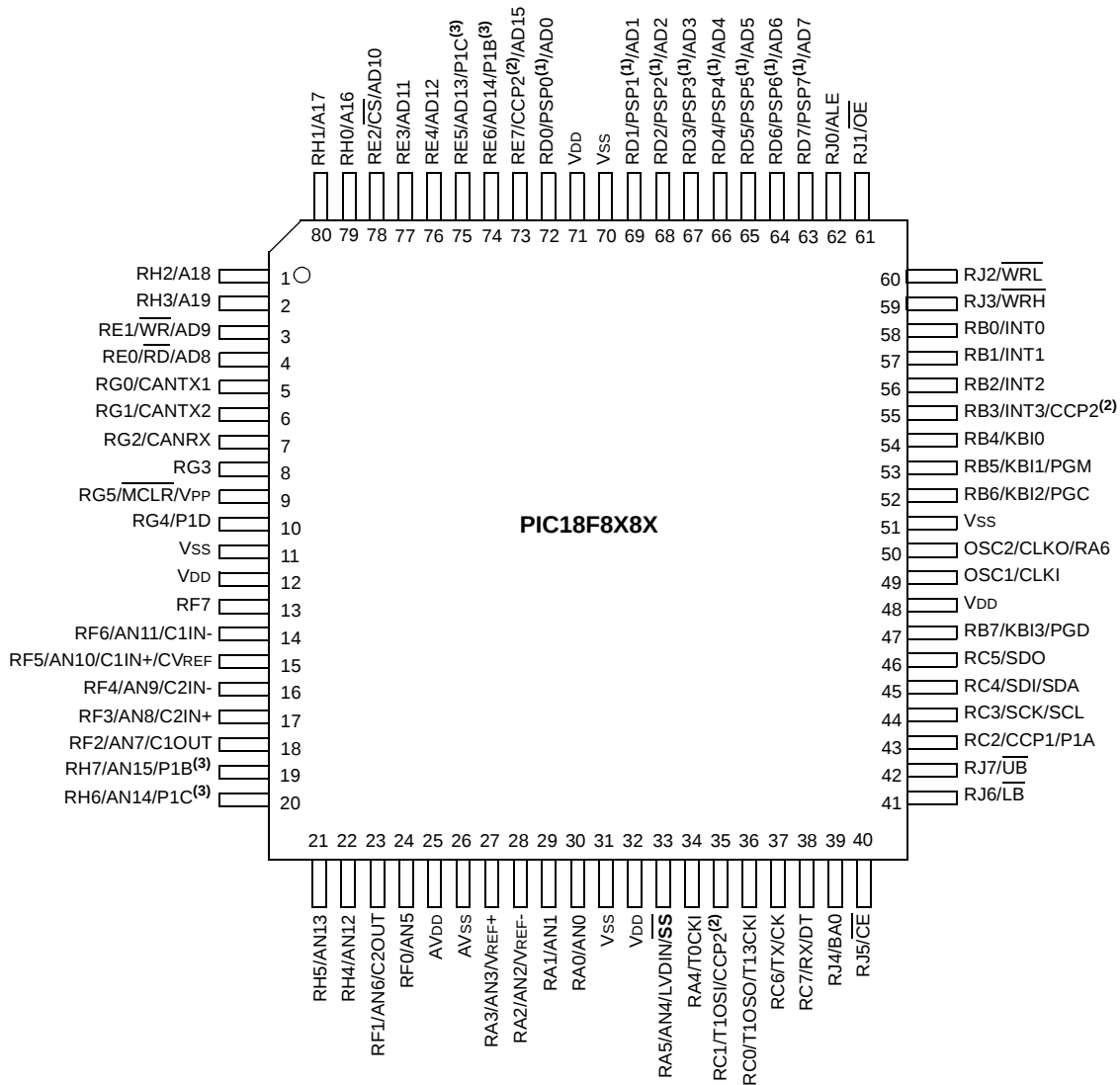


Note 1: CCP2 pin placement depends on CCP2MX setting.

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Pin Diagrams (Continued)

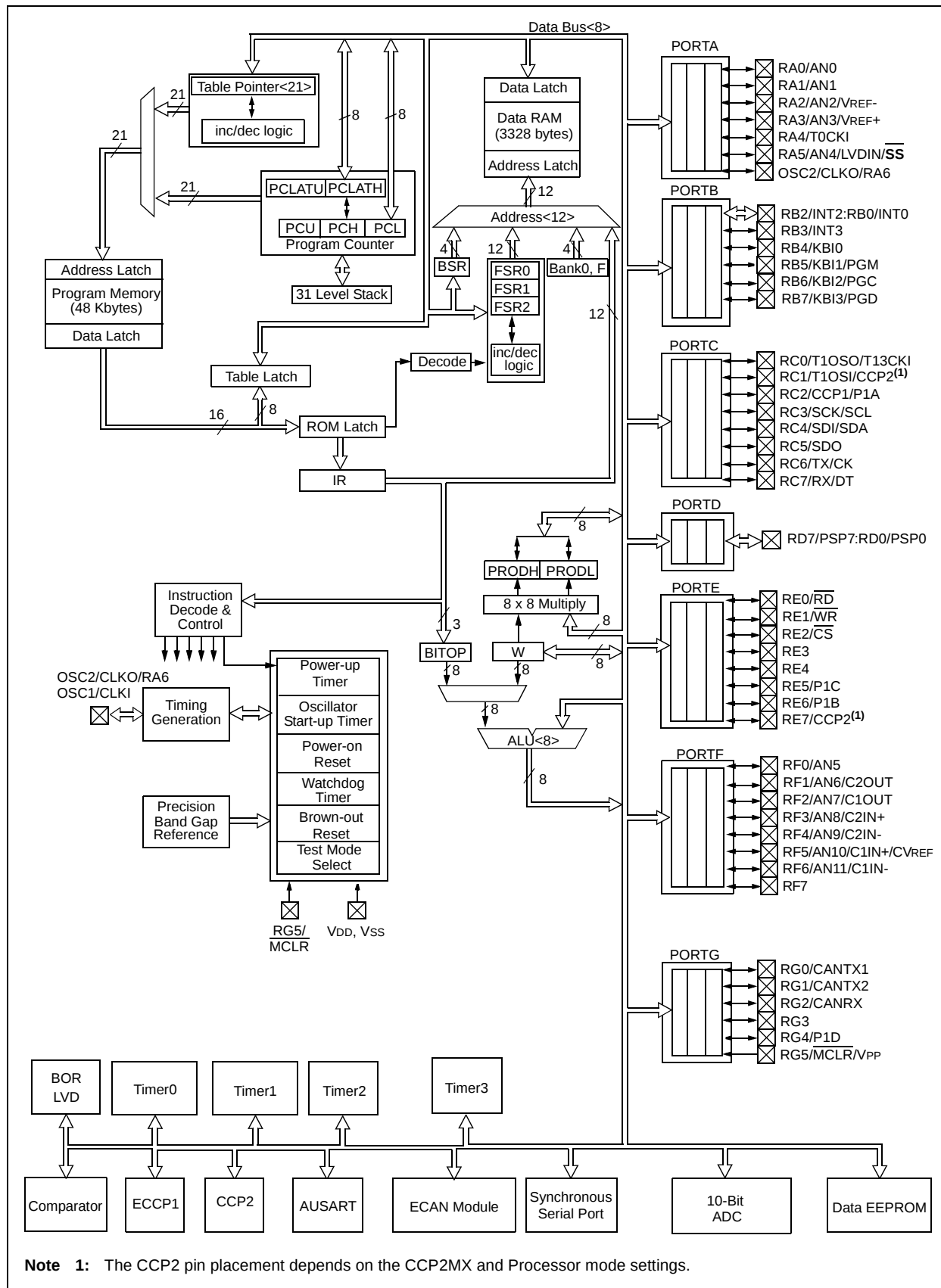
80-Pin TQFP



- Note 1:** PSP is available only in Microcontroller mode.
- Note 2:** CCP2 pin placement depends on CCP2MX and Processor mode settings.
- Note 3:** P1B and P1C pin placement depends on ECCPMX setting.

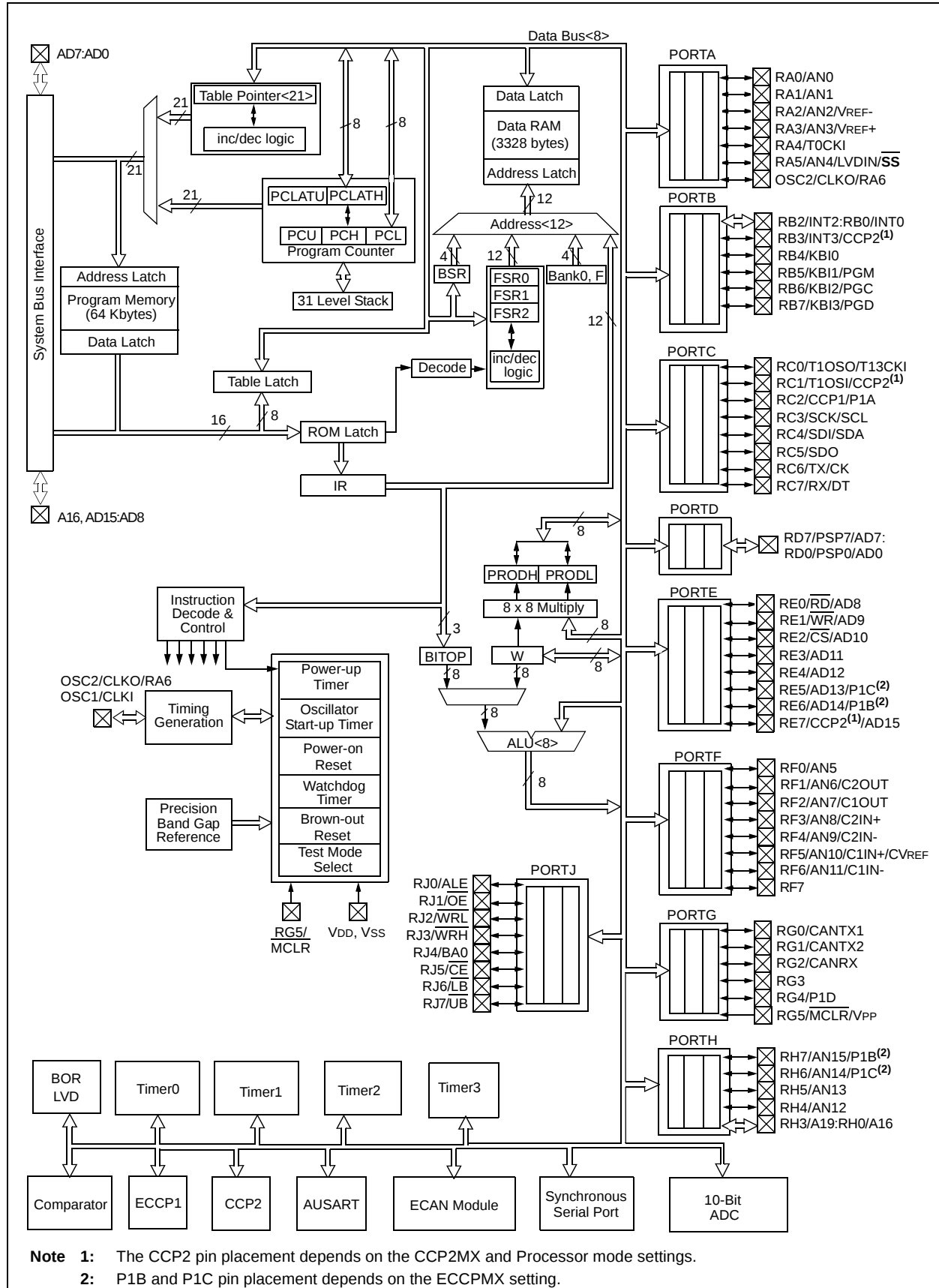
PIC18F6585/8585/6680/8680

FIGURE 1-1: PIC18F6X8X BLOCK DIAGRAM



PIC18F6585/8585/6680/8680

FIGURE 1-2: PIC18F8X8X BLOCK DIAGRAM



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TABLE 1-2: PIC18F6585/8585/6680/8680 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PIC18F6X8X		PIC18F8X8X			
	TQFP	PLCC	TQFP			
RA0/AN0	24	34	30	I/O	TTL	PORTA is a bidirectional I/O port.
RA0 AN0				I	Analog	
RA1/AN1	23	33	29	I/O	TTL	Digital I/O. Analog input 1.
RA1 AN1				I	Analog	
RA2/AN2/VREF-	22	32	28	I/O	TTL	Digital I/O. Analog input 2. A/D reference voltage (Low) input.
RA2 AN2				I	Analog	
VREF-				I	Analog	
RA3/AN3/VREF+	21	31	27	I/O	TTL	Digital I/O. Analog input 3. A/D reference voltage (High) input.
RA3 AN3				I	Analog	
VREF+				I	Analog	
RA4/T0CKI	28	39	34	I/O	ST/OD	Digital I/O – Open-drain when configured as output. Timer0 external clock input.
RA4				I	ST	
T0CKI				I	ST	
RA5/AN4/LVDIN/ <u>SS</u>	27	38	33	I/O	TTL	Digital I/O. Analog input 4. Low-voltage detect input. SPI slave select input. See the OSC2/CLKO/RA6 pin.
RA5				I	Analog	
AN4				I	Analog	
LVDIN				I	Analog	
<u>SS</u>				I	TTL	
RA6						

Note: The SS signal is removed from the PORTF portion of the same table, where it had been associated with the RF7 signal.

FIGURE 10-2: BLOCK DIAGRAM OF RA3:RA0 AND RA5/SS PINS

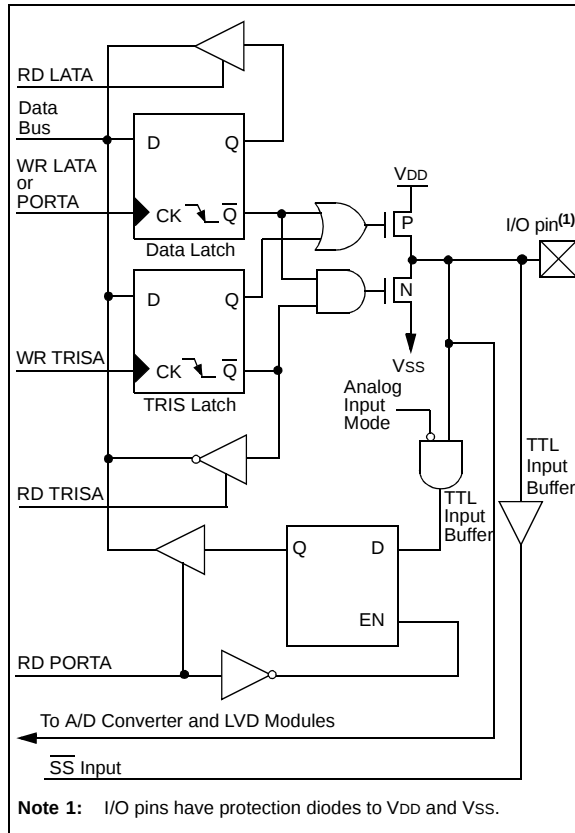
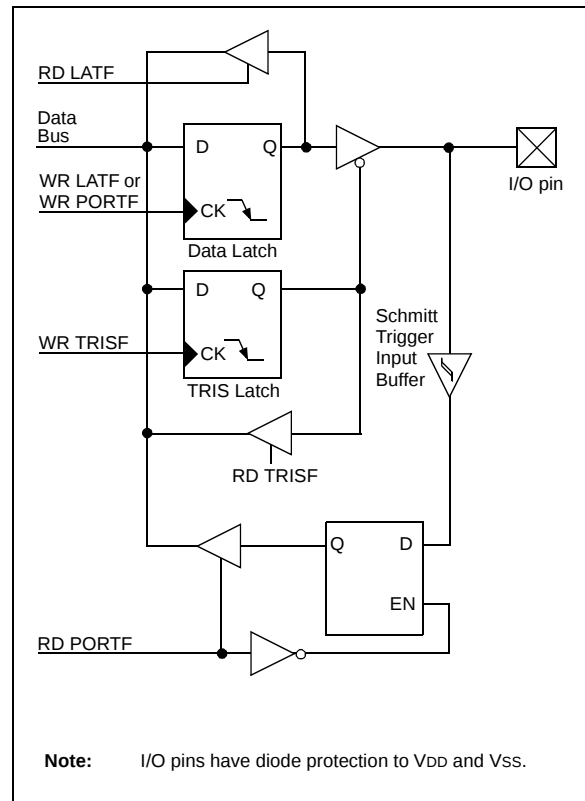


FIGURE 10-15: RF7 PIN BLOCK DIAGRAM



Note: The $\overline{SS}$ signal was removed from this diagram.

TABLE 10-11: PORTF FUNCTIONS

Name	Bit#	Buffer Type	Function
RF0/AN5	bit 0	ST	Input/output port pin or analog input.
RF1/AN6/C2OUT	bit 1	ST	Input/output port pin, analog input or comparator 2 output.
RF2/AN7/C1OUT	bit 2	ST	Input/output port pin, analog input or comparator 1 output.
RF3/AN8/C2IN+	bit 3	ST	Input/output port pin, analog input or comparator 2 input (+).
RF4/AN9/C2IN-	bit 4	ST	Input/output port pin, analog input or comparator 2 input (-).
RF5/AN10/C1IN+/CVREF	bit 5	ST	Input/output port pin, analog input, comparator 1 input (+) or comparator reference output.
RF6/AN11/C1IN-	bit 6	ST	Input/output port pin, analog input or comparator 1 input (-).
RF7	bit 7	ST/TTL	Input/output port pin or slave select pin for synchronous serial port.

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note: The $\overline{SS}$ signal was removed from this table's bottom row.

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17.3 SPI Mode

The SPI mode allows eight bits of data to be synchronously transmitted and received simultaneously. All four modes of SPI are supported. To accomplish communication, typically three pins are used:

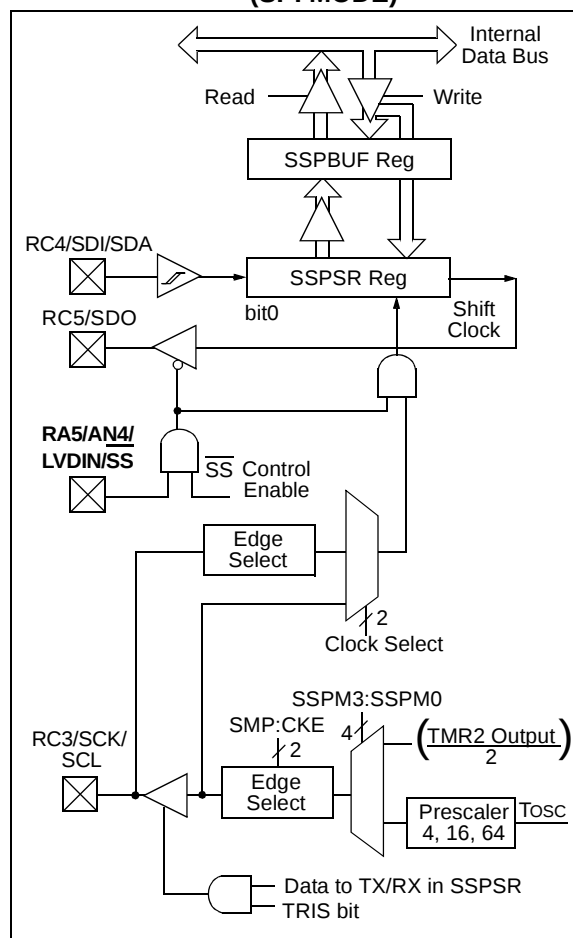
- Serial Data Out (SDO) – RC5/SDO
- Serial Data In (SDI) – RC4/SDI/SDA
- Serial Clock (SCK) – RC3/SCK/SCL

Additionally, a fourth pin may be used when in a Slave mode of operation:

- Slave Select ($\overline{SS}$) – **RA5/AN4/LVDIN/ $\overline{SS}$**

Figure 17-1 shows the block diagram of the MSSP module when operating in SPI mode.

FIGURE 17-1: MSSP BLOCK DIAGRAM (SPI MODE)



REVISION HISTORY

Rev A Document (3/2008)

Original release of this errata. Data Sheet Clarification 1 (Device Overview – Pinout Descriptions).

Rev B Document (8/2008)

Added Data Sheet Clarification 2 (Master Synchronous Serial Port Module, SPI Slave Mode).

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NOTES:

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