

PIC18F45J10 Family Silicon Errata and Data Sheet Clarification

The PIC18F45J10 family devices that you have received conform functionally to the current Device Data Sheet (DS39682E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC18F45J10 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (A4).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICKit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICKit™ 3.
2. From the main menu in MPLAB IDE, select Configure>Select Device, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (Debugger>Select Tool).
4. Perform a "Connect" operation to the device (Debugger>Connect). Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F45J10 family silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾		
		A2	A3	A4
PIC18F24J10	1D0h	1h	3h	3h
PIC18F25J10	1C0h			
PIC18F44J10	1D2h			
PIC18F45J10	1C2h			
PIC18LF24J10	1D4h			
PIC18LF25J10	1C4h			
PIC18LF44J10	1D6h			
PIC18LF45J10	1C6h			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the "PIC18F2XJXX/4XJXX Family Flash Microcontroller Programming Specification" (DS39687) for detailed information on Device and Revision IDs for your specific device.

PIC18F45J10 FAMILY

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾		
				A2	A3	A4
Timer1	16-Bit Counter	1.	In 16-Bit Asynchronous Counter mode or 16-Bit Asynchronous Oscillator mode, the TMR1H buffer does not update when TMR1L is read.	X	X	X
EUSART	Reception	2.	In asynchronous duplex communication, received data can get corrupted if any bit of the TXSTA register is modified during reception.	X	X	X
EUSART	Baud Rate	3.	In Synchronous mode, EUSART baud rates using SPBRG values of '0' and '1' may not function correctly.	X	X	X
EUSART	Buffer	4.	After the last received byte has been read from the EUSART Receive Buffer (RCREG), the value is no longer valid for subsequent read operations.	X	X	X
EUSART	9-Bit	5.	In 9-Bit Asynchronous Full-Duplex Receive mode, received data may be corrupted if the TX9D bit (TXSTA<0>) is not modified immediately after RCIDL (BAUDCON<6>) is set.	X	X	X
MSSP	SPI	6.	In SPI mode, the Buffer Full flag bit (BF, SSPxSTAT<0>), the Write Collision Detect bit (WCOL, SSPxCON1<7>) and the Receive Overflow Indicator bit (SSPOV, SSPxCON1<6>) are not reset upon disabling the SPI module.	X	X	X
MSSP	I ² C™	7.	After a Power-on Reset, I ² C mode may not initialize properly if only the SCLx and SDAx pins have been configured as either inputs or outputs.	X	X	X
Core	Program Memory	8.	Writes to program memory address, 300000h, that are not blocked, can cause different locations of the program memory to become corrupted.	X	X	X
EUSART	Transmission	9.	In rare situations, one or more extra zero bytes may appear in packets transmitted with the module in Asynchronous mode.	X	X	X
ECCP	PWM	10.	When switching direction in Full-Bridge PWM mode, the modulated outputs will switch immediately instead of waiting for the next PWM cycle. This may generate unexpected short pulses on the modulated outputs.	X	X	X
MSSP	I ² C™	11.	When configured for I ² C slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read within a window after the SSPxIF interrupt (PIR1<3>) has occurred.	X	X	X
EUSART	Interrupt	12.	In rare situations, unexpected results may occur if interrupts are disabled and enabled and a two-cycle instruction is executed.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A4).

1. Module: Timer1

In 16-Bit Asynchronous Counter mode or 16-Bit Asynchronous Oscillator mode, the TMR1H buffer does not update when TMR1L is read. This issue only affects the reading of the TMR1H registers. The timers increment and set the interrupt flags as expected. The Timer registers can also be written as expected.

Work around

Use the 8-bit mode by clearing the RD16 (T1CON<7>) bit or use the synchronization option by clearing, T1SYNC (T1CON<2>).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

2. Module: EUSART

In asynchronous duplex communication, the reception can get corrupted if any bit of the TXSTA register is modified during a reception.

Work around

The CSRC (TXSTA<7>) bit should not be set. Though this is a "don't care" bit in Asynchronous mode, make sure that this bit is not set.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

3. Module: EUSART

In Synchronous mode, EUSART baud rates using SPBRG values of '0' and '1' may not function correctly.

Work around

Use another baud rate configuration to generate the desired baud rate.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

4. Module: EUSART

After the last received byte has been read from the EUSART Receive Buffer (RCREG), the value is no longer valid for subsequent read operations. The RCREG register should only be read once for each byte received.

Work around

After each byte is received from the EUSART, store the byte into a user variable. To determine when a byte is available to read from RCREG, poll the RCIDL bit (BAUDCON<6>) for a low-to-high transition, or use the EUSART Receive Interrupt Flag (RCIF, PIR1<5>).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

5. Module: EUSART

In 9-Bit Asynchronous Full-Duplex Receive mode, received data may be corrupted if the TX9D bit (TXSTA<0>) is not modified immediately after RCIDL (BAUDCON<6>) is set.

Work around

Only write to TX9D when a reception is not in progress (RCIDL = 1). No interrupt is associated with RCIDL, therefore, it must be polled in software to determine when TX9D can be updated.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

PIC18F45J10 FAMILY

6. Module: MSSP

In SPI mode, the Buffer Full flag bit (BF, SSPxSTAT<0>), the Write Collision Detect bit (WCOL, SSPxCON1<7>) and the Receive Overflow Indicator bit (SSPOV, SSPxCON1<6>) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPxCON1 register).

For example, if SSPxBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPxBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

Work around

Ensure that if the buffer is full, SSPxBUF is read (thus, clearing the BF flag) and WCOL is clear before disabling the MSSP module. If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

7. Module: MSSP (I²C™ Mode)

After a Power-on Reset, the I²C mode may not initialize properly by just configuring the SCLx and SDAx pins as either inputs or outputs. This has only been seen in a few unique system environments.

A test of a statistically significant sample of pre-production systems, across the voltage and current range of the application's power supply, should indicate if a system is susceptible to this issue.

Work around

Before configuring the module for I²C operation:

1. Configure the SCLx and SDAx pins as outputs by clearing their corresponding TRIS bits.
2. Force SCLx and SDAx low by clearing the corresponding LAT bits.
3. While keeping the LAT bits clear, configure SCLx and SDAx as inputs by setting their TRIS bits.

Once this is done, use the SSPxCON1 and SSPxCON2 registers to configure the proper I²C mode as before.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

8. Module: Core (Program Memory Space)

Writes to program memory address, 300000h, that are not blocked, can cause the program memory at different locations to be corrupted.

Work around

Do not write to address, 300000h.

If you wish to modify the contents of the Configuration registers:

1. Modify the Configuration Words located at the end of the user memory:
 - For PIC18FX5J10 devices – 7FF4h
 - For PIC18FX4J10 devices – 3FF4h
2. Issue a Reset command.

This will reload the Configuration registers with the new configuration setting.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

9. Module: EUSART

In rare situations, one or more extra zero bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted; only unwanted (extra) zero bytes are observed in the packet.

This situation has only been observed when the contents of the Transmit Buffer (TXREG) are transferred to the TSR during the transmission of a Stop bit. For this to occur, three things must happen in the same instruction cycle:

- TXREG is written to
- The baud rate counter overflows (at the end of the bit period)
- A Stop bit is being transmitted (shifted out of TSR)

Work around

If possible, do not use the module's double-buffer capability. Instead, load the TXREG register when the TRMT bit (TXSTA<1>) is set, indicating the TSR is empty.

If double-buffering is used and back-to-back transmission is performed, load TXREG immediately after TXIF is set or wait 1 bit time after TXIF is set. Both solutions prevent writing TXREG while a Stop bit is transmitted.

The TXIF bit is set at the beginning of the Stop bit transmission.

If transmission is intermittent, do one of the following:

- Wait for the TRMT bit to be set before loading TXREG
- Use a free timer resource to time the baud period:
 1. Set up the timer to overflow at the end of the Stop bit.
 2. Start the timer when you load the TXREG.

Do not load the TXREG when the timer is about to overflow.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

10. Module: ECCP (Enhanced PWM)

When switching direction in Full-Bridge PWM mode, the modulated outputs will switch immediately instead of waiting for the next PWM cycle. This may generate unexpected short pulses on the modulated outputs.

Work around

Disable the PWM or set the duty cycle to zero prior to switching directions.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

11. Module: MSSP – I²C™

When configured for I²C slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature.
This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPxIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

PIC18F45J10 FAMILY

12. Module: EUSART

In rare situations, when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTAx<7> = 0)
- The EUSART is re-enabled (RCSTAx<7> = 1)
- A two-cycle instruction is executed immediately after setting SPEN = 1

Work around

Add a 2 Tcy delay after any instruction that re-enables the EUSART module (sets SPEN = 1). See [Example 1](#).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

EXAMPLE 1: RE-ENABLING A EUSART MODULE

```
;Initial conditions: SPEN = 0 (module disabled)
;To re-enable the module:
;Re-Initialize TXSTAx, BAUDCONx, SPBRGx, SPBRGHx registers (if needed)
;Re-Initialize RCSTAx register (if needed), but do not set SPEN = 1 yet

;Now enable the module, but add a 2-Tcy delay before executing any two-cycle
;instructions
bsf RCSTA1, SPEN;or RCSTA2 if EUSART2
nop;1 Tcy delay
nop;1 Tcy delay (two total)

;CPU may now execute 2 cycle instructions
```

PIC18F45J10 FAMILY

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39682E):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with PIC18FJ Microcontrollers

Section 2.4 Voltage Regulator Pins (VCAP/VDDCORE) has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins (VCAP/VDDCORE)

When the regulator is enabled (F devices), a low-ESR ($< 5\Omega$) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 μF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in [Table 2-1](#). Capacitors with equivalent specifications can be used.

Designers may use [Figure 2-3](#) to evaluate ESR equivalence of candidate devices.

It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 24.0 “Electrical Characteristics”** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 24.0 “Electrical Characteristics”** for information on VDD and VDDCORE.

Note that the “LF” versions of some low pin count PIC18FJ parts (e.g., the PIC18LF45J10) do not have the ENVREG pin. These devices are provided with the voltage regulator permanently disabled; they must always be provided with a supply voltage on the VDDCORE pin.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP

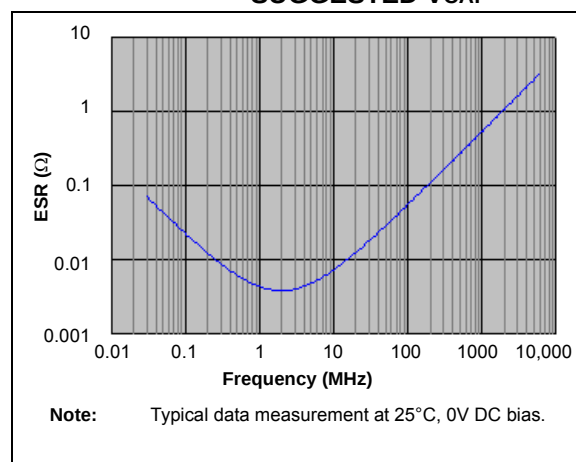


TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 μF	$\pm 10\%$	16V	-55 to 125°C
TDK	C3216X5R1C106K	10 μF	$\pm 10\%$	16V	-55 to 85°C
Panasonic	ECJ-3YX1C106K	10 μF	$\pm 10\%$	16V	-55 to 125°C
Panasonic	ECJ-4YB1C106K	10 μF	$\pm 10\%$	16V	-55 to 85°C
Murata	GRM32DR71C106KA01L	10 μF	$\pm 10\%$	16V	-55 to 125°C
Murata	GRM31CR61C106KC31L	10 μF	$\pm 10\%$	16V	-55 to 85°C

PIC18F45J10 FAMILY

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

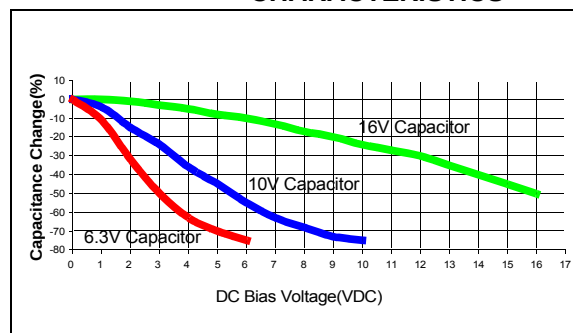
Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as $\pm 10\%$ to $\pm 20\%$ (X5R and X7R), or $-20\%/+80\%$ (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: $\pm 15\%$, over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of $+22\%/-82\%$. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal voltage regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2009)

Combined the issues from the pre-existing A2 and A3 silicon documents, carrying forward silicon issue 1 (Timer1), 2-5 (EUSART), 6 (MSSP), 7 (MSSP – I²C Mode), 8 (Core – Program Memory Space), 9 (EUSART) and 10 (ECCP – Enhanced PWM). Added issue 11 (MSSP) and 12 (EUSART). Added silicon revision A4.

There were no existing data sheet clarifications to compile into this document. None were added.

This document replaces these errata documents:

- DS80269C, “PIC18F24J10/25J10/44J10/45J10 Rev. A2 Silicon Errata”
- DS80380A, “PIC18F24J10/25J10/44J10/45J10 Rev. A3 Silicon Errata”

Rev B Document 10/2010

Added data sheet clarification issue 1 (Guidelines For Getting Started with PIC18FJ Microcontrollers).

PIC18F45J10 FAMILY

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICTail, REAL ICE, rLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2010, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-60932-598-5

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==



Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://support.microchip.com>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-213-7830
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820