PIC18F24K20/25K20/44K20/45K20 Silicon Errata and Data Sheet Clarification

The PIC18F24K20/25K20/44K20/45K20 devices that you have received conform functionally to the current Device Data Sheet (DS41303**H**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F24K20/25K20/44K20/45K20 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**AF**).

Data Sheet clarifications and corrections start on page 13, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F24K20/25K20/44K20/45K20 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1) (11-bit)	Revision ID for Silicon Revision(2) (5-bit)								
		A4	A7	A9	AB	A4	A7	A8	AE	AF
PIC18F24K20	105h	0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
PIC18F25K20	103h	0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
PIC18F44K20	104h	0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
PIC18F45K20	102h	0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID:DEVREV".

2: Refer to the *"PIC18F2XK20/4XK20 Flash Memory Programming Specification"* (DS41297) for detailed information on Device and Revision IDs for your specific device.

3: Shaded cells in this table indicate older device revisions that are no longer in production.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)								
				A4	A7	A9	AB	A4	A7	A8	AE	AF
				0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
ECCP	CCP1CON	1.	Changing CCP1M bits may cause capture of Timer1 value.	X	X	X	X					
ECCP	Full-Bridge mode	2.	Direction change issue.	X	X	X	X					
MSSP SPI	SPI Clock	3.	Shortened SPI high time.	X	X	X	X					
MSSP I^2C	Slew Rate	4.	Slow slew rate when SLRCON<2> is set.	X	X	X	X					
ADC	Offset	5.	Time dependent on offset.	X	X	X	X					
MSSP I^2C	Receiving	6.	Address may be received as data.	X	X	X	X					
MSSP I^2C	Master mode	7.	Master mode not functional.	X								
MSSP SPI	SPI Master	8.	Improper sampling of last bit.	X	X	X	X					
MSSP SPI	SPI Master	9.	$\overline{SS}$PBUF improperly reloads on $\overline{SS}$ pin transitions.	X	X	X	X					
MSSP SPI	SPI Master	10.	Improper extra pulse on SCK pin.	X	X	X	X					
EUSART	Synchronous Master mode	11.	Duty cycle of CK output is skewed when SPBRG is odd.	X	X	X	X					
EUSART	Synchronous Master mode	12.	LS bit corruption during transmission when SPBRG = 3.	X	X	X	X					
EUSART	Synchronous Master mode	13.	Clock fails to stop at end of character transmission when SPBRG = 0.	X	X	X	X					
Internal Fixed Voltage Reference (FVR)	—	14.	FVRST bit activates prematurely.	X	X							
High Low Voltage Detect (HLVD)	—	15.	IVRST bit activates prematurely.	X	X							
BOR	FVR	16.	Unexpected BOR occurrence.	X	X							
System Clocks	—	17.	HFINTOSC output accuracy.	X	X	X	X					
POR/BOR	—	18.	Unexpected code execution at low V_{DD}.	X	X	X	X					
POR	—	19.	Premature POR release.	X	X	X	X					
POR	—	20.	POR may become stuck.	X	X	X	X					
Clocks	EC mode	21.	48 MHz maximum frequency.	X	X							
Comparators	Interrupt-on-Change	22.	Presetting interrupt-on-change issue.	X	X	X	X					
Data EEPROM Memory	Endurance	23.	Endurance is limited to 10K cycles.	X	X	X	X	X	X	X		
Program Flash Memory	Endurance	24.	Endurance is limited to 1K cycles.	X	X	X	X	X	X	X		
Configuration Bits	CONFIG3H	25.	HFOFST bit erases to '0' instead of '1'.	X	X	X	X					

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

2: Shaded cells in this table indicate older device revisions that are no longer in production.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)								
				A4	A7	A9	AB	A4	A7	A8	AE	AF
				0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
EUSART	Asynchronous Receive mode	26.	RCIDL bit may stay low improperly.	X	X	X	X					
PORTB Interrupts	Interrupt-on-Change	27.	False interrupt when setting interrupt enable.	X	X	X	X	X	X	X	X	X
ADC	ADC Conversion	28.	ADC conversion may be limited to half scale.	X	X	X	X	X	X	X		
ECCP	Full-Bridge mode	29.	Wrong dead-band time.	X	X	X	X	X	X	X	X	X
ECCP	Full-Bridge mode	30.	Wrong signal start time.	X	X	X	X	X	X	X	X	X
MSSP SPI	SPI Clock	31.	Improper SCK output.	X	X	X	X	X	X	X	X	X
MSSP SPI	SPI Master	32.	Improper sampling of last bit.	X	X	X	X	X	X	X	X	X
MSSP SPI	SPI Master	33.	Improper handling of write collision.	X	X	X	X	X	X	X	X	X
MSSP I^2C	I^2C Master	34.	Improper handling of Stop event.	X	X	X	X	X	X	X	X	X
EUSART	OERR Flag	35.	Clearing SPEN bit does not clear OERR flag.	X	X	X	X	X	X	X	X	X
EUSART	BAUDCTL	36.	RCIDL bit may stay low improperly.	X	X	X	X	X	X	X	X	X
PORTB Interrupts	Interrupt-on-Change	37.	False interrupt when waking from Sleep.	X	X	X	X	X	X	X	X	X
BOR	Reset	38.	Reset on configuring the analog comparators to the FVR.	X	X	X	X	X	X	X	X	X
Wake-up from Low-Power Sleep mode	Wake-up Sources	39.	Device may not wake-up under specific conditions.	X	X	X	X	X	X	X	X	X
Low-Voltage Detect	LVD in Sleep	40.	LVD erroneously triggers upon wake-up from Sleep if band gap is disabled in Sleep mode.	X	X	X	X	X	X	X	X	X
Timer1/3	Interrupt	41.	When the timer is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur.	X	X	X	X	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

2: Shaded cells in this table indicate older device revisions that are no longer in production.

Silicon Errata Issues

Note 1: This document summarizes all silicon errata issues from all specified revisions of silicon.

2: Shaded cells in this section indicate latest silicon in production.

1. Module: ECCP

Changing the CCP1M<3:0> bits of CCP1CON may cause the CCPR1H and CCPR1L registers to capture the value of Timer1.

Work around

Halt Timer1 before changing ECCP mode. Reload Timer1 with desired value after ECCP is setup and before Timer1 is restarted.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

2. Module: ECCP

Changing direction in Full-Bridge mode does not insert dead time between changing the active drivers in common legs of the bridge.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

3. Module: MSSP SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011), the first SPI high time may be short.

Work around

Option 1: Ensure TMR2 value rolls over to zero immediately before writing to SSPBUF.

Option 2: Turn Timer2 off and clear TMR2 before writing SSPBUF. Enable TMR2 after SSPBUF is written.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

4. Module: MSSP I^2C

Slew rate is slower than I^2C specifications when the SLRCON<2> bit is set.

Work around

Clear SLRCON<2> bit when using the I^2C peripheral.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

5. Module: ADC

Offset error is 3 LSb typical, 7 LSb maximum, including an acquisition time-dependent component (~2 LSb).

Work around

The time dependent error is insignificant when the time between conversions is less than 100 ms. When the time since the previous conversion is greater than 100 ms then take two ADC conversions and discard the first.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

6. Module: MSSP I^2C

If a new address byte is received while the BF flag is set, the SSPOV bit is properly set and an ACK is not properly generated. If only the SSPOV bit is set (BF flag was cleared) and a matching address is clocked in, that received byte will be improperly loaded into the SSPBUF register and an ACK will be improperly generated.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

7. Module: MSSP I²C

I²C Master mode is not functional (Rev. A4 only).

Work around

Use software to emulate Master mode.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X								

8. Module: MSSP SPI

In SPI Master mode, when the CKE bit is cleared and the SMP bit is set, the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

9. Module: MSSP SPI

In SPI Master mode, when CKE bit is set, the SSPBUF will reload the SSPSR output shift register on every high-to-low transition of the $\overline{SS}$ pin.

Work around

Avoid using the $\overline{SS}$ pin when the CKE bit is set and the MSSP is configured for SPI Master mode.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

10. Module: MSSP SPI

When SPI is enabled in Master mode with CKE = 1 and CKP = 0, a 1/FOSC wide pulse will occur on the SCK pin.

Work around

Configure SCK pin as an input until after the MSSP is setup.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

11. Module: EUSART

In Synchronous Master mode, when the SPBRG is set to an odd number, the duty cycle of the CK output will be skewed by one baud clock count.

Work around

High values of SPBRG will minimize the effect of this anomaly.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

12. Module: EUSART

In Synchronous Master mode, when the SPBRG is set to 3 and the TXREG is written while the previous character is still in the TX shift register, the LS bit of the TXREG character may be corrupted during transmission.

Work around

When SPBRG is set to 3, wait until the TRMT bit of the TXSTA register is set before loading TXREG with the next character to be transmitted.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

13. Module: EUSART

In Synchronous Master mode, if the SPBRG register is equal to 0 when the TXEN bit is set, then writing to TXREG will properly start transmission. However, the clock will be improperly out of phase with the data bits and the clock will not stop at the end of the character transmission.

Work around

Set SPBRG register to non-zero value before setting the TXEN bit.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

14. Module: Internal Fixed Voltage Reference (FVR)

The FVRST bit of the CVRCON2 register activates prematurely (Rev. A4 and A7 only).

Work around

Wait an additional 20 µs after FVRST is sensed high before using the fixed voltage reference. Enable the FVR by setting the FVREN bit of the CVRCON2 register before activating any peripheral that automatically enables the FVR. Peripherals that automatically enable the FVR include the Brown-out Reset, the High/Low-Voltage Detect, and the HFINTOSC.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X							

15. Module: High Low Voltage Detect (HLVD)

The IVRST bit of the HLVDCON register activates prematurely (Rev. A4 and A7 only).

Work around

Wait an additional 20 µs after IVRST is sensed high before using the fixed voltage reference. Enable the FVR by setting the FVREN bit of the CVRCON2 register before activating any peripheral that automatically enables the FVR. Peripherals that automatically enable the FVR include the Brown-out Reset, the High/Low-Voltage Detect, and the HFINTOSC.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X							

16. Module: BOR

An unexpected Brown-out Reset may occur when the fixed voltage reference is inactive and BOR is activated, thereby activating the fixed voltage reference simultaneously. This error is caused by a premature FVRST stable flag (Rev. A4 and A7 only) and only affects Brown-out disable in Sleep and software enabled BOR modes.

Work around

Enable the FVR by setting the FVREN bit of the CVRCON2 register and then wait an additional 20 µs after FVRST is sensed high before enabling BOR. Brown-out disable in Sleep mode with automatic enable on wake-up cannot be used.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X							

17. Module: System Clocks

HFINTOSC output frequency is 16 MHz ±3%, 25°C to 85°C.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

18. Module: POR/BOR

The POR rearm voltage may be below the low end of the BOR range, causing unexpected code execution below the BOR range.

Work around

Use external power monitor to hold the device in Reset below 1.1V.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

19. Module: POR

The POR may release around 0.8V (below the POR rearm voltage of 1.2V, nominal) when VDD rises from below 0.60V (when BOR is not enabled) or 0.33V (when BOR is enabled).

Work around

Use Power-up Timer when operating with the EC, EXTRC or HFINTOSC oscillator modes. Ensure that VDD rise time is less than the Power-up Timer time.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

20. Module: POR

The part may hang in the Reset state when VDD rises to the operating range at a rate faster than 7500V per second. Recovery from the hung state is possible only by first lowering VDD to below 0.3V, followed by raising VDD to the operating range.

Work around

Slow VDD rise time by adding series resistance between the voltage supply and the VDD pin and increasing the VDD bypass capacitance. VDD bypassing should remain on the pin side of the series resistor.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

21. Module: Clocks

EC mode operation is limited to a maximum of 48 MHz (Rev. A4 and A7 only).

Work around

Divide external clock by 4 and use HS-PLL Clock mode for external clocking above 48 MHz.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X							

22. Module: Comparators

When the CxON bit is clear, the output from the comparator will be properly forced to zero, but the CxPOL bit will improperly have no effect on the CxOUT bit. This prevents presetting the comparator change-on-interrupt mismatch latches as described in the data sheet.

Work around

Configure one of the unused comparator input channels as a digital output. Use that digital output to manipulate the comparator output to the desired CxOUT non-interrupt level. When the comparator is then set to the desired inputs, the mismatch latches will be preset to the non-interrupt level and the CxIF flag can then be cleared.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

23. Module: Data EEPROM Memory

The write/erase endurance of Data EE Memory is limited to 10K cycles.

Work around

Use error correction method that stores data in multiple locations.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X		

24. Module: Program Flash Memory

The write/erase endurance of the PFM is limited to 1K cycles when VDD is above 3V. Endurance degrades when VDD is below 3V.

Work around

For data tables in Program Flash Memory use error correction method that stores data in multiple locations.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X		

25. Module: Configuration Bits

Bit 3 of CONFIG3H defaults to '0' after a Bulk Erase instead of '1' as specified in the data sheet.

Work around

Program the HFOFST bit to the desired state after a Bulk Erase. All MPLAB® IDE programming tools currently perform this way.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

26. Module: EUSART

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when an invalid Start bit less than 1/8th of a bit time is received. The RCIDL bit will then stay low improperly until a valid Start bit is received.

Work around

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X					

27. Module: PORTB

Setting a PORTB interrupt-on-change enable bit of the IOCB register while the corresponding PORTB input is high will cause an RBIF interrupt.

Work around

Set the IOCB bits to the desired configuration, then read PORTB to clear the mismatch latches. Finally, clear the RBIF bit before setting the RBIE bit.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

28. Module: ADC

After extended stress, the Most Significant bit (MSb) of the ADC conversion result can become stuck at '0'. Conversions resulting in code 511 or less are still accurate, but conversions that should result in codes greater than 511 are, instead, pinned at 511.

The potential for failures is a function of several factors:

- The potential for failures increases over the life of the part. No failures have ever been seen for accelerated stress estimated to be equivalent to 34 years at room temperature. The failure rate after accelerated stress estimated to be equivalent to 146 years at room temperature can be as high as 10% for V_{DD} = 1.8V. The time to failure will decrease as the operating temperature increases.
- The potential for failures is highest at low V_{DD} and decreases as V_{DD} increases.

Work around

1. Restrict the input voltage to less than 1/2 of the ADC voltage reference so that the expected result is always a code less than or equal to 511.
2. Use manual acquisition time (ACQT<2:0> = 000) and put the part to Sleep after each conversion.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X		

29. Module: ECCP

Changing direction in Full-Bridge mode inserts a dead-band time of 4/FOSC * TMR2 Prescale instead of 1/FOSC * TMR2 Prescale as specified in the data sheet.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

30. Module: ECCP

ECCP – In Full-Bridge mode when PR2 = CCPR1L and DC1B[1:0] <>'00' and the direction is changed, then the dead time before the modulated output starts is compromised. The modulated signal improperly starts immediately with the direction change and stays on for TOSC * TMR2 Prescale * DC1B[1:0].

Work around

Avoid changing direction when the duty cycle is within three Least Significant steps of 100% duty cycle. Instead, clear the DC1B[1:0] bits before the direction change and then set them to the desired value after the direction change is complete.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

31. Module: MSSP SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011) and the CKE bit of the SSPSTAT register is '1', then when SSPBUF is written, the SCK output is improperly immediately driven to the non-Idle state together with the MSb value of the SSPBUF. The duration at which SDO and SCK remain at these levels may be shorter than a full half-bit period. The remaining bits in the byte are output properly.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

32. Module: MSSP SPI

In SPI Master mode, when the CKE bit of the SSPSTAT register is cleared and the SMP bit of the SSPSTAT register is set, then the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around

None.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

33. Module: MSSP SPI

In SPI Master mode, if the SSPBUF register is written while a byte is actively being transmitted, an extra clock pulse will be improperly generated at the end of the transmission. Further writes to the SSPBUF register will be inhibited although 8 or 9 clock pulses will be generated for each attempted write. The WCON bit of the SSPCON register is properly set indicating that a write collision occurred. However, the write collision condition can only be cleared by resetting the MSSP module. Clear the MSSP by clearing the SSPEN bit of the SSPCON1 register.

Work around

Use the SSPIF bit of the PIR1 register or the BF bit of the SSPSTAT register to determine that the transmission is complete before writing the SSPBUF register. In the event that a write collision does occur, use the slave select feature to resynchronize the slave clock.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

34. Module: MSSP I^2C

In Master I^2C Receive mode if a Stop condition occurs in the middle of an address or data reception, then the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain set improperly. If a Start condition occurs after the improper Stop condition then nine additional clocks will be generated followed by the RCEN bit going low.

Work around

Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches which may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition and resulting stuck RCEN bit. Clear the stuck RCEN bit by clearing the SSPEN bit of SSPCON1.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

35. Module: EUSART

The OERR flag of the RCSTA register is reset only by clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

Work around

Clear the OERR flag by clearing the CREN bit instead of clearing the SPEN bit.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

36. Module: EUSART

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when an invalid Start bit less than 1/16th of a bit time is received. The RCIDL bit will then properly go high 1/8th of a bit time later. However, if another invalid Start bit occurs less than 1 bit time after the leading edge of the first invalid Start bit, then the RCIDL bit will improperly stay high then improperly go low one bit time later. The RCIDL bit will then stay low improperly until a valid Start bit is received.

Work around

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

37. Module: Interrupt-on-Change

When any interrupt-on-change is enabled and the corresponding input is high, then waking from Sleep by a source other than interrupt-on-change may cause the RBIF interrupt flag bit to become set improperly.

Work around

1. Use the INTx interrupt in lieu of interrupt-on-change.

Or

2. Store the state of the PORTB inputs before entering Sleep. Upon waking, if an RBIF is detected, then compare the PORTB levels with those stored. If they are the same, then clear and ignore the RBIF interrupt.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

38. Module: BOR

An unexpected Brown-out Reset may occur when enabling the comparator with the Fixed Voltage Reference (FVR) selected as the V_{IN+} input.

Work around

Disconnect the FVR from the V_{IN+} comparator inputs prior to enabling the comparator and then reconnect it after enabling the comparator.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

39. Module: Wake-up from Low-Power Sleep mode

The device may not wake from Sleep when both of the following conditions are met:

1. The device is in Sleep mode for <1 ms;
2. On waking, the device executes a SLEEP instruction within 100 µs.

Under these conditions, the oscillator may stop before completing execution of the SLEEP instruction. The device will enter Sleep mode but will not wake-up on any enabled wake-up event, including the Watchdog Timer.

Work around

1. Disable High-Speed Start-up

Disabling High-Speed Start-up in the Configuration Word will delay the device executing code on wake-up by 250 µs, nominally, allowing the oscillator to stabilize.

The wake-up time from Sleep will increase by about 250 µs, nominally.

2. BOR enabled during Sleep

Configuring the device for hardware only BOR or software-controlled BOR and enabling SBOREN, the voltage reference is on during Sleep.

The device will wake-up and the oscillator will be stable. This will add 20 µA (nominal) to the Sleep current.

3. Enable the FVR during Sleep

In the same manner as the BOR, the FVR will keep the voltage reference on during Sleep, causing the oscillator to be stable on wake-up.

4. Avoid executing SLEEP within 100 µs of any wake-up event

This can be achieved by adding more instructions (NOP) before executing the SLEEP instruction. This minimizes the probability of the SLEEP instruction only partially executing.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

40. Module: Low-Voltage Detect

If Low-Voltage Detect is enabled, the band gap is disabled in Sleep, and the part is put to Sleep for a short period of time, the LVD will trigger immediately upon waking-up from Sleep.

Work around

Do not disable the band gap in Sleep when using the LVD.

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

41. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to 0x0000 when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 1.

EXAMPLE 1: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;         //Stop timer from incrementing
PIE1bits.TMR1IE = 0;          //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                 //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;         //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);          //Wait for 2 timer increments more than the Updated Timer
                              //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                        //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;          //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;          //Now re-enable interrupt vectoring for timer 1
```

Affected Silicon Revisions

0xA	0xC	0xE	0x11	0x16	0x18	0x19	0x1B	0x1C
X	X	X	X	X	X	X	X	X

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41303**H**):

Note:	Corrections are shown in **bold.** Where possible, the original bold text formatting has been removed for clarity.

1. Module: Product Identification System

The temperature range values have been corrected.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX	XXX
Device	Tape and Reel Option	Temperature Range	Package	Pattern

Device:	PIC18F24K20; PIC18F25K20; PIC18F44K20; PIC18F26K20; PIC18F45K20; PIC18F44K20; PIC18F45K20; PIC18F46K20.	
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel(1)	
Temperature Range:	**I = -40°C to +85°C (Industrial)** **E = -40°C to +125°C (Extended)**	
Package:	PT = TQFP (Thin Quad Flatpack) SS = SSOP SO = SOIC SP = SPDIP (Skinny Plastic DIP) P = PDIP ML = QFN MV = UQFN	
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC18F45K20 - E/P 301 = Industrial temp., PDIP package, QTP pattern #301.

b) PIC18F24K20 - I/SO = Industrial temp., SOIC package.

c) PIC18F44K20 - E/P = Extended temp., PDIP package.

d) PIC18F46K20 - I/PT = Industrial temp., TQFP package, tape and reel.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2008)

Initial release of this document.

Rev B Document (05/2009)

Updated Errata to new format; Added Module 11: PORTB and Module 12: ADC; minor edits.

Clarifications/Corrections to the Data Sheet: Added Module 1: MSSP; Module 2: Electrical Specifications; Module 3: Electrical Specifications.

Rev C Document (06/2009)

Clarifications/Corrections to the Data Sheet:

Deleted Module 1: MSSP: Figure 17-17 Baud Rate Generator Block Diagram, updating subsequent numbering. Added Module 3 MSSP: Register 17-3 SSPADD; Added Module 4 MSSP: Section 17.4.2 Operation; Added Module 5 MSSP: Figure 17-16 MSSP Block Diagram; Added Module 6 MSSP: Sections 17.4.7.1, 17.4.8, 17.4.9, 17.4.17.1, 17.4.17.2, 17.4.17.3: SSPADD, changing <6:0> to <7:0>.

Rev D Document (11/2009)

Updated to add revision 0x1B.

Data Sheet Clarifications: Deleted Modules 1, 2, 3, 4, 5, 6.

Rev E Document (04/2010)

Updated to include early revisions of silicon, revision IDs 0xA through 0x11. These early revisions were described in DS80366 errata, which is now obsolete.

Rev F Document (05/2010)

Updated Table 1.

Rev G Document (07/2010)

Removed ADC Work around #2 and changed #3 to #2 (Module 28).

Rev H Document (07/2011)

Updated errata to the new format; Updated Module 16; Added Modules 38 and 39; Updated Table 2 to include the new modules.

Data Sheet Clarifications: Added Module 1.

Rev J Document (07/2012)

Added Silicon revision AF.

Rev K Document (05/2013)

Added MPLAB X IDE; Added Module 40, Low-Voltage Detect.

Data Sheet Clarifications: Added Module 2, Electrical Characteristics.

Rev L Document (12/2013)

Data Sheet Clarification: Updated Module 2 (Electrical Characteristics, Table 26-8).

Rev M Document (4/2014)

Data Sheet Clarifications: Added Modules 3, 4, 5, 6, 7, 8.

Rev N Document (7/2014)

Added Module 41, Timer1/3 to Silicon Errata Issues section.

Rev P Document (9/2015)

Data Sheet Clarifications:

Removed modules 1-8. Added Module 1, Product Identification System.

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