

**MICROCHIP****PIC18F2420/2520/4420/4520****PIC18F2420/2520/4420/4520 Rev. B2 Silicon Errata**

The PIC18F2420/2520/4420/4520 Rev. B2 parts you have received conform functionally to the Device Data Sheet (DS39631C), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2420/2520/4420/4520 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2420/2520/4420/4520 devices with these Device/Revision IDs:

| Part Number | Device ID     | Revision ID |
|-------------|---------------|-------------|
| PIC18F2420  | 0001 0001 010 | 0 0101      |
| PIC18F2520  | 0001 0001 000 | 0 0101      |
| PIC18F4420  | 0001 0000 110 | 0 0101      |
| PIC18F4520  | 0001 0000 100 | 0 0101      |

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

**1. Module: MSSP**

In SPI Slave mode with slave select enabled (SSPM<3:0> = 0100), the minimum time between the falling edge of the  $\overline{SS}$  pin and first SCK edge is greater than specified in parameter 70 in Table 26-16 and Table 26-17. The updated specification is shown in bold in Table 1.

The minimum time between the  $\overline{SS}$  pin low and an SSPBUF write is also 3 Tcy. If the falling edge of the  $\overline{SS}$  pin occurs greater than 3 Tcy before the first SCK edge, or loading SSPBUF, the peripheral will function correctly. Also, if SSPBUF is written prior to the  $\overline{SS}$  pin going low, the peripheral will function correctly.

**Work around**

None.

**Date Codes that pertain to this issue:**

All engineering and production devices.

**TABLE 1: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING)**

| Param No. | Symbol             | Characteristic                                                         | Min          | Max | Units | Conditions |
|-----------|--------------------|------------------------------------------------------------------------|--------------|-----|-------|------------|
| 70        | TssL2sch, TssL2scL | $\overline{SS} \downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ Input | <b>3 Tcy</b> | —   | ns    |            |

# PIC18F2420/2520/4420/4520

## 2. Module: MSSP

With MSSP in SPI Master mode,  $F_{osc}/64$  or Timer2/2 clock rate, and  $CKE = 0$ , a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur, as indicated by the WCOL bit being set.

### Work around

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 3. Module: Timer1 and Timer3

For Timer1 or Timer3, if the TMRxH and TMRxL registers are written to in consecutive instruction cycles, the timer may not be updated with the correct value when configured for externally clocked 8-Bit Asynchronous mode ( $T1CON<7:0>$  or  $T3CON<7:0> = 0xxx\ x111$ ).

### Work around

Insert a delay of one or more instruction cycles between writes to TMRxH and TMRxL. This delay can be a `NOB`, or any instruction that does not access the Timer registers (Example 1).

### EXAMPLE 1:

```
CLRF    TMR1H
MOVLW   T1Offset ; 1 Tcy delay
MOVWF   TMR1L
```

### Date Codes that pertain to this issue:

All engineering and production devices.

## 4. Module: ECCP (PWM Mode)

**Note:** The ECCP module is implemented only in 40/44-pin devices.

When configured for half-bridge operation with dead band ( $CCPxCON<7:6> = 10$ ), the PWM output may be corrupted for certain values of the PWM duty cycle. This occurs when these additional criteria are also met:

- a non-zero, dead-band delay is specified ( $PDC6:PDC0 > 0$ ); and
- the duty cycle has a value of 0 through 3, or  $4n + 3$  ( $n \geq 1$ ).

### Work around

None.

### Date Codes that pertain to this issue:

All engineering and production devices.

## 5. Module: Power-up Timer

The Power-up Timer (PWRT) may not function as expected during a Power-on Reset (POR) when the Brown-out Reset (BOR) is disabled.

### Work around

Use either of the following work arounds:

- Enable the BOR using any desired mode and setpoint.
- If BOR operation is not desired:
  - Configure the BOR using  $BOREN<1:0> = 01$  ( $CONFIG2L<2:1>$ ) – BOR controlled by SBOREN.
  - Configure the BOR for the lowest voltage setpoint by clearing the  $BORV<1:0>$  bits ( $CONFIG2L<4:3>$ ).

In this configuration, the SBOREN bit resets to '1', enabling the BOR.

- When code execution begins following all Resets, disable the BOR by clearing the SBOREN bit ( $RCON<6>$ ).

### Date Codes that pertain to this issue:

All engineering and production devices.

## 6. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

One bit has been added to the BAUDCON register and one bit has been renamed. The added bit is RXDTP and is in the location, BAUDCON<5>. The renamed bit is the TXCKP bit (BAUDCON<4>), which had been named SCKP.

The TXCKP (BAUDCON<4>) and RXDTP (BAUDCON<5>) bits enable the Synchronous mode TX and RX signals to be inverted (polarity reversed). RXDTP has no effect on the Synchronous mode DT signal.

Register 18-3, on page 204, will be changed as shown.

### Work around

None required.

### Date Codes that pertain to this issue:

All engineering and production devices.

## REGISTER 18-3: BAUDCON: BAUD RATE CONTROL REGISTER

| R/W-0  | R-1   | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|--------|-------|-------|-------|-------|-----|-------|-------|
| ABDOVF | RCIDL | RXDTP | TXCKP | BRG16 | —   | WUE   | ABDEN |
| bit 7  |       |       |       |       |     |       | bit 0 |

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit, read as '0'  
'0' = Bit is cleared  
x = Bit is unknown

- bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit  
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)  
0 = No BRG rollover has occurred
- bit 6 **RCIDL**: Receive Operation Idle Status bit  
1 = Receive operation is Idle  
0 = Receive operation is Active
- bit 5 **RXDTP**: Receive Data Polarity Select bit (Asynchronous mode only)  
Asynchronous mode:  
1 = Receive data (RX) is inverted. Idle state is a low level.  
0 = No inversion of receive data (RX). Idle state is a high level.
- bit 4 **TXCKP**: Transmit/Clock Polarity Select bit  
Asynchronous mode:  
1 = Transmit data (TX) is inverted. Idle state is a low level.  
0 = No inversion of transmit data (TX). Idle state is a high level.  
Synchronous mode:  
1 = Idle state for clock (CK) is a high level  
0 = Idle state for clock (CK) is a low level
- bit 3 **BRG16**: 16-bit Baud Rate Register Enable bit  
1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG  
0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode); SPBRGH value ignored
- bit 2 **Unimplemented**: Read as '0'
- bit 1 **WUE**: Wake-up Enable bit  
Asynchronous mode:  
1 = EUSART will continue to sample the RX pin with the interrupt generated on the falling edge; bit cleared in hardware on following rising edge  
0 = RX pin is not monitored or rising edge detected  
Synchronous mode:  
Unused in this mode.

# PIC18F2420/2520/4420/4520

## REGISTER 18-3: BAUDCON: BAUD RATE CONTROL REGISTER (CONTINUED)

bit 0      **ABDEN**: Auto-Baud Detect Enable bit  
Asynchronous mode:  
1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.  
0 = Baud rate measurement disabled or completed  
Synchronous mode:  
Unused in this mode.

### 7. Module: 10-Bit Analog-to-Digital Converter

When the AD clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

#### Work around

Select the AD clock source as 4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC or 64 TOSC and avoid selecting 2 TOSC or RC.

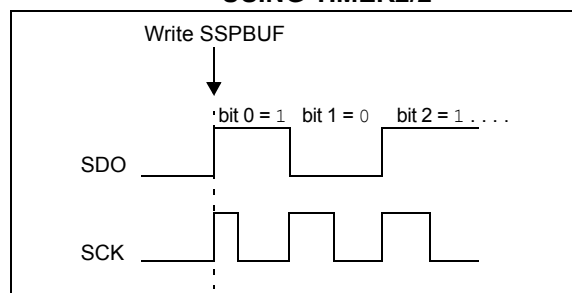
#### Date Codes that pertain to this issue:

All engineering and production devices.

### 8. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

**FIGURE 1: SCK PULSE VARIATION USING TIMER2/2**



#### Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 2 for sample code.

### EXAMPLE 2: AVOIDING THE INITIAL SHORT SCK PULSE

```
LOOP BTFSS SSPSTAT, BF    ;Data received?
                                ; (Xmit complete?)
    BRA     LOOP            ;No
    MOVF    SSPBUF, W        ;W = SSPBUF
    MOVWF   RXDATA          ;Save in user RAM
    MOVF    TXDATA, W        ;W = TXDATA
    BCF     T2CON, TMR2ON    ;Timer2 off
    CLRF    TMR2            ;Clear Timer2
    MOVWF   SSPBUF          ;Xmit New data
    BSF     T2CON, TMR2ON    ;Timer2 on
```

#### Date Codes that pertain to this issue:

All engineering and production devices.

## REVISION HISTORY

### Rev A Document (08/2006)

First revision of this document. Silicon issues 1-2 (MSSP).

### Rev B Document (10/2006)

Added silicon issue 3 (Timer1 and Timer3).

### Rev C Document (11/2006)

Updated silicon issue 3 (Timer1 and Timer3) and added silicon issue 4 (ECCP – PWM Mode).

### Rev D Document (1/2007)

Added silicon issue 5 (Power-up Timer).

### Rev E Document (4/2007)

Added silicon issue 6 (Enhanced Universal Synchronous Receiver Transmitter – EUSART).

### Rev F Document (6/2007)

Added silicon issue 7 (10-Bit Analog-to-Digital Converter) and 8 (MSSP – SPI Mode).

### Rev G Document (8/2007)

Modified silicon issue 6 (EUSART).

# PIC18F2420/2520/4420/4520

---

NOTES:

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, KEELOQ logo, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, rPIC and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AmpLab, FilterLab, Linear Active Thermistor, Migratable Memory, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rLAB, Select Mode, Smart Serial, SmartTel, Total Endurance, UNI/O, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2007, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949:2002 ==**

*Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*



---

## WORLDWIDE SALES AND SERVICE

---

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://support.microchip.com>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

#### Atlanta

Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

#### Boston

Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

#### Chicago

Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Dallas

Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

#### Kokomo

Kokomo, IN  
Tel: 765-864-8360  
Fax: 765-864-8387

#### Los Angeles

Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

#### Santa Clara

Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

#### Toronto

Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

#### Asia Pacific Office

Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

#### Australia - Sydney

Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

#### China - Beijing

Tel: 86-10-8528-2100  
Fax: 86-10-8528-2104

#### China - Chengdu

Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

#### China - Fuzhou

Tel: 86-591-8750-3506  
Fax: 86-591-8750-3521

#### China - Hong Kong SAR

Tel: 852-2401-1200  
Fax: 852-2401-3431

#### China - Qingdao

Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

#### China - Shanghai

Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

#### China - Shenyang

Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

#### China - Shenzhen

Tel: 86-755-8203-2660  
Fax: 86-755-8203-1760

#### China - Shunde

Tel: 86-757-2839-5507  
Fax: 86-757-2839-5571

#### China - Wuhan

Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

#### China - Xian

Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

### ASIA/PACIFIC

#### India - Bangalore

Tel: 91-80-4182-8400  
Fax: 91-80-4182-8422

#### India - New Delhi

Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

#### India - Pune

Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

#### Japan - Yokohama

Tel: 81-45-471-6166  
Fax: 81-45-471-6122

#### Korea - Daegu

Tel: 82-53-744-4301  
Fax: 82-53-744-4302

#### Korea - Seoul

Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

#### Malaysia - Penang

Tel: 60-4-646-8870  
Fax: 60-4-646-5086

#### Philippines - Manila

Tel: 63-2-634-9065  
Fax: 63-2-634-9069

#### Singapore

Tel: 65-6334-8870  
Fax: 65-6334-8850

#### Taiwan - Hsin Chu

Tel: 886-3-572-9526  
Fax: 886-3-572-6459

#### Taiwan - Kaohsiung

Tel: 886-7-536-4818  
Fax: 886-7-536-4803

#### Taiwan - Taipei

Tel: 886-2-2500-6610  
Fax: 886-2-2508-0102

#### Thailand - Bangkok

Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

#### Austria - Wels

Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

#### Denmark - Copenhagen

Tel: 45-4450-2828  
Fax: 45-4485-2829

#### France - Paris

Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

#### Germany - Munich

Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

#### Italy - Milan

Tel: 39-0331-742611  
Fax: 39-0331-466781

#### Netherlands - Drunen

Tel: 31-416-690399  
Fax: 31-416-690340

#### Spain - Madrid

Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

#### UK - Wokingham

Tel: 44-118-921-5869  
Fax: 44-118-921-5820