



MICROCHIP

PIC18F2682/2685/4682/4685

PIC18F2682/2685/4682/4685 Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39761B), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F2682/2685/4682/4685 will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Master Synchronous Serial Port (MSSP)

The following note is added to the end of **Section 17.3.3 "Enabling SPI I/O"**.

Note:	When the module is enabled and in Master mode (CKE, SSPSTAT<6> = 1), a small glitch of approximately half a T_{CY} may be seen on the SCK pin. To resolve this, keep the SCK pin as an input while setting SPEN. Then, configure the SCK pin as an output (TRISC<3> = 0).
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PIC18F2682/2685/4682/4685

REVISION HISTORY

Rev A Document (1/2008)

Initial release of this data sheet errata. Includes
Data Sheet Clarification 1 (Master Synchronous
Serial Port – MSSP).

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