PIC18C658/858

PIC18C658/858 Rev. C3 Silicon/Data Sheet Errata

The PIC18C658/858 parts you have received conform functionally to the Device Data Sheet (DS30475**A**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC18C658/858 silicon.

1. Module: CAN

The CAN module may send a passive error flag earlier than expected. This will occur at the transition point of error active to error passive, TEC (Transmit Error Count), or REC (Receive Error Count) ≥ 128.

Work around

None for current silicon revision. Use the latest silicon revision when it becomes available.

2. Module: CAN

The CAN module may not synchronize correctly if there is a phase error between nodes that is equal to the Synchronization Jump Width (SJW). As a result, the module may request retransmission of messages from the transmitting node.

Work around

1. Use the longest SJW possible that will work with the application.
2. Use the latest silicon revision when it becomes available.

Date Codes that pertain to this issue:

ALL

Note: When the manufacture date of a newer version of silicon is in production, the last date where this issue may occur will be specified.

3. Module: LVD

The minimum and maximum LVD voltage levels (parameter D420) have changed. The new values are shown in Table 1.

Work around

None

Date Codes that pertain to this issue:

ALL

Note: When the manufacture date of a newer version of silicon is in production, the last date where this issue may occur will be specified.

TABLE 1: LVD MINIMUM VOLTAGES

Param No.	Symbol	Characteristic		Min.	Max.	Units
D420	VLVD	LVD Voltage	LVDL<3:0> = 0100	2.35	2.80	V
			LVDL<3:0> = 0101	2.55	3.02	V
			LVDL<3:0> = 0110	2.64	3.14	V
			LVDL<3:0> = 0111	2.83	3.37	V
			LVDL<3:0> = 1000	3.11	3.71	V
			LVDL<3:0> = 1001	3.29	3.93	V
			LVDL<3:0> = 1010	3.39	4.04	V
			LVDL<3:0> = 1011	3.58	4.26	V
			LVDL<3:0> = 1100	3.77	4.49	V
			LVDL<3:0> = 1101	3.95	4.71	V
			LVDL<3:0> = 1110	4.23	5.05	V

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4. Module: BOR

The minimum and maximum BOR Voltage levels (parameter D005) have changed. The new values are shown in Table 2 (below).

Work around

None.

Date Codes that pertain to this issue:

ALL

Note:	When the manufacture date of a newer version of silicon is in production, the last date where this issue may occur will be specified.

5. Module: Watchdog Timer

After the WDT is allowed to time-out, all subsequent WDT periods following the very first, may double in duration. This can occur if the CLRWDT instruction is not executed prior to the timer timing out.

Work around

Always execute the CLRWDT instruction prior to entering a potential WDT time-out condition.

6. Module: CAN

Two of the Receive Buffer modes defined by bits RXM1 and RXM0 of the RXB0CON register (RXB0CON<6:5>), are currently reversed from their description in the original Device Data Sheet (DS30475**A**). The actual values for these bits are shown in the excerpt from Register 17-12 (below) (changes from the original data sheet in **bold**).

This anomaly is particular to this silicon revision. Future revisions will restore the operation of these bits to their original description in the Device Data Sheet (DS30475**A)**.

Work around

1. Always configure the mode for Receive Buffer 0 as 'Receive All Valid Messages' (bits RXM1:RXM0 = 00). In addition, use the EXIDEN bit of the RXF0SIDL register (RXF0SIDL<3>) to set the filter for standard or extended ID messages. Set EXIDEN (= 1) for extended ID messages, and clear EXIDEN for standard ID messages.
2. Use the latest silicon revision when it becomes available.

TABLE 2: BOR MAXIMUM VOLTAGES

Param No.	Symbol	Characteristic		Min.	Max.	Units
D005	VBOR	BOR Voltage	BORV<1:0> = 11	2.35	2.80	V
			BORV<1:0> = 10	2.55	3.02	V
			BORV<1:0> = 01	3.95	4.71	V
			BORV<1:0> = 00	4.23	5.05	V

REGISTER 17-12: RXB0CON - RECEIVE BUFFER 0 CONTROL REGISTER

bit 6-5 **RXM1:RXM0:** Receive Buffer Mode bits
11 = Receive all messages (including those with errors)
10 = Receive only valid messages with standard identifier
01 = Receive only valid messages with extended identifier
00 = Receive all valid messages

7. Module: WDT

When the device is configured for either EC or RC Oscillator modes, with the Power-up Timer enabled, bit $\overline{TO}$ of the RCON register (RCON<3>) may default to '0', even though no WDT time-out has occurred.

The $\overline{TO}$ bit functions normally in all other configurations.

Work around

1. Use bit $\overline{TO}$ in conjunction with bit $\overline{POR}$ (RCON<1>), to determine if a RESET condition has occurred.
2. Use the latest silicon revision when it becomes available.

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8. Module: I/O (Parallel Slave Port)

The Input Buffer Status bit of the PSPCON register (PSPCON<7>) may be inadvertently cleared, even when the PORTD input buffer has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = 1111), and
- Any instruction that contains 83h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh. In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the Access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select Banks 1 through 5 and the upper half of Bank 0.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contains 83h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

9. Module: Interrupts

High priority interrupts may become improperly enabled, while low priority interrupts become improperly disabled at the same time. This may occur when low priority interrupts are in an enabled state and the following conditions occur simultaneously:

- High priority interrupts are being changed from an enabled to a disabled state; and
- One or more low priority interrupts occur.

Work around

1. Always disable low priority interrupts before disabling high priority interrupts. Re-enable the low priority interrupts afterwards, if necessary.
2. Use the latest silicon revision when it becomes available.

10. Module: I/O (PORTB Interrupt-on-Change)

The RB Port Change Flag bit of the INTCON register (RBIF, INTCON<0>) may be inadvertently cleared, even when the PORTB<7:4> pins have not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = 1111), and
- Any instruction that contains 81h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh. In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the Access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select Banks 1 through 5, and the upper half of Bank 0.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain 81h in the 8 Least Significant bits, while the BSR points to Bank 15 (BSR = 0Fh).

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11. Module: Interrupts

When an interrupt occurs simultaneously with the clearing of one or more interrupt enable flags in the INTCON, PIE1 or PIE2 registers, the instruction immediately following the interrupted instruction may be executed before vectoring to the Interrupt Service Routine (ISR). If that instruction is a control operation, the ISR may not execute as intended.

In the case of conditional branch instructions, the first instruction of the ISR may be skipped if the tested condition would have resulted in a branch.

In the case of `GOTO`, `CALL`, or `BRA` instructions, program execution may vector to the address encoded in the instruction; the ISR will not be executed at all. The GIE bit will still be cleared, disabling all interrupts.

Additionally, on return from the interrupt (by executing `RETFIE`), the instruction following the interrupted instruction may be executed again.

There may be other interrupt related symptoms.

Work around

Three possible solutions are presented here. Other solutions may exist. None of these require special attention when setting interrupt enable bits.

1. All instructions that clear interrupt enable bits should be followed by a `NOP` instruction.
2. Prior to disabling any interrupt source, disable all interrupts by clearing the GIE bit (INTCON<7>). After disabling the desired interrupts, re-enable all interrupts by setting GIE.
3. If interrupt priority is being used:
   a) clear both GIEL and GIEH (in order) bits (INTCON<7:6>) to disable all peripheral interrupts
   b) clear the desired interrupt enable bits
   c) set both GIEH and GIEL, in order to re-enable peripheral interrupts

12. Module: CAN Module

Under certain circumstances, the module may transmit unexpected messages. This will only happen when all of the following conditions occur simultaneously:

1. The identifier registers for Transmit buffer TXB0 are never used or written to;
2. Either of the transmit buffers, TXB1 or TXB2, are in use; and
3. The CAN module attempts to retransmit a message that has lost one or more previous arbitrations.

Work around

Clear the TXB0SIDL and TXB0SIDH registers as part of the CAN initialization routine.

13. Module: A/D (External Voltage Reference) and Comparator Voltage Reference

When the external voltage reference, V_{REF-}, is selected for use with either the A/D or comparator voltage reference, AV_{SS} is connected to V_{REF-} in the comparator module. If V_{REF-} is a voltage other than AV_{SS} (which must be tied externally to V_{SS}), excessive current will flow into the V_{REF-} pin.

Work around

If external V_{REF-} is used with a voltage other than 0V, enable the comparator voltage reference by setting the CVREN bit in the CVRCON register. This disconnects V_{REF-} and AV_{SS} within the comparator module.

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Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30475**A**), the following clarifications and corrections should be noted.

1. Module: Timer1

Section 11.1 (Timer1 Operation) is amended with the following clarification:

When Timer1 is configured to operate as an asynchronous counter, care must be taken that there is no incoming pulse while the module is being turned off. If an incoming pulse arrives while Timer1 is being turned off, the value of register TMR1 may become unpredictable.

If an application requires that Timer1 be turned off and if it is possible that Timer1 may receive an incoming pulse while being turned off, synchronize the external clock first, by clearing the T1SYNC bit of register T1CON. Please note that this may cause Timer1 to miss up to one count.

2. Module: LVD

Table 25-1 of the Device Data Sheet is amended to include parameters D421, D422, D423 and D425, related to the performance of the Low Voltage Detect module.

In addition, the minimum and maximum LVD voltage levels (specification D420) are also amended (see Issue 3 of this Errata), and typical voltage levels are provided.

Table 25-1 should read as follows (changes and additions in **bold**):

TABLE 25-1: LOW VOLTAGE DETECT CHARACTERISTICS

				Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**		**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
D420	VLVD	LVD Voltage	LVDL<3:0> = 0100	**2.35**	**2.58**	2.80	V	
			LVDL<3:0> = 0101	**2.55**	**2.78**	3.02	V	
			LVDL<3:0> = 0110	**2.64**	**2.89**	3.14	V	
			LVDL<3:0> = 0111	**2.83**	**3.1**	3.37	V	
			LVDL<3:0> = 1000	**3.11**	**3.41**	3.71	V	
			LVDL<3:0> = 1001	**3.29**	**3.61**	3.93	V	
			LVDL<3:0> = 1010	**3.39**	**3.72**	4.04	V	
			LVDL<3:0> = 1011	**3.58**	**3.92**	4.26	V	
			LVDL<3:0> = 1100	**3.77**	**4.13**	4.49	V	
			LVDL<3:0> = 1101	**3.95**	**4.33**	4.71	V	
			LVDL<3:0> = 1110	**4.23**	**4.64**	5.05	V	
D421	**ΔILVD**	**Supply Current**		**—**	**35**	**50**	**μA**	
D425	**VBG**	**Internally Generated Reference Voltage**		**TBD**	**1.22**	**TBD**	**V**	

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3. Module: BOR

The minimum and maximum specified values for parameter D005, as listed in Section 25.1 of the Device Data Sheet, are amended as noted (see also Issue 4 of this Errata).

Also, the typical and maximum values for parameter D022A are amended, as noted (see Issue 4 of this Errata).

Section 25.1 in part should read as follows (changes and additions in **bold**):

25.1 DC Characteristics

PIC18LCXX8 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18CXX8 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic/ Device**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D005	VBOR	**Brown-out Reset Voltage**					
		PIC18LCXX8 BORV1:BORV0 = 11	**2.35**	—	**2.80**	V	
		BORV1:BORV0 = 10	**2.55**	—	**3.02**	V	
		BORV1:BORV0 = 01	**3.95**	—	**4.71**	V	
		BORV1:BORV0 = 00	**4.23**	—	**5.05**	V	
D005		PIC18CXX8 BORV1:BORV0 = 1x	N.A.	N.A.	N.A.	V	Not in operating voltage range of device
		BORV1:BORV0 = 01	3.95	—	**4.71**	V	
		BORV1:BORV0 = 00	4.23	—	**5.05**	V	
D022A	ΔIBOR	PIC18LCXX8	—	**10**	**TBD**	µA	VDD = 5.5V
		Brown-out Reset	—	**10**	TBD	µA	VDD = 2.5V, 25°C
D022A		PIC18CXX8	—	**10**	**TBD**	µA	VDD = 5.5V, -40°C to +85°C
		Brown-out Reset	—	**10**	TBD	µA	VDD = 5.5V, -40°C to +125°
			—	**10**	TBD	µA	VDD = 4.2V, 25°C

Legend: Shading added to differentiate characteristics for “LC” devices. Characteristics are assumed to be common for “C” and “LC” devices unless otherwise noted.

* These parameters are characterized but not tested.

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4. Module: Comparator

Section 25.1 of the Device Data Sheet is amended to add parameter D023 related to the Analog Comparator module.

In addition, a new table is added to describe the Analog Comparator specifications.

Section 25.1 in part should read as follows (changes and additions in **bold**):

25.1 DC Characteristics (cont'd)

PIC18LCXX8 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18CXX8 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic/ Device**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D020	IPD	**Power-down Current(3)**					
		PIC18LCXX8	—	<2.5	5	µA	VDD = 2.5V, -40°C to +85°C
			—	—	36	µA	VDD = 5.5V, -40°C to +85°C
			—	—	TBD	µA	VDD = 2.5V, 25°C
D020		PIC18CXX8	—	<1	TBD	µA	VDD = 4.2V, -40°C to +85°C
			—	—	36	µA	VDD = 5.5V, -40°C to +85°C
D020A			—	—	TBD	µA	VDD = 4.2V, 25°C
D021B			—	TBD	TBD	µA	VDD = 4.2V, -40°C to +125°C
			—	—	42		VDD = 5.5V, -40°C to +125°C
D022	ΔIWDT	**Module Differential Current**					
		PIC18LCXX8	—	—	12	µA	VDD = 2.5V
		Watchdog Timer	—	—	25	µA	VDD = 5.5V
			—	—	TBD	µA	VDD = 2.5V, 25°C
D022		PIC18CXX8	—	—	25	µA	VDD = 5.5V, -40°C to +85°C
		Watchdog Timer	—	—	TBD	µA	VDD = 5.5V, -40°C to +125°C
			—	—	TBD	µA	VDD = 4.2V, 25°C
D022A	ΔIBOR	PIC18LCXX8	—	—	50	µA	VDD = 5.5V
		Brown-out Reset	—		TBD	µA	VDD = 2.5V, 25°C
D022A		PIC18CXX8	—	—	50	µA	VDD = 5.5V, -40°C to +85°C
		Brown-out Reset	—	—	TBD	µA	VDD = 5.5V, -40°C to +125°
			—	—	TBD	µA	VDD = 4.2V, 25°C
D022B	ΔILVD	PIC18LCXX8	—	—	50	µA	VDD = 2.5V
		Low Voltage Detect	—	—	TBD	µA	VDD = 2.5V, 25°C
D022B		PIC18CXX8	—	—	TBD	µA	VDD = 4.2V, -40°C to +85°C
		Low Voltage Detect	—	—	TBD	µA	VDD = 4.2V, -40°C to +125°C
			—	—	TBD	µA	VDD = 4.2V, 25°C

Legend: Rows are shaded for improved readability.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode, or during a device RESET, without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD
MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS, and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, ...).

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.

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25.1 DC Characteristics (cont'd)

PIC18LCXX8 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18CXX8 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic/ Device**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D023	**ΔICOMP**	**PIC18LCXX8 Comparator**	**—**	**—**	**100**	**μA**	**VDD = 2.5V**
D023		PIC18CXX8 Comparator	—	—	100	μA	VDD = 4.2V
D023A	ΔIVREF	PIC18LCXX8 Voltage Reference	—	—	300	μA	VDD = 2.5V
D023A		PIC18CXX8 Voltage Reference	—	—	300	μA	VDD = 4.2V
D025	ΔIOSCB	PIC18LCXX8 Timer1 Oscillator	— —	— —	3 TBD	μA μA	VDD = 2.5V VDD = 2.5V, 25°C
D025		PIC18CXX8 Timer1 Oscillator	— — —	— — —	TBD TBD TBD	μA μA μA	VDD = 4.2V, -40°C to +85°C VDD = 4.2V, -40°C to +125°C VDD = 4.2V, 25°C

Legend: Rows are shaded for improved readability.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode, or during a device RESET, without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD
MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS, and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, ...).

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.

TABLE 1: COMPARATOR SPECIFICATIONS

	Operating conditions: VDD range as described in Table 1 Operating temperature -40°C < TA < +125°C Current consumption is specified in Table 1				
Characteristics	**Min.**	**Typ**	**Max**	**Units**	**Comments**
Input Offset Voltage		±5.0	±10	mV	
Input Common Mode Voltage	0		VDD – 1.5	V	
CMRR	+55			db	
Response Time(1)		150	400 600	ns ns	PIC18CXX8 PIC18LCXX8
Comparator Mode Change to Output Valid			10	μs	

Note 1: Response time measured with one comparator at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

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5. Module: Interrupts

The operation of the GIE/GIEH bit (INTCON<7>) is clarified as follows: when the bit is cleared, all interrupts are disabled. This is regardless of the state of the IPEN bit (RCON<7>), the priority of the interrupt, or whether or not the interrupt is unmasked. This varies from the original description, in which clearing the bit when IPEN = 1 would only disable high priority interrupts.

The seventh paragraph in Section 7.0 of the Device Data Sheet (beginning "When an interrupt is responded to....") is amended by adding the following sentence to the end:

"It is important to note, however, that clearing the GIE/GIEH bit, regardless of the state of the IPEN bit, will disable **all** interrupts."

The changes to the bit descriptions in Register 7-1 in the Device Data Sheet are shown in the excerpt below (changes in **bold**).

Also, the interrupt logic funnel shown in Figure 7-1 of the Device Data Sheet is amended with the addition of a GIE/GIEH control line, as shown in Figure 1 (new material in **bold line**).

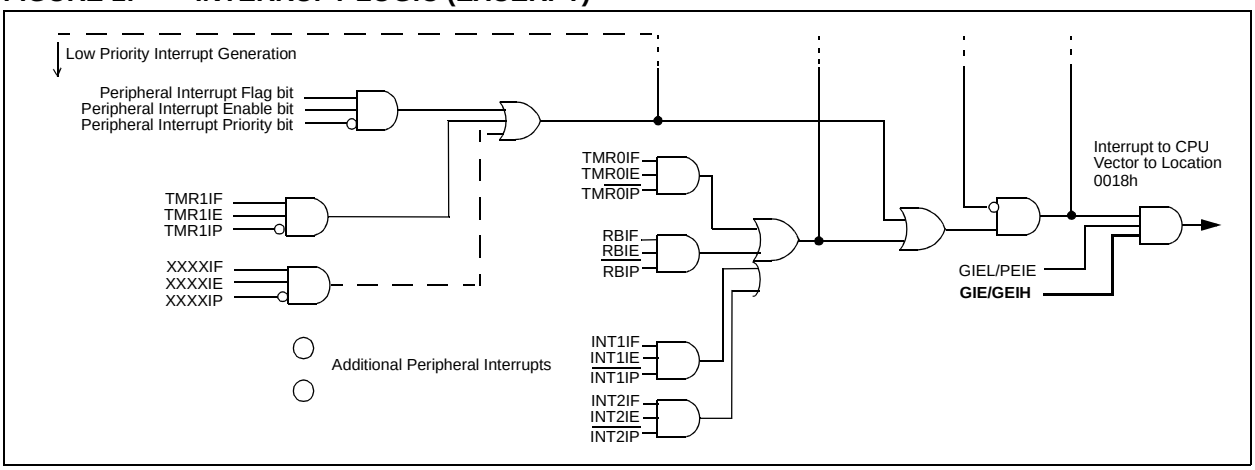
REGISTER 7-1: INTCON REGISTER (EXCERPT)

bit 7 **GIE/GIEH:** Global Interrupt Enable bit

When IPEN (RCON<7>) = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts

When IPEN (RCON<7>) = 1:
1 = Enables all high priority interrupts
0 = **Disables all interrupts**

FIGURE 1: INTERRUPT LOGIC (EXCERPT)



6. Module: USART

The operation of the USART Transmit Interrupt flag bit TXIF (PIR1<4>) is clarified as follows:

TXIF is not cleared immediately upon loading data into the transmit buffer TXREG. The flag bit becomes valid in the second instruction cycle following the load instruction (see Example 1). Polling TXIF immediately following a load of TXREG will give invalid results (Example 2).

This clarification applies to **all** USART transmission modes (master or slave, synchronous or asynchronous, 8-bit or 9-bit).

EXAMPLE 1: CORRECTLY POLLING THE TXIF BIT

```
movwf   TXREG       ;load the register
nop                 :first instruction--
                    ;just a placeholder, it
                    ;could be any instruction
btfss   PIR1,TXIF   ;second instruction--
                    ;now TXIF is valid
```

EXAMPLE 2: POLLING THE TXIF BIT IMMEDIATELY AFTER LOADING THE TRANSMIT BUFFER

```
movwf   TXREG       ;load the register
btfss   PIR1,TXIF   ;first instruction--
                    ;reading TXIF now will
                    ;give invalid results
```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7. Module: Electrical Specifications

The operating frequency range has been updated.

The maximum frequency for an external clock is clarified as 200 kHz in LP mode, and 4 MHz in XT mode. For all Oscillator modes, parameters 1 and 1A are also clarified as being applicable to both industrial and extended temperature range devices.

The maximum external clock frequency (EC and ECIO modes) and oscillator frequency (HS mode) remains at 40 MHz, as originally reported in the Device Data Sheet (DS30475**A**). Also, the maximum clock and oscillator frequency for HS+PLL mode remains at 10 MHz. This supersedes the more conservative values reported for earlier silicon revisions. Other values of the related clock period parameters are updated accordingly.

Table 25-4, Parameters 1 and 1A of the Device Data Sheet are amended in part, as shown below (changes and additions in **bold**).

The voltage vs. frequency graphs have also been updated. Figures 25-1 and 25-2 of the Device Data Sheet are replaced with the graphs shown on the following page.

Date Codes that pertain to this issue:

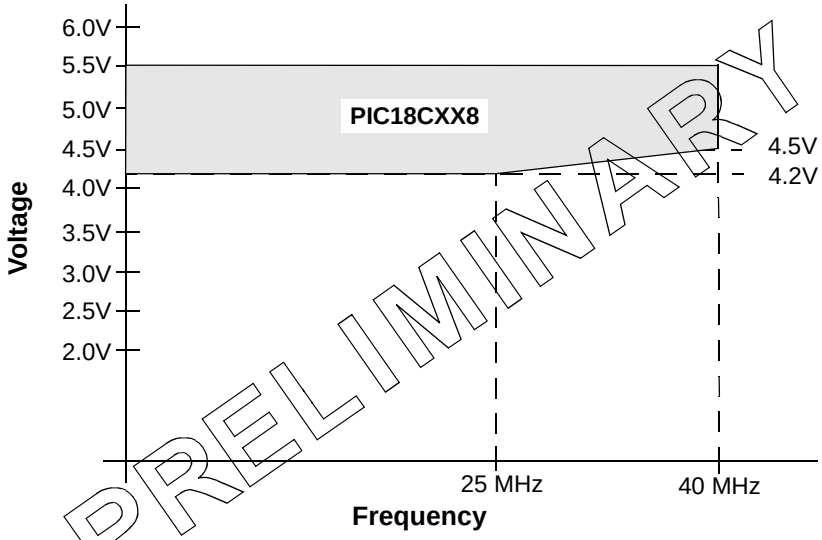
0233 and above

TABLE 25-4: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	FOSC	External CLKIN Frequency	**DC**	**4**	**MHz**	XT osc **(Industrial, Extended)**
			DC	**40**	**MHz**	HS osc **(Industrial, Extended)**
			4	**10**	**MHz**	HS + PLL osc **(Industrial, Extended)**
			DC	**200**	**kHz**	LP osc **(Industrial, Extended)**
			DC	**40**	**MHz**	EC**, ECIO (Industrial, Extended)**
		Oscillator Frequency	DC	4	MHz	RC osc **(Industrial, Extended**
			0.1	4	MHz	XT osc **(Industrial, Extended)**
			4	40	MHz	HS osc **(Industrial, Extended)**
			4	**10**	**MHz**	HS + PLL osc **(Industrial, Extended)**
			5	200	kHz	LP osc mode **(Industrial, Extended)**
1	TOSC	External CLKIN Period	**250**	—	ns	XT osc **(Industrial, Extended)**
			25	—	ns	HS osc **(Industrial, Extended)**
			100	**250**	**ns**	HS + PLL osc **(Industrial, Extended)**
			5	—	**µs**	LP osc **(Industrial, Extended)**
			25	**—**	**ns**	EC**, ECIO (Industrial, Extended)**
		Oscillator Period	250	—	ns	RC osc **(Industrial, Extended)**
			250	**—**	ns	XT osc **(Industrial, Extended)**
			25	**—**	**ns**	HS osc **(Industrial, Extended)**
			100	**250**	**ns**	HS + PLL osc **(Industrial, Extended)**
			5	—	µs	LP osc **(Industrial)**

Note: Footnotes in original table omitted for the sake of brevity.

FIGURE 25-1: PIC18CXX8 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL, EXTENDED)

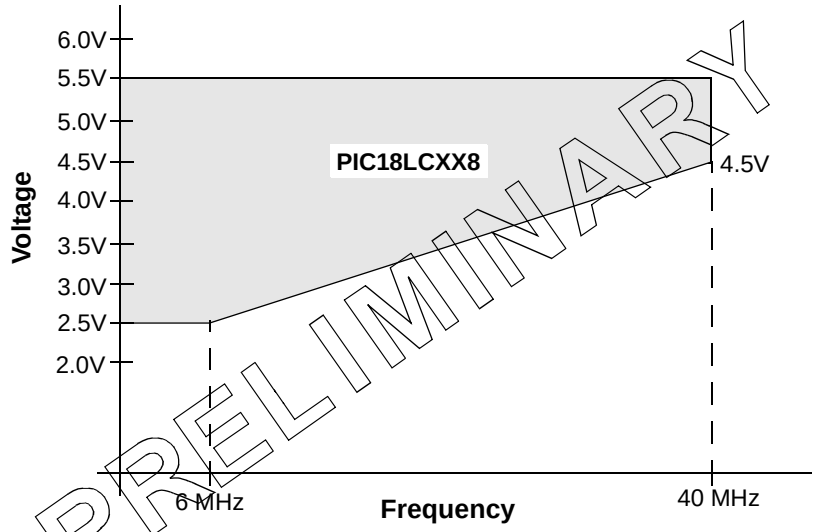


PRELIMINARY

FMAX = (50.0) (VDDAPPMIN – 4.2V) + 25 MHz, for 4.2V ≤ VDDAPPMIN ≤ 4.5V
FMAX = 40 MHz, for VDDAPPMIN > 4.5V

Note: VDDAPPMIN is the minimum voltage of the PICmicro® device in the application.

FIGURE 25-2: PIC18LCXX8 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



PRELIMINARY

FMAX = (17.0 MHz/V) (VDDAPPMIN – 2.5V) + 6 MHz, for VDDAPPMIN ≤ 4.5V
FMAX = 40 MHz for VDDAPPMIN > 4.5V

Note: VDDAPPMIN is the minimum voltage of the PICmicro® device in the application.

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8. Module: A/D (V_{REF}+ and V_{REF}- References)

The operation of the module is clarified by the addition of the following note to the end of Section 18.1 (“A/D Acquisition Requirements”):

Note: When using external voltage references with the A/D converter, the source impedance of the external voltage references must be less than 20Ω to obtain the specified A/D resolution. Higher reference source impedances will increase both offset and gain errors. Resistive voltage dividers will not provide a sufficiently low source impedance.

To maintain the best possible performance in A/D conversions, external V_{REF} inputs should be buffered with an operational amplifier or other low output impedance circuit.

APPENDIX A: REVISION HISTORY

Rev A Document (4/2002)
First revision of this document.

Rev B Document (9/2002)
Revision of previous data sheet correction 5 (Electrical Specifications) and addition of new voltage vs. frequency graphs to create data sheet correction 7 (Electrical Specifications). Previous items 6 and 7 (Interrupts and USART) renumbered as 5 and 6.
Removes previous and obsoleted silicon issue 10 (Core — Voltage vs. Frequency) and renumbers subsequent silicon issues 11 through 13 as issues 10 through 12.

Rev C Document (3/2003)
Added silicon issue 13 (A/D (External Voltage Reference) and Comparator Voltage Reference), and data sheet clarification issue 8 (A/D - $V_{REF}+$ and $V_{REF}-$ References).

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