PIC18(L)F2X/4X/6XK40

Large Memory, Highly Integrated 8-Bit General Purpose Flash Microcontrollers Product Brief

Description:

PIC18(L)F2X/4X/6XK40 microcontrollers combine large Flash/EE/RAM memory, rich peripheral integration, eXtreme Low-Power (XLP) technology and 5V support for a wide range of general purpose and low-power applications. These 28/40/44/64-pin devices deliver Core Independent Peripherals (CIPs) such as Complementary Waveform Generator (CWG), Windowed Watchdog Timer (WWDT), Cyclic Redundancy Check (CRC)/Memory Scan, Zero-Cross Detect (ZCD) and Peripheral Pin Select (PPS), providing for increased design flexibility and lower system cost. Additionally, this family includes a 10-bit ADC with Computation (ADC^2) extensions for automated signal analysis to reduce the complexity of the application.

Core Features:

- C Compiler Optimized RISC Architecture
- Only 83 Instructions
- Operating Speed:
  - 0-64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Interrupt Capability
- 31-Level Deep Hardware Stack
- Up to Four 8-bit Timers/Counters
- Up to Five 16-bit Timers/Counters
- Low Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Extended Watchdog Timer (WDT) with Dedicated On-Chip Oscillator for Reliable Operation
- Programmable Code Protection
- Window Watchdog Timer (WWDT):
  - Timer monitoring of overflow and underflow events
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software

Memory:

- Up to 128 Kbytes Flash Program Memory
- Up to 3720 bytes Data SRAM Memory
- Up to 1024 bytes Data EEPROM

Operating Characteristics:

- Operating Voltage Ranges:
  - 1.8V to 3.6V (PIC18LF2X/4X/6XK40)
  - 2.3V to 5.5V (PIC18F2X/4X/6XK40)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Operating Modes:

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is slower)
- Idle: CPU Halted while Peripherals Operate
- Sleep: Lowest Power Consumption

eXtreme Low-Power (XLP) Features:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Digital Peripherals:

- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Up to Five Capture/Compare/PWM (CCP) modules
- PWM: Two 10-Bit Pulse-Width Modulators
- Serial Communications:
  - Up to five Enhanced USART (EUSART)
  - Up to two SPI, I^2C, RS-232, RS-485, LIN compatible
  - Auto-Baud Detect, Auto-wake-up on start
- Up to 59 I/O Pins and One Input-Only Pin:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for fail-safe operation (e.g., Class B)
  - Calculate CRC over any portion of Flash or EEPROM
  - High-speed or background operation

- Hardware Limit Timer (HLT):
  - Hardware monitoring and Fault detection
- Signal Measurement Timer (SMT):
  - 24-bit signal measurement timer and 24-bit timer/counter
- Hardware Capacitive Voltage Divider (CVD):
  - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
  - Adjustable sample and hold capacitor array
  - Two guard ring output drives
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Analog Peripherals:

- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 47 external channels
  - Conversion available during Sleep
  - Temperature indicator
  - Internal and external trigger options
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- 5-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Programmable 5-bit voltage (% of V_{DD})
  - Internal connections to comparators, Fixed Voltage Reference and ADC
- Up to Three Comparators (CMP):
  - Four external inputs
  - External output via PPS
- Fixed Voltage Reference (FVR) module:
  - 1.024V, 2.048V and 4.096V output levels

Clocking Structure:

- 16 MHz Internal Oscillator Block:
  - ±1% at calibration
  - Selectable frequency range from 1 MHz to 16 MHz
- 32 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Two Crystal/Resonator modes up to 64 MHz
  - External clock up to 64 MHz
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up

Programming/Debug Features:

- In-Circuit Debug Integrated On-Chip
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

TABLE 1: PIC18(L)F2X/4X/6XK40 FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (bytes)	Data SRAM (bytes)	Data EEPROM (bytes)	I/O Pins	16-bit/8-bit Timers	Comparators	10-bit ADC^2 (ch)	5-bit DAC	Zero-Cross Detect	CCP/10-bit PWM	CWG	HLT	Windowed Watchdog Timer	CRC with Memory Scan	EUSART	I^{2}C/SPI	PPS	Debug(1)	SMT
PIC18(L)F24K40	(A)	16k	1024	256	25	4/3	2	24	1	1	2/2	1	3	Y	Y	1	1	Y	I	0
PIC18(L)F25K40	(A)	32k	2048	256	25	4/3	2	24	1	1	2/2	1	3	Y	Y	1	1	Y	I	0
PIC18(L)F26K40	(B)	64k	3720	1024	25	4/3	2	24	1	1	2/2	1	3	Y	Y	2	2	Y	I	0
PIC18(L)F27K40	(C)	128k	3720	1024	25	4/3	2	24	1	1	2/2	1	3	Y	Y	2	2	Y	I	0
PIC18(L)F45K40	(B)	32k	2048	256	36	4/3	2	35	1	1	2/2	1	3	Y	Y	2	2	Y	I	0
PIC18(L)F46K40	(B)	64k	3720	1024	36	4/3	2	35	1	1	2/2	1	3	Y	Y	2	2	Y	I	0
PIC18(L)F47K40	(C)	128k	3720	1024	36	4/3	2	35	1	1	2/2	1	3	Y	Y	2	2	Y	I	0
PIC18(L)F65K40	(D)	32k	2048	1024	60	5/4	3	47	1	1	5/2	1	4	Y	Y	5	2	Y	I	2
PIC18(L)F66K40	(D)	64k	3562	1024	60	5/4	3	47	1	1	5/2	1	4	Y	Y	5	2	Y	I	2
PIC18(L)F67K40	(E)	128k	3562	1024	60	5/4	3	47	1	1	5/2	1	4	Y	Y	5	2	Y	I	2

Note 1: Debugging Methods: (I) – Integrated on Chip; (H) – via ICD Header; E – using Emulation Product.

Data Sheet Index:

- **A.** DS40001843 PIC18(L)F24K40/25K40 Data Sheet, 28-Pin, 8-bit Flash Microcontrollers
- **B.** DS40001816 PIC18(L)F26K40/45K40/46K40 Data Sheet, 28/40-Pin, 8-bit Flash Microcontrollers
- **C.** DS40001844 PIC18(L)F27K40/47K40 Data Sheet, 28/40-Pin, 8-bit Flash Microcontrollers
- **D.** DS40001842 PIC18(L)F65K40/66K40 Data Sheet, 64-Pin, 8-bit Flash Microcontrollers
- **E.** DS40001841 PIC18(L)F67K40 Data Sheet, 64-Pin, 8-bit Flash Microcontrollers

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

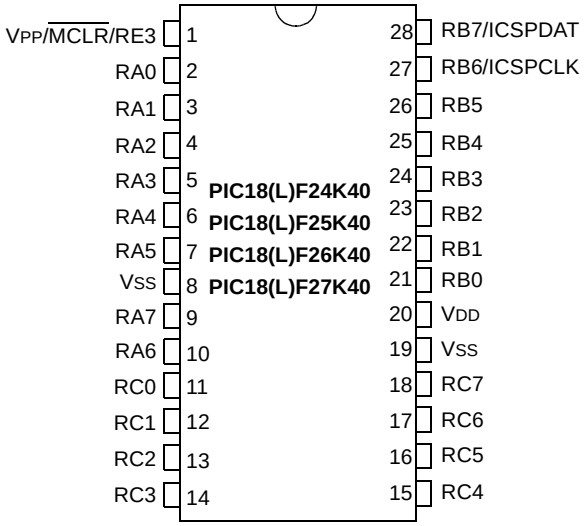
TABLE 2: PACKAGES

Packages	SPDIP (SP)	SOIC (SO)	SSOP (SS)	QFN (ML) (6x6x0.9)	UQFN (MV) (4x4x0.5)	TQFP (PT)	PDIP (P)	UQFN (MV) (5x5x0.5)	QFN (ML) (8x8)	QFN (MR) (9x9)
PIC18(L)F24K40	X	X	X	X	X					
PIC18(L)F25K40	X	X	X	X	X					
PIC18(L)F26K40	X	X	X	X	X					
PIC18(L)F27K40	X	X	X	X						
PIC18(L)F45K40						X	X	X	X	
PIC18(L)F46K40						X	X	X	X	
PIC18(L)F47K40						X	X	X	X	
PIC18(L)F65K40						X				X
PIC18(L)F66K40						X				X
PIC18(L)F67K40						X				X

Note: Pin details are subject to change.

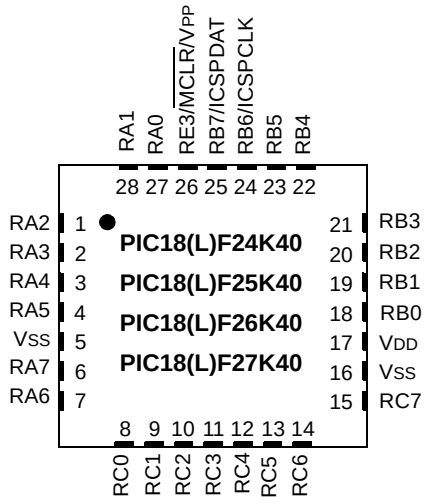
PIN DIAGRAMS

FIGURE 1: 28-PIN PDIP, SOIC, SSOP PIN DIAGRAM FOR PIC18(L)F24K40, PIC18(L)F25K40, PIC18(L)F26K40, PIC18(L)F27K40



Note: See Table 3 for location of all peripheral functions.

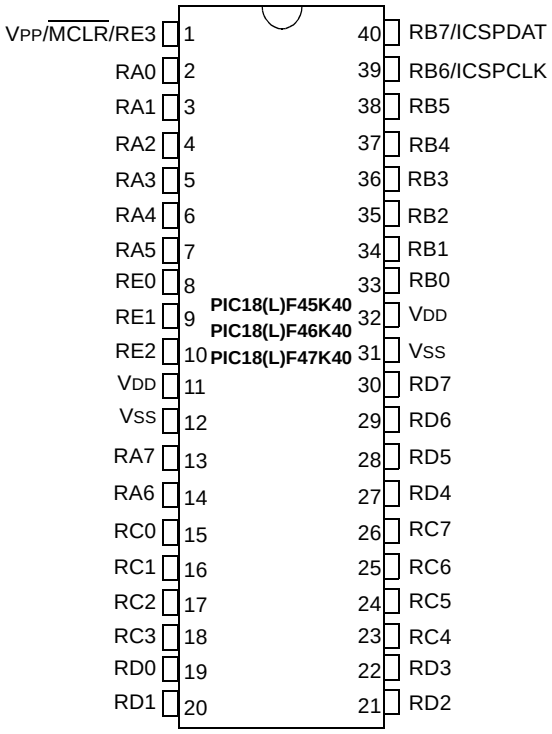
FIGURE 2: 28-PIN UQFN (4x4x0.5 mm), QFN (6x6x0.9 mm) PIN DIAGRAM FOR PIC18(L)F24K40, PIC18(L)F25K40, PIC18(L)F26K40, PIC18(L)F27K40



Note 1: See Table 3 for location of all peripheral functions.

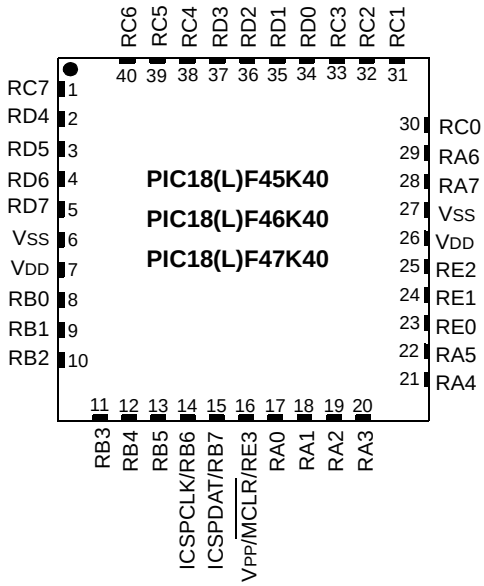
2: It is recommended that the exposed bottom pad be connected to VSS.

FIGURE 3: 40-PIN PDIP PIN DIAGRAM FOR PIC18(L)F45K40, PIC18(L)F46K40, PIC18(L)F47K40



Note: See Table 4 for location of all peripheral functions.

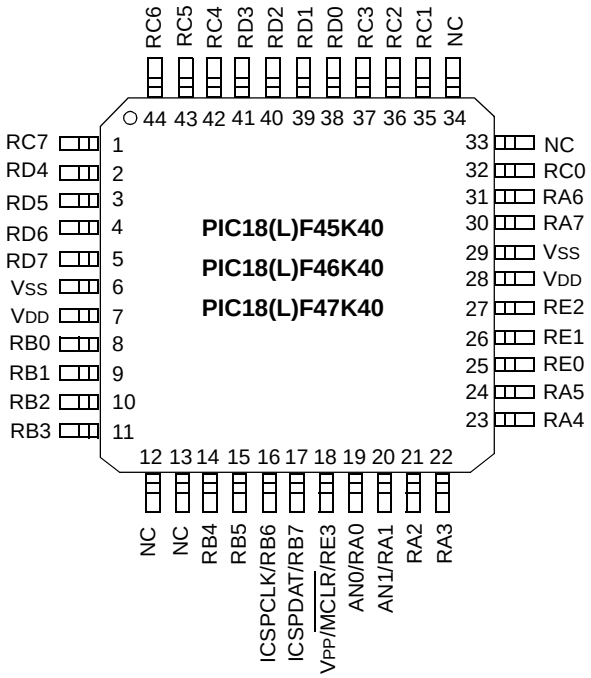
FIGURE 4: 40-PIN UQFN (5x5x0.5 mm) PIN DIAGRAM FOR PIC18(L)F45K40, PIC18(L)F46K40, PIC18(L)F47K40



Note 1: See Table 4 for location of all peripheral functions.

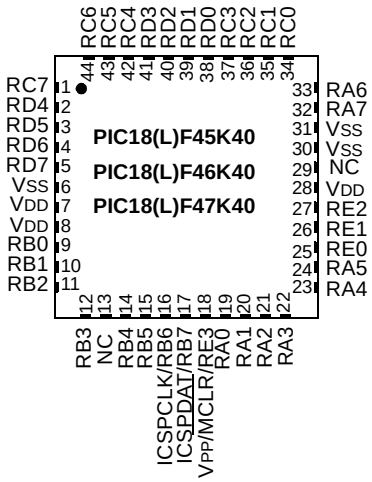
2: It is recommended that the exposed bottom pad be connected to VSS.

FIGURE 5: 44-PIN TQFP PIN DIAGRAM FOR PIC18(L)F45K40, PIC18(L)F46K40, PIC18(L)F47K40



Note: See Table 4 for location of all peripheral functions.

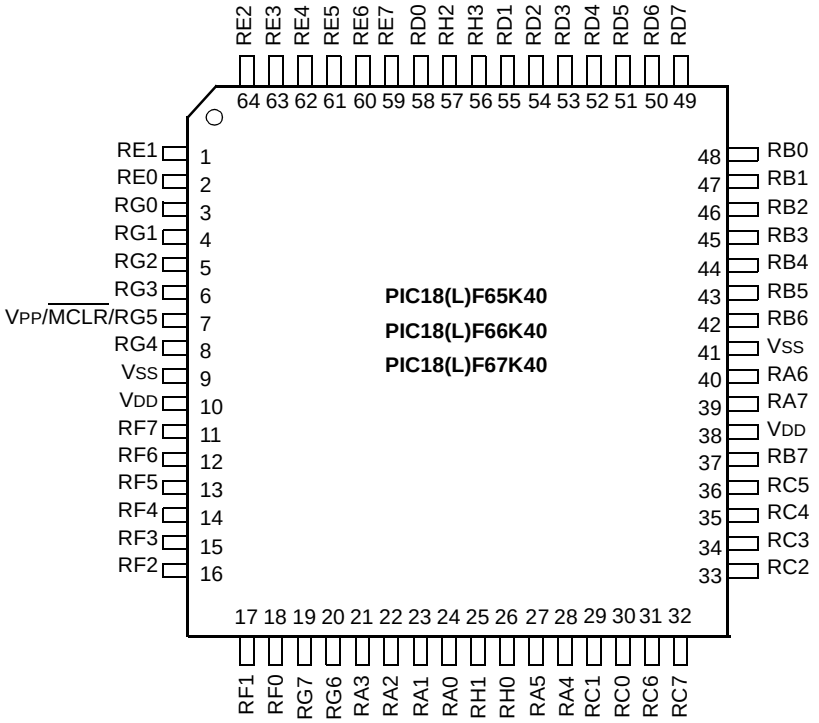
FIGURE 6: 44-PIN QFN (8x8x0.9 mm) PIN DIAGRAM FOR PIC18(L)F45K40, PIC18(L)F46K40, PIC18(L)F47K40



Note 1: See Table 4 for location of all peripheral functions.

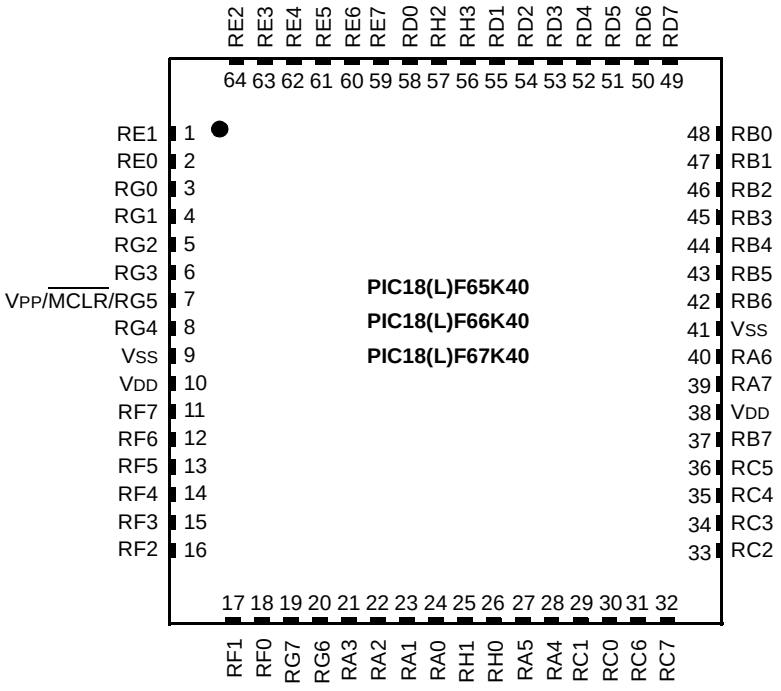
2: It is recommended that the exposed bottom pad be connected to VSS.

FIGURE 7: 64-PIN TQFP PIN DIAGRAM FOR PIC18(L)F65K40, PIC18(L)F66K40, PIC18(L)F67K40



Note 1: See Table 5 for list of pin peripheral function.

FIGURE 8: 64-PIN QFN (9x9 mm) PIN DIAGRAM FOR PIC18(L)F65K40, PIC18(L)F66K40, PIC18(L)F67K40



Note 1: See Table 5 for list of pin peripheral function.

PIN ALLOCATION TABLES

TABLE 3: 28-PIN ALLOCATION TABLE (PIC18(L)F2XK40)

I/O(2)	28-Pin PDIP, SOIC, SSOP	28-Pin (U)QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	LVD	Pull-up	Basic
RA0	2	27	ANA0	—	C1IN0- C2IN0-	—	—	—	—	IOCA0	—	—	—	—	Y	—
RA1	3	28	ANA1	—	C1IN1- C2IN1-	—	—	—	—	IOCA1	—	—	—	—	Y	—
RA2	4	1	ANA2	DAC1OUT1 VREF- (DAC5) VREF- (ADC)	C1IN0+ C2IN0+	—	—	—	—	IOCA2	—	—	—	—	Y	—
RA3	5	2	ANA3	VREF+ (DAC5) VREF+ (ADC)	C1IN1+	—	—	—	—	IOCA3	—	MDCIN1(1)	—	—	Y	—
RA4	6	3	ANA4	—	—	T0CKI(1)	—	—	—	IOCA4	—	MDCIN2(1)	—	—	Y	—
RA5	7	4	ANA5	—	—	—	—	—	—	IOCA5	—	MDMIN(1)	$\overline{SS1}$(1)	LVDIN	Y	—
RA6	10	7	ANA6	—	—	—	—	—	—	IOCA6	—	—	—	—	Y	CLKOUT OSC2
RA7	9	6	ANA7	—	—	—	—	—	—	IOCA7	—	—	—	—	Y	OSC1 ECIN
RB0	21	18	ANB0	—	C2IN1+	—	—	CWG1(1)	ZCD	IOCB0 INT0(1)	—	—	$\overline{SS2}$(1,4)	—	Y	—
RB1	22	19	ANB1	—	C1IN3- C2IN3-	—	—	—	—	IOCB1 INT1(1)	—	—	SCK2(1,4) SCL2(3,4)	—	Y	—
RB2	23	20	ANB2	—	—	—	—	—	—	IOCB2 INT2(1)	—	—	SDI2(1,4) SDA2(3,4)	—	Y	—
RB3	24	21	ANB3	—	C1IN2- C2IN2-	—	—	—	—	IOCB3	—	—	—	—	Y	—
RB4	25	22	ANB4	—	—	T5G(1)	—	—	—	IOCB4	—	—	—	—	Y	—
RB5	26	23	ANB5	—	—	T1G(1)	—	—	—	IOCB5	—	—	—	—	Y	—
RB6	27	24	ANB6	—	—	—	—	—	—	IOCB6	CK2(4)	—	—	—	Y	ICSPCLK
RB7	28	25	ANB7	DAC1OUT2	—	T6AIN(1)	—	—	—	IOCB7	RX2/ DT2(4)	—	—	—	Y	ICSPDAT

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: Not available on PIC18(L)F24/25K40.

TABLE 3: 28-PIN ALLOCATION TABLE (PIC18(L)F2XK40) (CONTINUED)

I/O(2)	28-Pin PDIP, SOIC, SSOP	28-Pin (U)QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	LVD	Pull-up	Basic
RC0	11	8	ANC0	—	—	T1CKI(1) T3CKI(1) T3G(1)	—	—	—	IOCC0	—	—	—	—	Y	SOSCO
RC1	12	9	ANC1	—	—	—	CCP2(1)	—	—	IOCC1	—	—	—	—	Y	SOSCIN SOSCI
RC2	13	10	ANC2	—	—	T5CKI(1)	CCP1(1)	—	—	IOCC2	—	—	—	—	Y	—
RC3	14	11	ANC3	—	—	T2AIN(1)	—	—	—	IOCC3	—	—	SCK(1) SCL1(3)	—	Y	—
RC4	15	12	ANC4	—	—	—	—	—	—	IOCC4	—	—	SDI1(1) SDA1(3)	—	Y	—
RC5	16	13	ANC5	—	—	T4AIN(1)	—	—	—	IOCC5	—	—	—	—	Y	—
RC6	17	14	ANC6	—	—	—	—	—	—	IOCC6	TX/CK(1)	—	—	—	Y	—
RC7	18	15	ANC7	—	—	—	—	—	—	IOCC7	RX/DT(1)	—	—	—	Y	—
RE3	1	26	—	—	—	—	—	—	—	IOCE3	—	—	—	—	Y	$\overline{\text{MCLR}}$
VSS	19	16	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
AVDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	AVDD
AVSS	8	5	—	—	—	—	—	—	—	—	—	—	—	—	—	AVSS

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: Not available on PIC18(L)F24/25K40.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC18(L)F4XK40)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	LVD	Pull-up	Basic
RA0	2	17	19	19	ANA0	—	—	—	—	—	—	IOCA0	—	—	—	—	Y	—
RA1	3	18	20	20	ANA1	—	C1IN1- C2IN1-	—	—	—	—	IOCA1	—	—	—	—	Y	—
RA2	4	19	21	21	ANA2	DAC1OUT1 VREF- (DAC5) VREF- (ADC)	C1IN0+ C2IN0+	—	—	—	—	IOCA2	—	—	—	—	Y	—
RA3	5	20	22	22	ANA3	VREF+ (DAC5) VREF+ (ADC)	C1IN1+	—	—	—	—	IOCA3	—	MDCIN1(1)	—	—	Y	—
RA4	6	21	23	23	ANA4	—	—	T0CKI(1)	—	—	—	IOCA4	—	MDCIN2(1)	—	—	Y	—
RA5	7	22	24	24	ANA5	—	—	—	—	—	—	IOCA5	—	MDMIN(1)	$\overline{SS1}$(1)	LVDIN	Y	—
RA6	14	29	33	31	ANA6	—	—	—	—	—	—	IOCA6	—	—	—	—	Y	CLKOUT OSC2
RA7	13	28	32	30	ANA7	—	—	—	—	—	—	IOCA7	—	—	—	—	Y	OSC1 ECIN
RB0	33	8	9	8	ANB0	—	C2IN1+	—	—	CWG1(1)	ZCD	IOCB0 INT0(1)	—	—	$\overline{SS2}$(1)	—	Y	—
RB1	34	9	10	9	ANB1	—	C1IN3- C2IN3-	—	—	—	—	IOCB1 INT1(1)	—	—	SCK2(1) SCL2(3)	—	Y	—
RB2	35	10	11	10	ANB2	—	—	—	—	—	—	IOCB2 INT2(1)	—	—	SDI2(1) SDA2(3)	—	Y	—
RB3	36	11	12	11	ANB3	—	C1IN2- C2IN2-	—	—	—	—	IOCB3	—	—	—	—	Y	—
RB4	37	12	14	14	ANB4	—	—	T5G(1)	—	—	—	IOCB4	—	—	—	—	Y	—
RB5	38	13	15	15	ANB5	—	—	T1G(1)	—	—	—	IOCB5	—	—	—	—	Y	—
RB6	39	14	16	16	ANB6	—	—	—	—	—	—	IOCB6	CK2(1)	—	—	—	Y	ICSPCLK
RB7	40	15	17	17	ANB7	DAC1OUT2	—	T6AIN(1)	—	—	—	IOCB7	RX2/ DT2(1)	—	—	—	Y	ICSPDAT
RC0	15	30	34	32	ANC0	—	—	T1CKI(1) T3CKI(1) T3G(1)	—	—	—	IOCC0	—	—	—	—	Y	SOSCO
RC1	16	31	35	35	ANC1	—	—	—	CCP2(1)	—	—	IOCC1	—	—	—	—	Y	SOSCIN SOSCI
RC2	17	32	36	36	ANC2	—	—	T5CKI(1)	CCP1(1)	—	—	IOCC2	—	—	—	—	Y	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC18(L)F4XK40) (CONTINUED)

I/O(2)	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	EUSART	DSM	MSSP	LVD	Pull-up	Basic
RC3	18	33	37	37	ANC3	—	—	T2AIN(1)	—	—	—	IOCC3	—	—	SCK1(1) SCL1(3)	—	Y	—
RC4	23	38	42	42	ANC4	—	—	—	—	—	—	IOCC4	—	—	SDI1(1) SDA1(3)	—	—	—
RC5	24	39	43	43	ANC5	—	—	T4AIN(1)	—	—	—	IOCC5	—	—	—	—	Y	—
RC6	25	40	44	44	ANC6	—	—	—	—	—	—	IOCC6	—	—	—	—	Y	—
RC7	26	1	1	1	ANC7	—	—	—	—	—	—	IOCC7	TX/CK(1)	—	—	—	Y	—
RD0	19	34	38	38	AND0	—	—	—	—	—	—	IOCD0	RX/DT(1)	—	—	—	Y	—
RD1	20	35	39	39	AND1	—	—	—	—	—	—	IOCD1	—	—	—	—	Y	—
RD2	21	36	40	40	AND2	—	—	—	—	—	—	IOCD2	—	—	—	—	Y	—
RD3	22	37	41	41	AND3	—	—	—	—	—	—	IOCD3	—	—	—	—	Y	—
RD4	27	2	2	2	AND4	—	—	—	—	—	—	IOCD4	—	—	—	—	Y	—
RD5	28	3	3	3	AND5	—	—	—	—	—	—	IOCD5	—	—	—	—	Y	—
RD6	29	4	4	4	AND6	—	—	—	—	—	—	IOCD6	—	—	—	—	Y	—
RD7	30	5	5	5	AND7	—	—	—	—	—	—	IOCD7	—	—	—	—	Y	—
RE0	8	23	25	25	ANE0	—	—	—	—	—	—	IOCE0	—	—	—	—	Y	—
RE1	9	24	26	26	ANE1	—	—	—	—	—	—	IOCE1	—	—	—	—	Y	—
RE2	10	25	27	27	ANE2	—	—	—	—	—	—	IOCE2	—	—	—	—	Y	—
RE3	1	16	18	18	—	—	—	—	—	—	—	IOCE3	—	—	—	—	Y	$\overline{MCLR}$
VSS	12	6	6	6	—	—	—	—	—	—	—	—	—	—	—	—	—	AVSS
VDD	11	7	7	7	—	—	—	—	—	—	—	—	—	—	—	—	—	AVDD
VDD	32	26	28	28	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	31	27	30	29	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VDD	—	—	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VDD	—	—	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 5: 64-PIN ALLOCATION TABLE PIC18(L)F6XK40

I/O	64-pin TQFP/QFN	ADC	DAC	Comparators	Zero Cross Detect	MSSP (SPI/I²C)	EUSART	DSM	Timers	SMT	CCP and PWM	CWG	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RA0	24	ANA0	—	C1IN4- C2IN4- C3IN4-	—	—	—	—	T8IN(1)	—	—	—	—	—	—
RA1	23	ANA1	—	—	—	—	—	—	T2IN(1)	—	—	—	—	—	—
RA2	22	VREF- ANA2	VREF-	C1IN1+ C2IN1+ C3IN1+	—	—	—	—	—	—	—	—	—	—	—
RA3	21	VREF+ ANA3	VREF+	—	—	—	—	—	—	—	—	—	—	—	—
RA4	28	ANA4	—	—	—	—	—	—	T0CKI(1)	—	—	—	—	—	—
RA5	27	ANA5	—	—	—	—	—	—	T3G(1)	—	—	—	—	—	—
RA6	40	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	OSC2 CLKOUT
RA7	39	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	OSC1 CLKIN
RB0	48	ANB0	—	—	ZCD	—	—	—	—	—	—	—r	—	INT0(1) IOCB0	—
RB1	47	ANB1	—	—	—	—	—	—	—	—	—	—	—	INT1(1) IOCB1	—
RB2	46	ANB2	—	—	—	—	—	—	—	—	—	—	—	INT2(1) IOCB2	—
RB3	45	ANB3	—	—	—	—	—	—	—	—	—	—	—	INT3(1) IOCB3	—
RB4	44	ANB4	—	—	—	—	—	—	—	—	—	—	—	IOCB4	—
RB5	43	ANB5	—	—	—	—	—	—	T1G(1) T3CKI(1)	—	—	—	—	IOCB5	—
RB6	42	ANB6	—	—	—	—	—	—	—	—	—	—	—	IOCB6	ICSPCLK
RB7	37	ANB7	DAC1OUT2	—	—	—	—	—	—	—	—	—	—	IOCB7	ICSPDAT
RC0	30	—	—	—	—	—	CK4(3)	—	T1CKI(1)	—	—	—	—	IOCC0	SOSCO

Note 1: This is a PPS remappable signal. The input function may be removed from the default location shown to one of several other PORTx pins. Details about this can be found in the data sheet.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several POTRTx pin options. Details about this can be found in the data sheet.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I²C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected b the INLVL register, instead of the I²C specific input buffer thresholds.

TABLE 5: 64-PIN ALLOCATION TABLE PIC18(L)F6XK40 (CONTINUED)

I/O	64-pin TQFP/QFN	ADC	DAC	Comparators	Zero Cross Detect	MSSP (SPI/I²C)	EUSART	DSM	Timers	SMT	CCP and PWM	CWG	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RC1	29	—	—	—	—	—	RX4(1) DT4(3)	—	T6IN(1)	—	—	—	—	IOCC1	SOSCI
RC2	33	—	—	—	—	—	—	—	—	—	—	CWG1IN(1)	—	IOCC2	—
RC3	34	—	—	—	—	SCL1(3,4) SCK1(1)	—	—	—	—	—	—	—	IOCC3	—
RC4	35	—	—	—	—	SDA1(3,4) SDI1(1)	—	—	—	—	—	—	—	IOCC4	—
RC5	36	—	—	—	—	—	—	—	—	—	—	—	—	IOCC5	—
RC6	31	—	—	—	—	—	CK1(3)	—	—	—	—	—	—	IOCC6	—
RC7	32	—	—	—	—	—	RX1(1) DT1(3)	—	—	—	—	—	—	IOCC7	—
RD0	58	AND0	—	—	—	—	—	—	—	—	—	—	—	—	—
RD1	55	AND1	—	—	—	—	—	—	T5CKI(1) T7G(1)	—	—	—	—	—	—
RD2	54	AND2	—	—	—	—	—	—	—	—	—	—	—	—	—
RD3	53	AND3	—	—	—	—	—	MDCARL(1)	—	—	—	—	—	—	—
RD4	52	AND4	—	—	—	—	—	MDCARH(1)	—	—	—	—	—	—	—
RD5	51	AND5	—	—	—	SDA2(3,4) SDI2(1)	—	MDSRC(1)	—	—	—	—	—	—	—
RD6	50	AND6	—	—	—	SCL2(3,4) SCK2(1)	—	—	—	—	—	—	—	—	—
RD7	49	AND7	—	—	—	$\overline{SS2}$(1)	—	—	—	—	—	—	—	—	—
RE0	2	ANE0	—	—	—	—	CK3(3)	—	—	—	—	—	—	IOCE0	—
RE1	1	ANE1	—	—	—	—	RX3(1) DT3(3)	—	—	—	—	—	—	IOCE1	—
RE2	64	ANE2	—	—	—	—	CK5(3)	—	—	—	—	—	—	IOCE2	—
RE3	63	ANE3	—	—	—	—	RX5(1) DT5(3)	—	—	—	—	—	—	IOCE3	—
RE4	62	ANE4	—	—	—	—	—	—	T4IN(1)	—	CCP5(1)	—	—	IOCE4	—
RE5	61	ANE5	—	—	—	—	—	—	—	—	CCP4(1)	—	—	IOCE5	—

Note 1: This is a PPS remappable signal. The input function may be removed from the default location shown to one of several other PORTx pins. Details about this can be found in the data sheet.
2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several POTRTx pin options. Details about this can be found in the data sheet.
3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4: These pins are configured for I²C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected b the INLVL register, instead of the I²C specific input buffer thresholds.

TABLE 5: 64-PIN ALLOCATION TABLE PIC18(L)F6XK40 (CONTINUED)

I/O	64-pin TQFP/QFN	ADC	DAC	Comparators	Zero Cross Detect	MSSP (SPI/I²C)	EUSART	DSM	Timers	SMT	CCP and PWM	CWG	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RE6	60	ANE6	—	—	—	—	—	—	—	SMT1WIN1(1)	CCP3(1)	—	—	IOCE6	—
RE7	59	ANE7	—	—	—	—	—	—	—	SMT1SIG1(1)	—	—	—	IOCE7	—
RF0	18	ANF0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	—
RF1	17	ANF1	—	—	—	—	—	—	—	—	—	—	—	—	—
RF2	16	ANF2	—	—	—	—	—	—	—	—	—	—	—	—	—
RF3	15	ANF3	—	C1IN2- C2IN2- C3IN2-	—	—	—	—	—	—	—	—	—	—	—
RF4	14	ANF4	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—
RF5	13	ANF5	DAC1OUT1	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—
RF6	12	ANF6	—	C1IN0+	—	—	—	—	—	—	—	—	—	—	—
RF7	11	ANF7	—	C1IN3- C2IN3- C3IN3-	—	$\overline{SS1}$(1)	—	—	—	—	—	—	—	—	—
RG0	3	ANG0	—	—	—	—	—	—	—	—	—	—	—	—	—
RG1	4	ANG1	—	—	—	—	CK2(3)	—	—	—	—	—	—	—	—
RG2	5	ANG2	—	C3IN0+	—	—	RX2(1) DT2(3)	—	—	—	—	—	—	—	—
RG3	6	ANG3	—	C3IN0-	—	—	—	—	—	—	CCP1(1)	—	—	—	—
RG4	8	ANG4	—	C3IN1-	—	—	—	—	T5G(1) T7CKI(1)	—	CCP2(1)	—	—	—	—
RG5	7	—	—	—	—	—	—	—	—	—	—	—	—	—	$\overline{MCLR}$ VPP
RG6	20	ANG6	—	—	—	—	—	—	—	SMT2WIN1(1)	—	—	—	—	—
RG7	19	ANG7	—	—	—	—	—	—	—	SMT2SIG1(1)	—	—	—	—	—
RH0	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RH1	25	ADCACT(1)	—	—	—	—	—	—	—	—	—	—	—	—	—
RH2	57	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Note 1: This is a PPS remappable signal. The input function may be removed from the default location shown to one of several other PORTx pins. Details about this can be found in the data sheet.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several POTRTx pin options. Details about this can be found in the data sheet.

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I/O	64-pin TQFP/QFN	ADC	DAC	Comparators	Zero Cross Detect	MSSP (SPI/I²C)	EUSART	DSM	Timers	SMT	CCP and PWM	CWG	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RH3	56	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VDD	10, 38	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	9, 41	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT(2)	—	ADGRDA ADGRDB	—	C1OUT C2OUT C3OUT	—	SDO1 SCK1 SDO2 SCK2	TX1/CK1(3) DT1(3) TX2/CK2(3) DT2(3) TX3/CK3(3) DT3(3) TX4/CK4(3) DT4(3) TX5/CK5(3) DT5(3)	DSM	TMR0	—	CCP1 CCP2 CCP3 CCP4 CCP5 PWM6OUT PWM7OUT	CWG1A CWG1B CWG1C CWG1D	CLKR	—	—

Note 1: This is a PPS remappable signal. The input function may be removed from the default location shown to one of several other PORTx pins. Details about this can be found in the data sheet.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several POTRTx pin options. Details about this can be found in the data sheet.

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