



PIC16F73/74/76/77

PIC16F73/74/76/77 (Rev. C0 Silicon) Data Sheet Errata

The PIC16F73/74/76/77 parts you have received conform functionally to the Device Data Sheet (DS30325B), except for the anomalies described below.

None.

Date Codes that pertain to Rev. C0 Silicon:

PIC16F73/74 0220 and later
PIC16F76/77 0304 and later

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30325B), the following clarifications and corrections should be noted.

1. Module: Core

The typical and maximum supply currents (parameter D010A) specified for extended voltage devices have been changed.

The I_{DD} specifications differ from the Device Data Sheet only for devices operating at a V_{DD} of 3.0V and a F_{osc} of 32 kHz with the WDT disabled.

The changes in the specification are shown in **bold** in Table 1.

TABLE 1: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic/ Device	New Specification			Data Sheet Specification			Units	Notes
			Min	Typ	Max	Min	Typ	Max		
D010A	I _{DD}	Supply Current PIC16LF73/74/76/77	—	25	48	—	20	48	μA	LP osc configuration, F _{osc} = 32 kHz, V _{DD} = 3.0V, WDT disabled

PIC16F73/74/76/77

2. Module: Pinout Correction

The MLF (now known as QFN) package pinout locations for pins RA4 and RA5 were incorrectly stated in Table 1-2 of the Device Data Sheet.

The correct pinout locations are indicated in **bold** in Table 2.

TABLE 2: PIC16F73 AND PIC16F76 PINOUT DESCRIPTION

Pin Name	DIP SSOP SOIC Pin#	MLF Pin#	I/O/P Type	Buffer Type	Description
. . . RA4/T0CKI RA4 T0CKI RA5/ <u>SS</u> /AN4 RA5 <u>SS</u> AN4	6 7	3 4	 I/O I I/O I I	ST TTL	 Digital I/O – Open drain when configured as output. Timer0 external clock input. Digital I/O. SPI slave select input. Analog input 4.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

3. Module: Pinout Correction

The PIC16F73/74/76/77 device family does not offer low-voltage programming. The Device Data Sheet incorrectly lists RB3 as providing the PGM function required for low-voltage programming.

References to the PGM function in Tables 1-2 and Table 1-3 of the Device Data Sheet have been removed. Table 3 and Table 4 show the corrections for the PIC16F73/76 and PIC16F74/77 devices respectively. The text shown in **bold** has been removed.

References to the PGM function in the Pin Diagrams on pages 2 and 3, and Figures 1-1 and 1-2 (pages 6 and 7) in the Data Sheet have also been removed.

A reference to the PGM function listed in the Data Sheet Index has also been removed.

TABLE 3: PIC16F73 AND PIC16F76 PINOUT DESCRIPTION

Pin Name	DIP SSOP SOIC Pin#	MLF Pin#	I/O/P Type	Buffer Type	Description
. . . RB3/ PGM RB3 PGM . . .	24	21	I/O I/O	TTL	Digital I/O. Low voltage ICSP programming enable pin.

TABLE 4: PIC16F74 AND PIC16F77 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
. . . RB3/ PGM RB3 PGM . . .	36	39	11	I/O I/O	TTL	Digital I/O. Low voltage ICSP programming enable pin.

PIC16F73/74/76/77

4. Module: Packaging (Pinout and Product Identification)

PIC16F74 and PIC16F77 devices are now offered in a 44-pin, micro lead frame package (commonly known as "QFN"). This provides near chip scale package size. This option is in addition to the 28-pin QFN packages already available for the PIC16F73 and PIC16F76 devices. The 44-pin QFN package has been added to the product line since the original publication of the Device Data Sheet.

The addition of this option requires the following additions to the Device Data Sheet (DS30325B). Referenced figures and tables follow this text.

1. The "Pin Diagrams" on pages 2-3 of the Data Sheet are amended with the addition of the 44-pin QFN pinout shown in Figure 1.
2. Table 1.3 of Section 1.0 ("Device Overview") is replaced with an updated version which adds a column for QFN pin assignments. All new information is indicated in **bold**.

3. Section 17.1 ("Package Marking Information") is amended to include a marking template and example for 44-pin QFN devices. These are shown in Figure 2.

4. Section 17.2 ("Package Details") is amended to include the mechanical drawing of the 44-pin QFN package, following the existing drawings. This is shown in Figure 3.

5. In the "PIC16F7X Product Identification System" (page 171), the "ML" line item in the "Package" options section should now read (change in **bold**):

ML = **QFN**

For the sake of completeness, it is also noted that the package designation "MLF" is now replaced by "QFN" in all occurrences throughout the Device Data Sheet. "MLF" should be considered an obsoleted term.

FIGURE 1: PINOUT DIAGRAM FOR PIC16F74/77, 44-PIN QFN PACKAGE

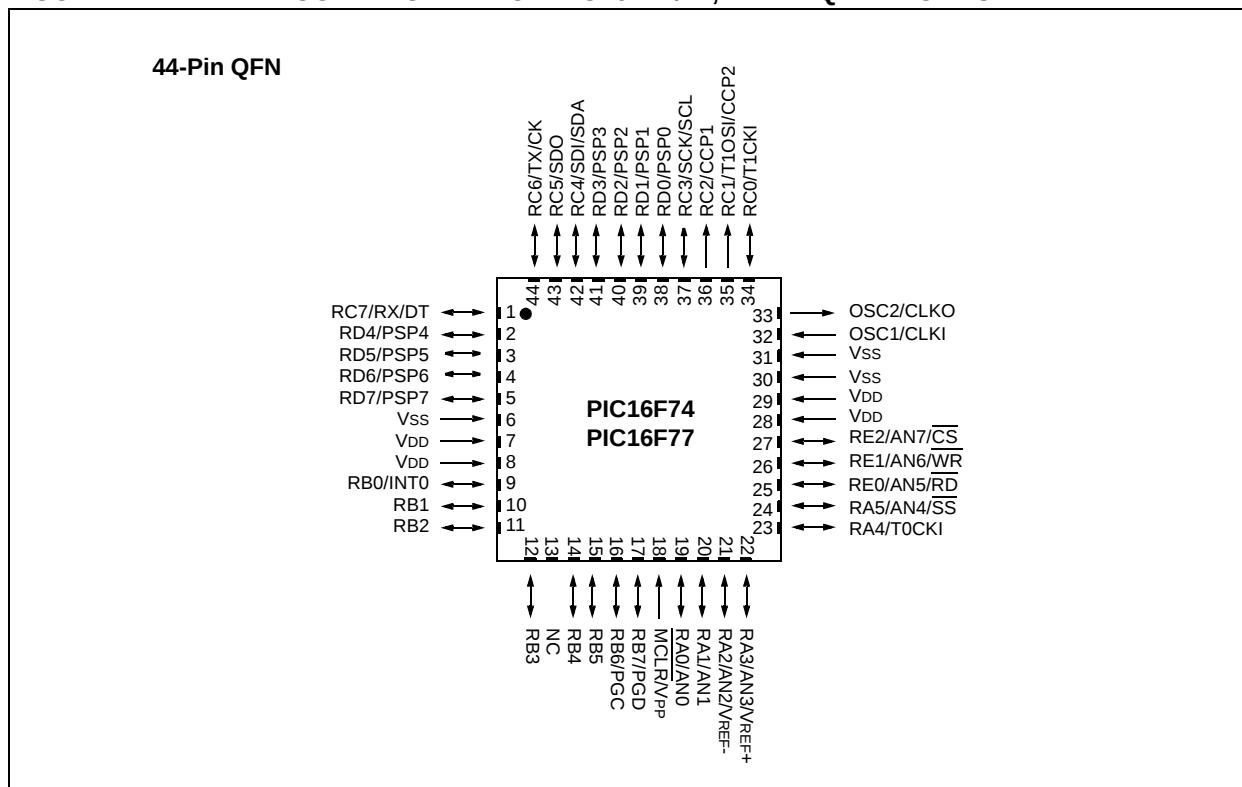
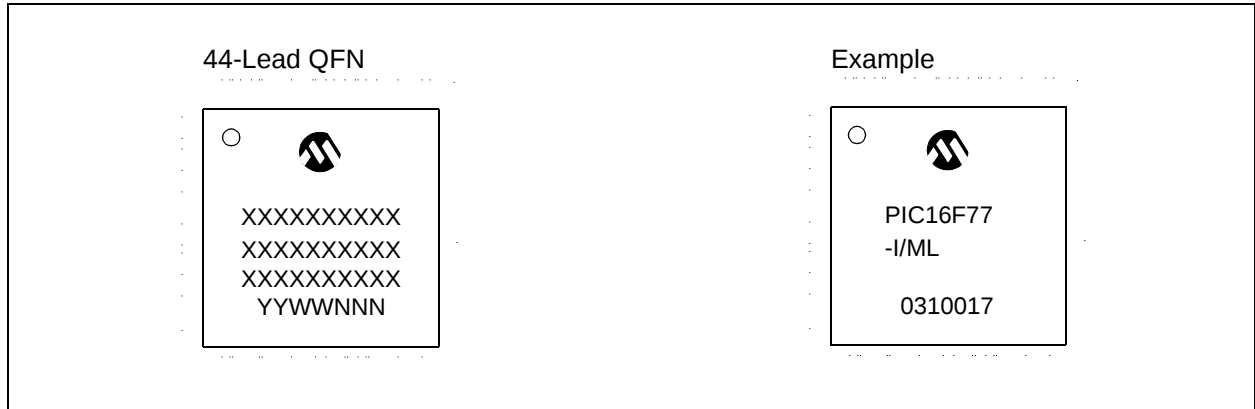


FIGURE 2: PACKAGE MARKING TEMPLATE FOR PIC16F74/77, 44-PIN QFN



PIC16F73/74/76/77

TABLE 1-3: PIC16F74/77 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFN Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI OSC1 CLKI	13	14	32	30	I	ST/CMOS ⁽⁴⁾	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS. External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO OSC2 CLKO	14	15	33	31	O	—	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP MCLR VPP	1	2	18	18	I/P	ST	Master Clear (input) or programming voltage (output). Master Clear (Reset) input. This pin is an active low RESET to the device. Programming voltage input.
RA0/AN0 RA0 AN0	2	3	19	19	I/O I	TTL	PORTA is a bidirectional I/O port. Digital I/O. Analog input 0. Digital I/O. Analog input 1. Digital I/O. Analog input 2. A/D reference voltage (Low) input. Digital I/O. Analog input 3. A/D reference voltage (High) input. Digital I/O – Open drain when configured as output. Timer0 external clock input.
RA1/AN1 RA1 AN1	3	4	20	20	I/O I	TTL	
RA2/AN2/VREF- RA2 AN2 VREF-	4	5	21	21	I/O I I	TTL	
RA3/AN3/VREF+ RA3 AN3 VREF+	5	6	22	22	I/O I I	TTL	
RA4/T0CKI RA4 T0CKI	6	7	23	23	I/O I	ST	
RA5/SS/AN4 RA5 SS AN4	7	8	24	24	I/O I I	TTL	

Legend: I = input O = output I/O = input/output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

- Note**
- 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
 - 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
 - 3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
 - 4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F74/77 PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP Pin#	PLCC Pin#	QFN Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
RB0/INT RB0 INT	33	36	9	8	I/O I	TTL/ST ⁽¹⁾	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. Digital I/O. External interrupt.
RB1	34	37	10	9	I/O	TTL	Digital I/O.
RB2	35	38	11	10	I/O	TTL	Digital I/O.
RB3	36	39	12	11	I/O	TTL	Digital I/O.
RB4	37	41	14	14	I/O	TTL	Digital I/O.
RB5	38	42	15	15	I/O	TTL	Digital I/O.
RB6/PGC RB6 PGC	39	43	16	16	I/O I/O	TTL/ST ⁽²⁾	Digital I/O. In-circuit debugger and ICSP™ programming clock.
RB7/PGD RB7 PGD	40	44	17	17	I/O I/O	TTL/ST ⁽²⁾	Digital I/O. In-circuit debugger and ICSP™ programming data.
RC0/T1OSO/T1CKI RC0 T1OSO T1CKI	15	16	34	32	I/O O I	ST	PORTC is a bidirectional I/O port. Digital I/O. Timer1 oscillator output. Timer1 external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2	16	18	35	35	I/O I I/O	ST	Digital I/O. Timer1 oscillator input. Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1 RC2 CCP1	17	19	36	36	I/O I/O	ST	Digital I/O. Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL RC3 SCK SCL	18	20	37	37	I/O I/O I/O	ST	Digital I/O. Synchronous serial clock input/output for SPI™ mode. Synchronous serial clock input/output for I²C™ mode.
RC4/SDI/SDA RC4 SDI SDA	23	25	42	42	I/O I I/O	ST	Digital I/O. SPI data in. I²C data I/O.
RC5/SDO RC5 SDO	24	26	43	43	I/O O	ST	Digital I/O. SPI data out.
RC6/TX/CK RC6 TX CK	25	27	44	44	I/O O I/O	ST	Digital I/O. USART asynchronous transmit. USART 1 synchronous clock.
RC7/RX/DT RC7 RX DT	26	29	1	1	I/O I I/O	ST	Digital I/O. USART asynchronous receive. USART synchronous data.

Legend: I = input O = output I/O = input/output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

- Note 1:** This buffer is a Schmitt Trigger input when configured as an external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

PIC16F73/74/76/77

TABLE 1-3: PIC16F74/77 PINOUT DESCRIPTION (CONTINUED)

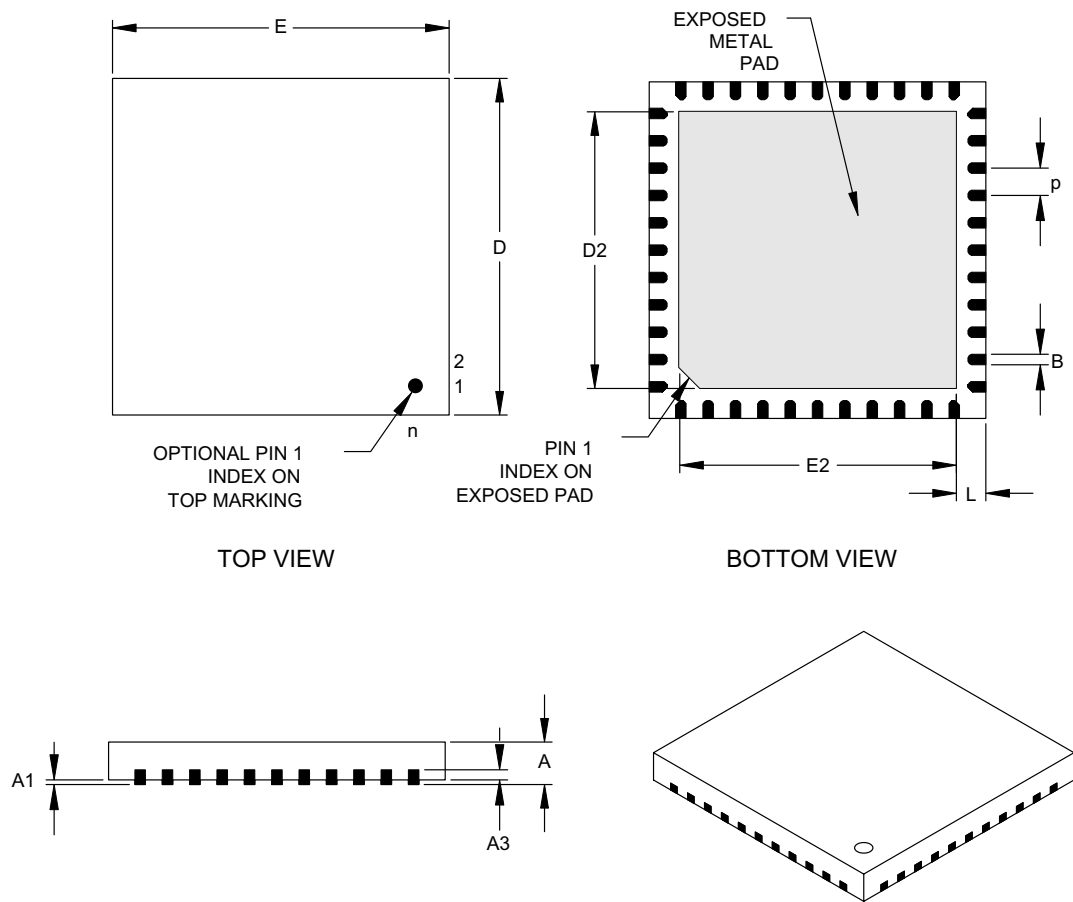
Pin Name	DIP Pin#	PLCC Pin#	QFN Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
RD0/PSP0 RD0 PSP0	19	21	38	38	I/O I/O	ST/TTL ⁽³⁾	PORTD is a bidirectional I/O port or parallel slave port when interfacing to a microprocessor bus. Digital I/O. Parallel Slave Port data.
RD1/PSP1 RD1 PSP1	20	22	39	39	I/O I/O	ST/TTL ⁽³⁾	Digital I/O. Parallel Slave Port data.
RD2/PSP2 RD2 PSP2	21	23	40	40	I/O I/O	ST/TTL ⁽³⁾	Digital I/O. Parallel Slave Port data.
RD3/PSP3 RD3 PSP3	22	24	41	41	I/O I/O	ST/TTL ⁽³⁾	Digital I/O. Parallel Slave Port data.
RD4/PSP4 RD4 PSP4	27	30	2	2	I/O I/O	ST/TTL ⁽³⁾	Digital I/O. Parallel Slave Port data.
RD5/PSP5 RD5 PSP5	28	31	3	3	I/O I/O	ST/TTL ⁽³⁾	Digital I/O. Parallel Slave Port data.
RD6/PSP6 RD6 PSP6	29	32	4	4	I/O I/O	ST/TTL ⁽³⁾	Digital I/O. Parallel Slave Port data.
RD7/PSP7 RD7 PSP7	30	33	5	5	I/O I/O	ST/TTL ⁽³⁾	Digital I/O. Parallel Slave Port data.
RE0/RD/AN5 RE0 RD AN5	8	9	25	25	I/O I I	ST/TTL ⁽³⁾	PORTE is a bidirectional I/O port. Digital I/O. Read control for parallel slave port. Analog input 5.
RE1/WR/AN6 RE1 WR AN6	9	10	26	26	I/O I I	ST/TTL ⁽³⁾	Digital I/O. Write control for parallel slave port. Analog input 6.
RE2/CS/AN7 RE2 CS AN7	10	11	27	27	I/O I I	ST/TTL ⁽³⁾	Digital I/O. Chip select control for parallel slave port. Analog input 7.
Vss	12,31	13,34	6, 30, 31	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7, 8, 28, 29	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17, 28,40	13	12,13, 33,34	—	—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

- Note**
- 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
 - 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
 - 3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
 - 4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

FIGURE 3: 44-PIN QFN PACKAGE (DRAWING 1, PACKAGING)

44-Lead Plastic Quad Flat No Lead Package (ML) 8x8 mm Body (QFN)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0	0.02	0.05
Base Thickness	A3		.010 REF			0.25 REF	
Overall Width	E		.315 BSC			8.00 BSC	
Exposed Pad Width	E2	.262	.268	.274	6.65	6.80	6.95
Overall Length	D		.315 BSC			8.00 BSC	
Exposed Pad Length	D2	.262	.268	.274	6.65	6.80	6.95
Lead Width	B	.012	.013	.013	0.30	0.33	0.35
Lead Length	L	.014	.016	.018	0.35	0.40	0.45

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC equivalent: M0-220

Drawing No. C04-103

PIC16F73/74/76/77

REVISION HISTORY

Rev A Document (8/2003)

First revision of this document. Device Data Sheet
Clarification issues 1 (Core), 2 (Pinout Correction),
3 (Pinout Correction) and 4 (Packaging).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, MPLAB, PIC, PICmicro, PICSTART, PRO MATE and PowerSmart are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, microID, MXDEV, MXLAB, PICMASTER, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

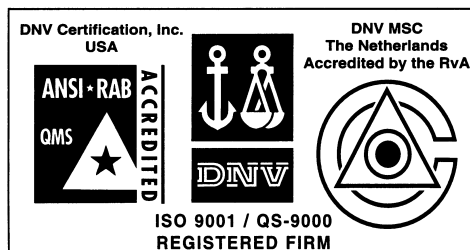
Accuron, Application Maestro, dsPICDEM, dsPICDEM.net, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICC, PICkit, PICDEM, PICDEM.net, PowerCal, PowerInfo, PowerMate, PowerTool, rFLAB, rPIC, Select Mode, SmartSensor, SmartShunt, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2003, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Atlanta

3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034
Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848
Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, IN 46902
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888
Fax: 949-263-1338

Phoenix

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966
Fax: 480-792-4338

San Jose

2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950
Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia

Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu

Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou

Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

China - Hong Kong SAR

Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai

Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700
Fax: 86-21-6275-5060

China - Shenzhen

Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380
Fax: 86-755-8295-1393

China - Shunde

Room 401, Hongjian Building
No. 2 Fengxiangnan Road, Ronggui Town
Shunde City, Guangdong 528303, China
Tel: 86-765-8395507 Fax: 86-765-8395571

China - Qingdao

Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India

Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessy Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea

168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or
82-2-558-5934

Singapore

200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Kaohsiung Branch
30F - 1 No. 8
Min Chuan 2nd Road
Kaohsiung 806, Taiwan
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan

Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria

Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark

Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France

Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany

Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy

Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands

P. A. De Biesbosch 14
NL-5152 SC Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom

505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820

07/28/03