
PIC16C781/782 Rev. B3 Silicon/Data Sheet Errata

The PIC16C781/782 parts you have received conform functionally to the Device Data Sheet (DS41171A), except for the anomalies described below.

Note: The silicon revision of a specific component is identified by its manufacture date code: YYWW, YY is the year of manufacture and WW is the specific work week. All material with a date code of 0229 or later is revision B3 silicon, and subject to the Errata contained in this document. Any components with a earlier date code will be silicon revision B1 and will be covered in a separate Errata. For additional information concerning date codes, refer to the packaging information section of the PIC16C781/782 data sheet (DS41171A).

1. Module: Voltage Comparator

When the voltage comparator inputs are subjected to fast rise time pulses, some units exhibit a momentary invalid state on their output. The probability of generating an invalid output state is dependant upon four factors:

1. Pulse slew rate
2. Supply Voltage (V_{DD})
3. Ambient Temperature
4. Reference Voltage (V_{COMMON_MODE})

Figures 1 through 5 show the input slew rate limits for normal operation of the voltage comparators in Fast mode ($CMxCON0<3>=1$) for a variety of Common mode voltages, supply voltages and ambient temperatures.

If the PSMC is used in conjunction with the voltage comparators, an invalid voltage comparator output state can cause the premature termination of PSMC output pulses.

Work around

The pulse rise time of inputs to the voltage comparators should be less than the limits shown in Figures 1 through 5 for the specific conditions of operation (supply voltage, temperature, Common mode voltage). The values shown are for pulses with a constant rise time. For pulses with compound rise times (pulses with non-linear or changing slopes), the limits may be different.

Note: The area below the line for any given temperature is the safe operating area. Graph data is from B1 revision silicon. When B3 revision characterization data is available, the slew rate limits will be relaxed to reflect the improved performance of B3 silicon.

PIC16C781/782

FIGURE 1: VOLTAGE COMPARATOR INPUT, MAXIMUM SLEW RATE AT V_{DD} = 5.5V, FAST MODE

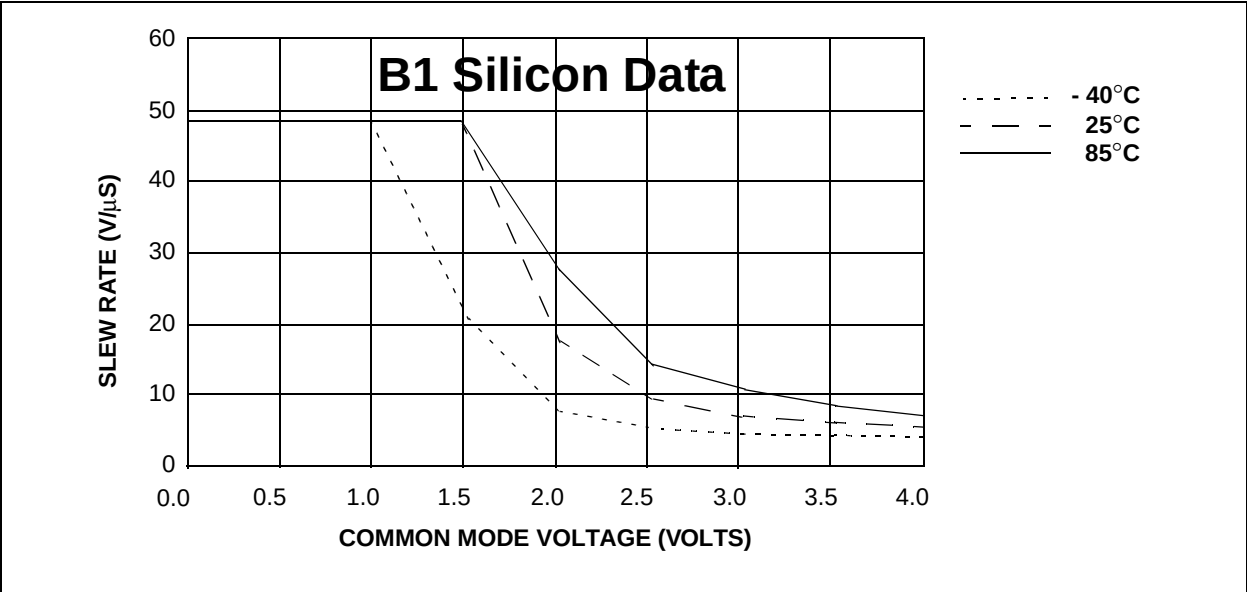


FIGURE 2: VOLTAGE COMPARATOR INPUT, MAXIMUM SLEW RATE AT V_{DD} = 5.5V, FAST MODE

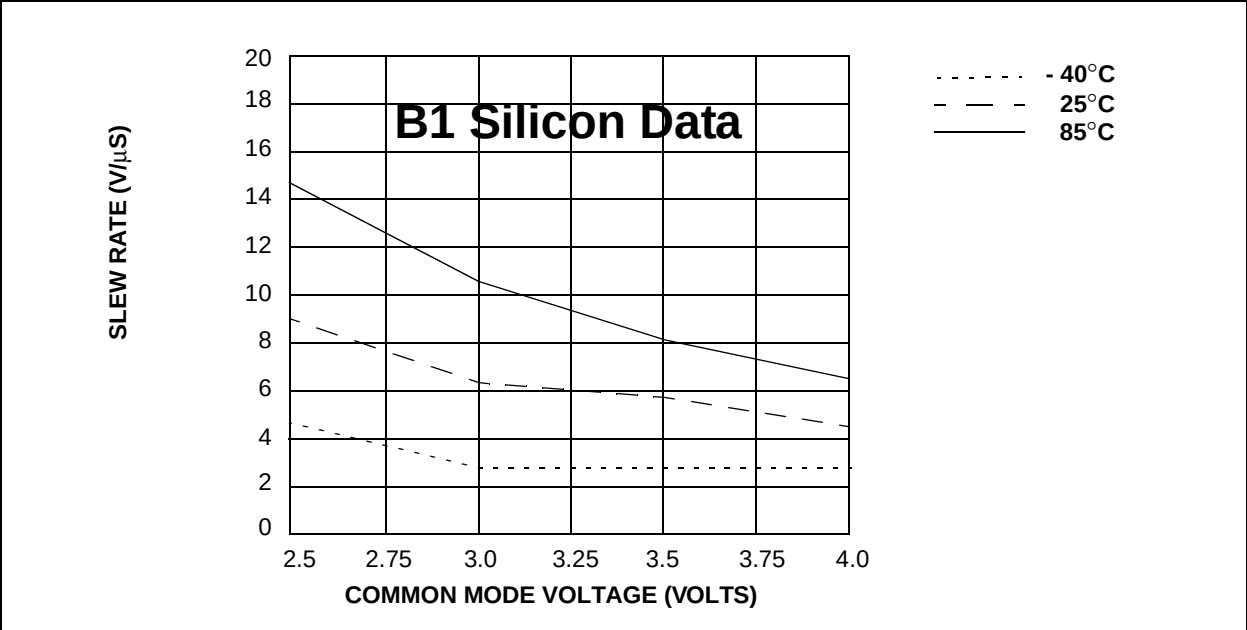


FIGURE 3: VOLTAGE COMPARATOR INPUT, MAXIMUM SLEW RATE AT V_{DD} = 4.0V, FAST MODE

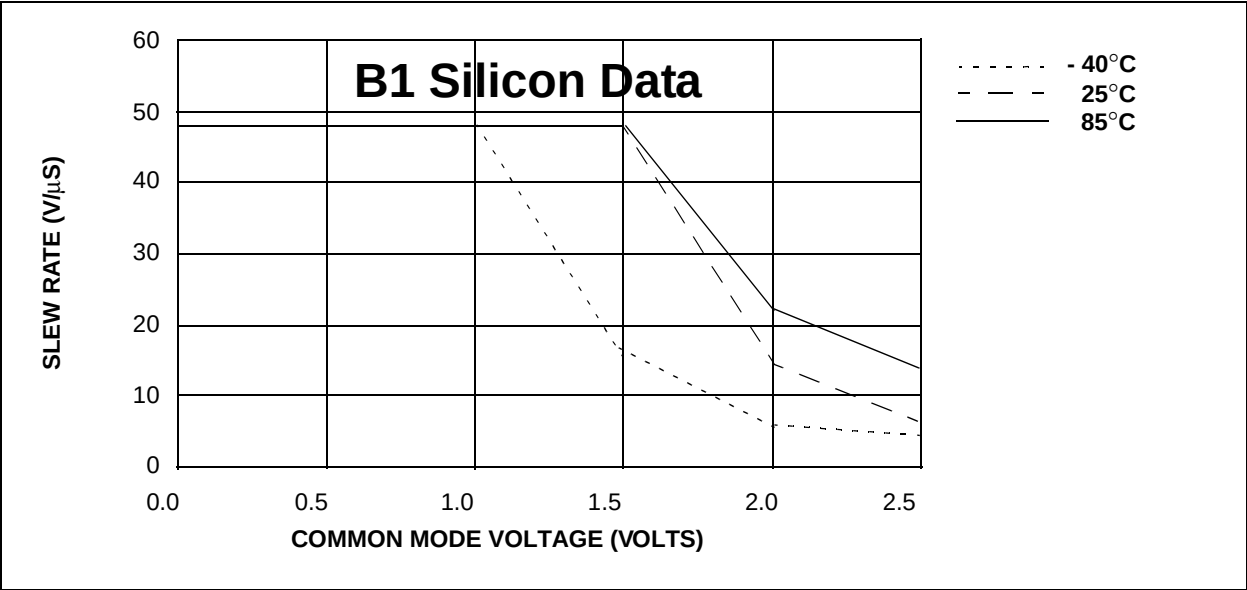
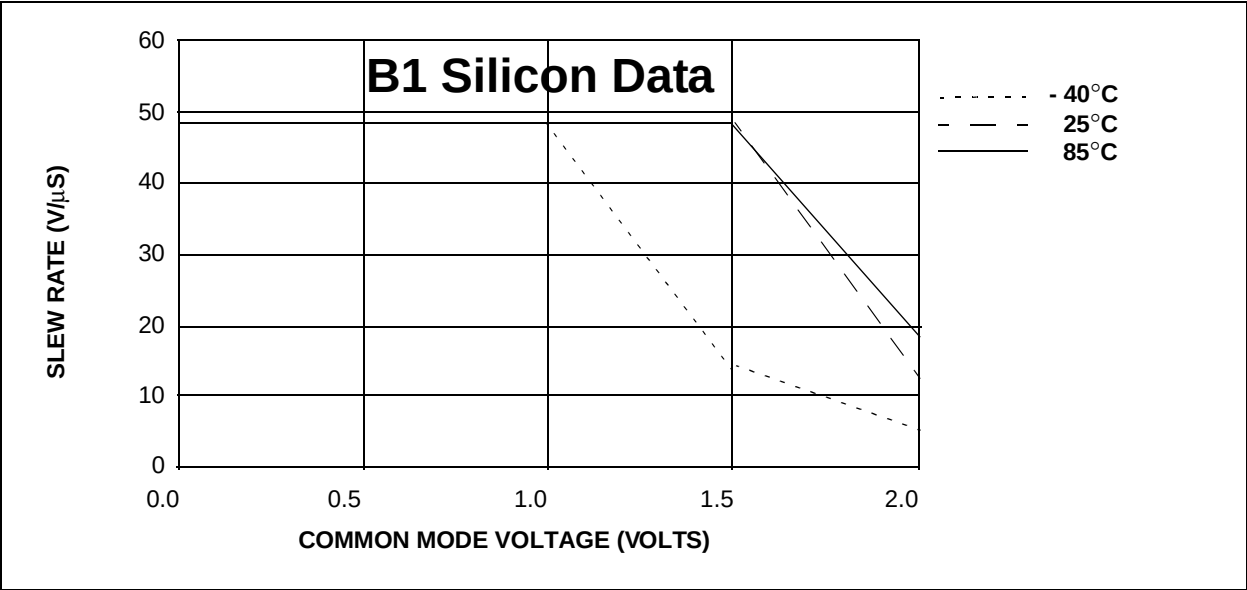
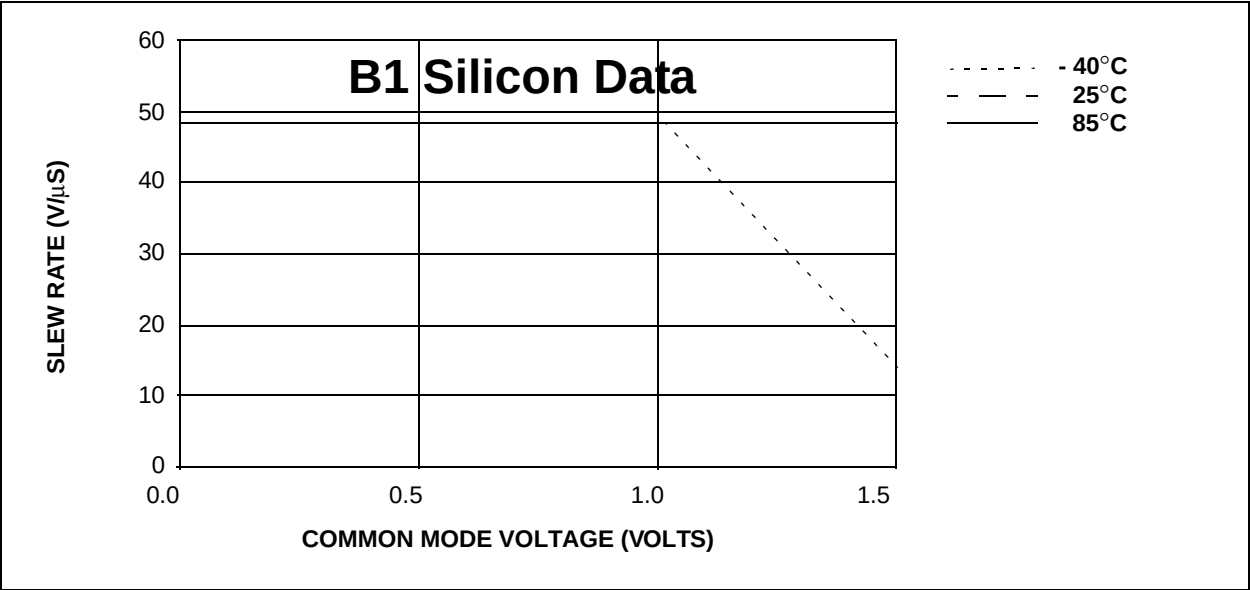


FIGURE 4: VOLTAGE COMPARATOR INPUT, MAXIMUM SLEW RATE AT V_{DD} = 3.5V, FAST MODE



PIC16C781/782

FIGURE 5: VOLTAGE COMPARATOR INPUT, MAXIMUM SLEW RATE AT VDD = 3.0V, FAST MODE



Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41171A), the following clarifications and corrections should be noted.

1. Module: I/O Ports

Exception to Figure 3-6 on page 32.

When the RA5 pin is configured as the external MCLR input (CONFIG<MCLRE> = 1), the port bit will read as set (RA<5> = 1), not cleared, as specified in Figure 3-6.

2. Module: Digital-to-Analog Converter

Correction to Example 10-1 on page 81.

The following line of code:

```
"BSF    ANSEL,1      ;set RB1 as analog"
```

Should be:

```
"BSF    ANSEL,5      ;set RB1 as analog"
```

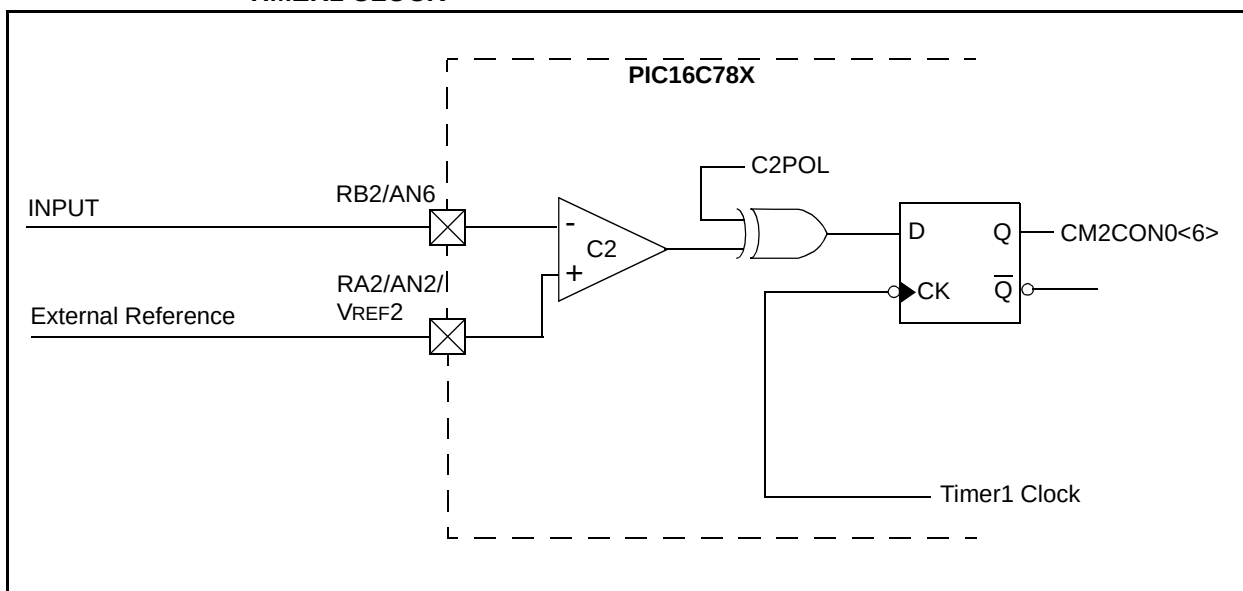
Note: DAC output function overrides ANSEL and TRISB register control of the port pin.

3. Module: Comparator Module

Correction to Figure 12-3 on page 95.

The synchronizing clock signal is supplied by the Timer1 clock, not the RA6 pin as shown in Figure 12-3.

FIGURE 12-3: COMPARATOR C2 CONFIGURATION WITH OUTPUT SYNCHRONIZED TO TIMER1 CLOCK



PIC16C781/782

REVISION HISTORY

Rev A Document (1/02)

Original errata document, which includes Item 1 and clarifications/corrections to Data Sheet, Items 1, 2 and 3.

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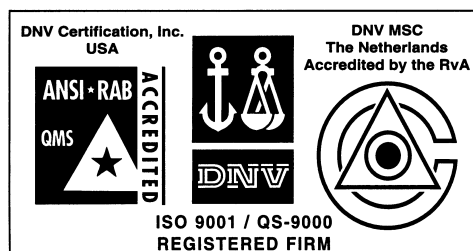
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