

PIC16C745/765 Rev. A1 Silicon/Data Sheet Errata

The PIC16C745/765 (Rev. A1) parts you have received conform functionally to the PIC16C745/765 Data Sheet (DS41124C), except for the anomalies described below.

Note: The silicon revision of a specific component is identified by its manufacture date code: YYWW. YY is the year of manufacture and WW is the specific work week. All material with a date code of 0230 or earlier is Rev. A1 silicon and subject to this Errata document. Components with a date code later than 0230 will be Rev. A2 silicon and will be covered by a separate Errata document. For additional information concerning date codes, refer to the packaging information section of the PIC16C745/765 Data Sheet (DS41124C)

All significant issues listed here are addressed by Rev. A2 of the PIC16C745/765 silicon.

1. Module: USB Transceiver

The first bit in the sync pattern during Microcontroller-to-host transactions is elongated by approximately 100 ns (see Figure 1). According to Section 7.1.11 of the USB Specification, Version 1.1, the bit period for a low speed device can vary 1.5% from 667 ns. This

means the average bit length can vary from 657 ns to 676 ns. Section 7.1.13.1 states, "For low speed transmissions, the jitter time for any consecutive differential data transitions must be within ± 25 ns and within ± 10 ns for any set of paired differential data transitions."

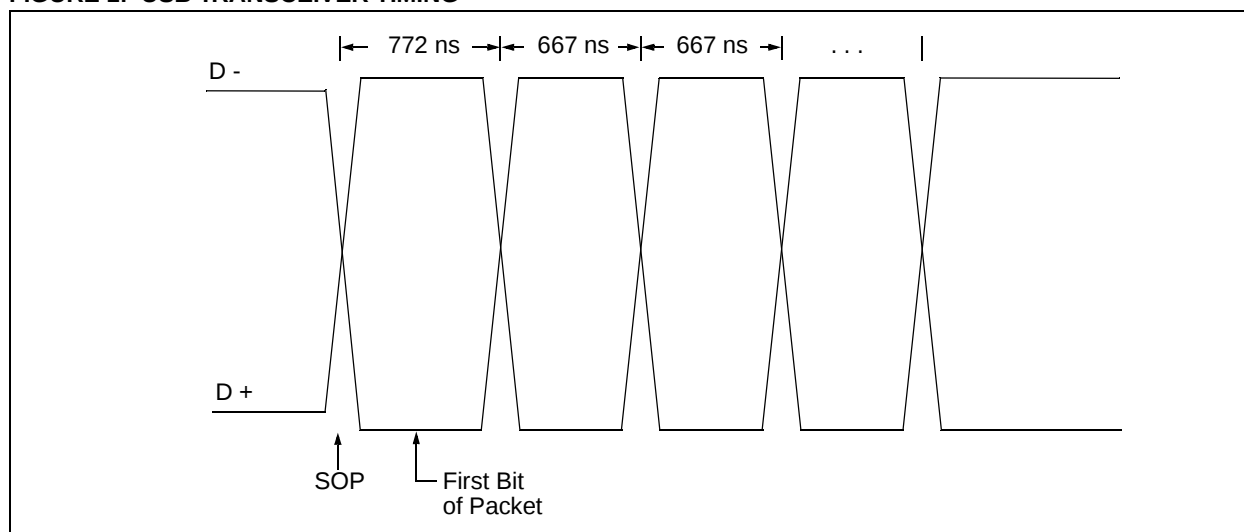
The initial bit from the PIC16C745/765, at approximately 772 ns in length, violates the consecutive transition jitter specification by 71 ns to 90 ns, depending on the actual data rate. It violates the paired data transition jitter specification by 82 ns to 120 ns, depending on the actual data rate. Devices based on the PIC16C745/765 are likely to fail the USB Implementer's Forum Compliance Test due to the jitter violation. However, the elongated bit does not affect the reliability of USB transactions between current USB host controllers and the PIC16C745/765. All packets are communicated successfully between microcontroller and host.

Work Around

No work around available.

Note: USB-IF certification is necessary only if use of the USB logo is desired.

FIGURE 1: USB TRANSCEIVER TIMING



PIC16C745/765

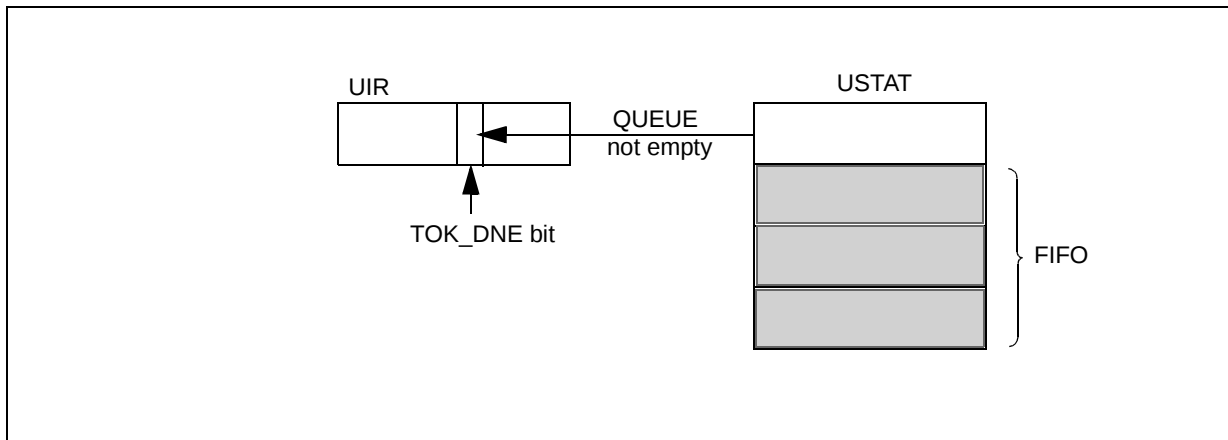
2. Module: USTAT Register

The TOK_DNE bit (UIR Bit 3) is not set correctly for pending USB transactions in the USTAT register (see Figure 2). If additional transactions arrive prior to clearing the TOK_DNE bit, they will be lost.

Work around

The interrupt driver Microchip firmware does not lose any transactions with current operating systems.

FIGURE 2: UIR / USTAT REGISTER



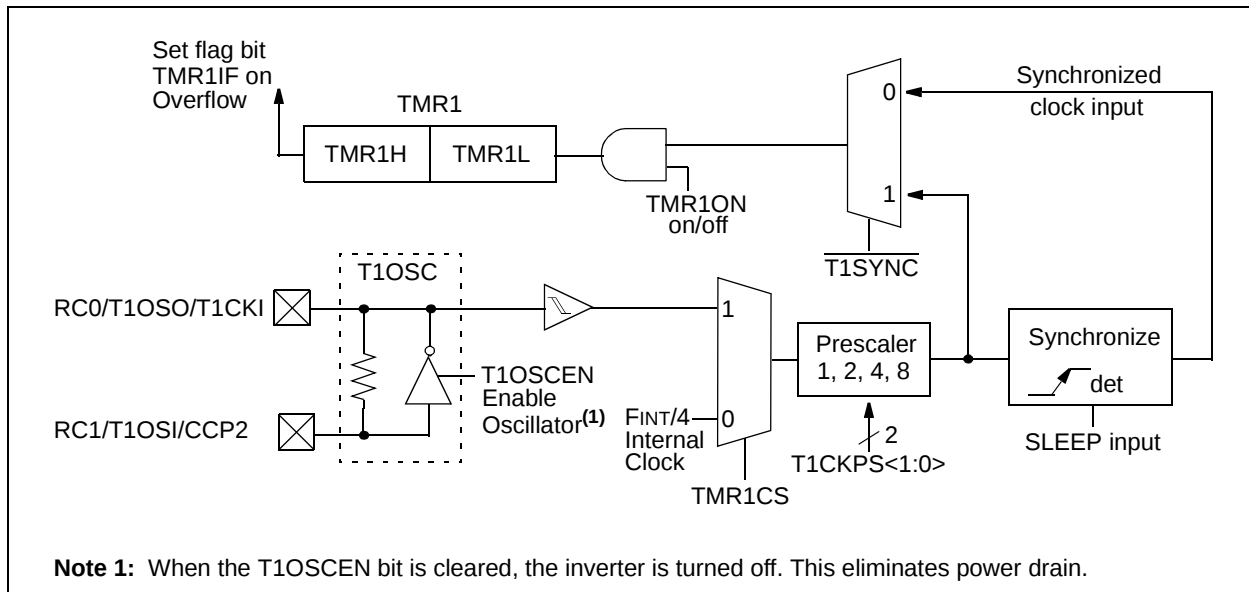
Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet, the following clarifications and corrections should be noted.

1. Module: Timer1

In Section 7.0, Timer1 module, there is an error in Figure 7-1. The label FINT should read FINT/4.

FIGURE 7-1: TIMER1 BLOCK DIAGRAM



PIC16C745/765

APPENDIX A: REVISION HISTORY

Rev A Document (9/01)

Original Errata document.

Issue 1 (USTAT Register) was added (page 1).

USB Transceiver Timing was added to page 1.

Rev B Document (6/02)

Under the Clarifications/Corrections to the Data Sheet, Issue 1 (Timer1) was added (page 2).

Rev C Document (9/02)

All reference to PIC16C745 in this Errata document is changed to PIC16C745/765.

All reference to Rev. A in this Errata document is changed to Rev. A1.

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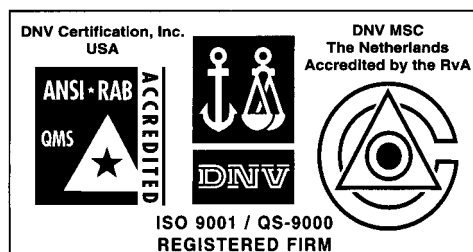
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