

PIC16(L)F18313/18323 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F18313/18323 family devices that you have received conform functionally to the current Device Data Sheet (DS40001799F), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC16(L)F18313/18323 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A6**).

Data Sheet clarifications and corrections start on [page 7](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F18313/18323 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾		
		A3	A4	A6
PIC16F18313	3066h	2003h	2004h	2006h
PIC16LF18313	3068h	2003h	2004h	2006h
PIC16F18323	3067h	2003h	2004h	2006h
PIC16LF18323	3069h	2003h	2004h	2006h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the "*PIC16(L)F183XX Memory Programming Specification*" (DS40001738) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾		
				A3	A4	A6
Oscillators	Register Reset Values	1.1	Reset value of OSCTUNE register is 0x20.	X		
Oscillators	32 MHz Clock	1.2	32 MHz Internal Clock Signal is not stable.	X		
Oscillators	Fail-Safe Clock Monitor (FSCM)	1.3	The FSCM may fail to trigger.	X		
Oscillators	Status Flag	1.4	PLLR bit of OSCSTAT1 register is incorrectly cleared.	X		
EUSART	Transmit	2.1	TX pin driven low.	X		
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.1	Slave Select release during Sleep corrupts data.	X		
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.2	Receive data lost when Slave Select enable occurs just before Sleep execution.	X		
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.3	WCOL improperly set in Sleep.	X		
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	3.4	SSPBUF transmit shift register may be corrupted under certain conditions.	X	X	X
Nonvolatile Memory (NVM) Control	NVMREG Access	4.1	Self-writes on LF devices below 2.2V at -40°C may not work.	X	X	
Nonvolatile Memory (NVM) Control	WRERR Bit	4.2	Write Error (WRERR) bit is incorrectly set.	X	X	X
Electrical Specifications	Fixed Voltage Reference (FVR) Accuracy	5.1	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X	X	X
Electrical Specifications	SMBus 2.0	5.2	The maximum VIL level changes when VDD is below 4.0V at 125°C.	X	X	
Electrical Specifications	NVM Access	5.3	NVM access on LF devices may not work at all specified voltage and temperature ranges.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: Oscillators

1.1 Register Reset Values

Upon any Power-on Reset (POR), the value in the OSTUNE register will be 0x20, which is the lowest frequency adjustment allowed.

Work around

On initial start-up or after any Power-on Reset, write a 0x00 value into the OSTUNE register, restoring the frequency adjustment back to the factory calibrated setting.

Affected Silicon Revisions

A3	A4	A6					
X							

1.2 32 MHz Clock

When the 32 MHz internal oscillator frequency is selected by writing '110' to either the RSTOSC[2:0] bits of Configuration Word 1 or the NOSC[2:0] bits of OSCCON1 and writing '0111' or '1xxx' to the HFFRQ[3:0] bits of OSCFRQ, the oscillator will fail to lock at 32 MHz and may become unstable.

Work around

1. To achieve a 32 MHz internal oscillator upon power-up or Reset, write '000' to the RSTOSC[2:0] bits of Configuration Word 1, which automatically selects the 32 MHz INTOSC with an internal 2xPLL, sets the HFFRQ[3:0] bits to '0110', and sets the NDIV[3:0] bits of OSCCON1 to '0000' (1:1 divider ratio).

2. To achieve a 32 MHz internal oscillator from an established clock source, write '000' to the NOSC[2:0] bits and '0000' to the NDIV[3:0] bits of OSCCON1, and write '0110' to the HFFRQ[3:0] bits of OSCFRQ.

HFFRQ[3:0]	Nominal Freq. (MHz) (NOSC = 110)	2xPLL Freq. (MHz) (NOSC = 000)
0000	1	Reserved
0001	2	
0010	Reserved	
0011	4	
0100	8	16
0101	12	24
0110	16	32
0111	Reserved	Reserved
1xxx	Reserved	Reserved

Affected Silicon Revisions

A3	A4	A6					
X							

1.3 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor may fail to trigger with the loss of the external clock signal when the 4x PLL is enabled. This includes all external clock modes, LP, XT, HS, ECL, ECM, and ECH.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X							

1.4 Status Flag

When switching from the Internal Oscillator with PLL enabled to an external oscillator with PLL enabled and the clock switch fails, the PLL ready (PLLR) bit of the OSCSTAT1 register is incorrectly cleared.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X							

2. Module: EUSART

2.1 Transmit

When the EUSART module is enabled (SPEN = 1) with the transmit function disabled (TXEN = 0), the TX assigned pin is driven low.

Work around

Load the desired logic level into the corresponding LATx register and assign the I/O function via the PPS output register.

Affected Silicon Revisions

A3	A4	A6					
X							

3. Module: Master Synchronous Serial Port (MSSP)

3.1 SPI Slave Data Corruption During Sleep

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master releases the $\overline{SS}$ line ($\overline{SS}$ goes high) before the device wakes from Sleep and updates SSPBUF, the received data will be lost.

Work around

Method 1: The SPI master must wait a minimum of parameter SP83 (1.5 T_{CY} + 40 nS) after the last SCK edge AND the additional wake-up time from Sleep (device dependent) before releasing the $\overline{SS}$ line.

Method 2: If both the master and slave devices have an available pin, once the slave has completed the transaction and BF or SSPIF is set, the slave could toggle an output to inform the master that the transaction is complete and that it is safe to release the $\overline{SS}$ line.

Affected Silicon Revisions

A3	A4	A6					
X							

3.2 SPI Slave Data Corruption During Sleep

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master enables $\overline{SS}$ ($\overline{SS}$ goes low) within 1 T_{CY} before Sleep is executed, the data written into the SSPBUF by the slave for transmission will remain in the SSPBUF, and the byte received by the slave will be completely discarded. The MSb of the data byte that is currently loaded into SSPBUF will be transmitted on each of the eight SCK clocks, resulting in either a 0x00 or 0xFF to be incorrectly transmitted. This issue typically occurs when the device wakes up from Sleep to process data and immediately goes back to Sleep during the next transmission.

Work around

The SPI Slave must wait a minimum of 2.25*T_{CY} from the time the $\overline{SS}$ line becomes active ($\overline{SS}$ goes low) before executing the Sleep command.

Affected Silicon Revisions

A3	A4	A6					
X							

3.3 WCOL Bit Improperly Set During Sleep

When the MSSP module is configured with either of the Slave modes listed below and Sleep is executed during transmission, the WCOL bit is erroneously set. Although the WCOL bit is set, it does not cause a break in transmission or reception.

Mode 1: SPI Slave mode with $\overline{SS}$ disabled (SSPM = 0101) and CKE = 0.

Mode 2: SPI Slave mode with $\overline{SS}$ enabled (SSPM = 0100) and $\overline{SS}$ is not set and then cleared before each consecutive transmission. This typically occurs during multiple byte transmissions in which the master does not release the $\overline{SS}$ line until all transmission has completed.

Work around

Method 1: The WCOL bit can be ignored since the issue does not interfere with MSSP hardware.

Method 2: Clear the SSPEN after each transaction, then set SSPEN before the next transaction.

Affected Silicon Revisions

A3	A4	A6					
X							

3.4 MSSP SPI Slave Mode

When operating in SPI Slave mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit shift register may become corrupted. The transmitted slave byte cannot be guaranteed to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:

- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read

Work around

Method 1 (Interrupt-based using $\overline{SS}$):
Connect the $\overline{SS}$ line to both the $\overline{SS}$ input and either an INT or IOC input pin.

1. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that $\overline{SS}=0$ when the interrupt occurs).
2. Load SSPBUF with the data to be transmitted.
3. Continue program execution.
4. When the Interrupt Service Routine (ISR) is invoked, do either of the following:
 - a) Add a delay that ensures the first SCK clock will be complete, or
 - b) Poll SSPSTAT.BF (while(BF==0)) and wait for the transmission/reception to complete.

Once either of these are complete, it is safe to return to program execution.

Method 2 (Bit polling-based using $\overline{SS}$):

1. Load SSPBUF with the data to be transmitted.
2. Poll the $\overline{SS}$ line and wait for the $\overline{SS}$ to go active (while(!PORTx. $\overline{SS}$ ==0)).
3. When $\overline{SS}$ is active ($\overline{SS}$ ==0), do either of the following:
 - a) Add a delay that ensures the first SCK clock will be complete, or
 - b) Poll SSPSTAT.BF (while(BF==0)), and wait for the transmission/reception to complete.

Once one of these two methods are complete, it is safe to return to program execution.

Method 3 ($\overline{SS}$ not available):

1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF==0)), and wait for the transmission/reception to complete.

Affected Silicon Revisions

A3	A4	A6					
X	X	X					

4. Module: Nonvolatile Memory (NVM) Control

4.1 NVMREG Access

When performing self-writes through NVMREG access on PIC16LF18313/18323 devices with VDD below 2.2V and at temperature of -40°C, the write operation may not work. This applies to both Program Flash Memory and EEPROM writes.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X	X						

4.2 NVM WRERR

If a Reset occurs while a self-write operation is in progress, the Write Error (WRERR) bit is set. If the user clears the WRERR bit and another Reset occurs even though no self-write is in progress, the WRERR bit will be incorrectly set again since the internal write latch has not been cleared.

Work around

A successful write operation will clear the WRERR condition.

Affected Silicon Revisions

A3	A4	A6					
X	X	X					

5. Module: Electrical Specifications

5.1 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A3	A4	A6					
X	X	X					

5.2. SMBus 2.0 ViL Level

At 125°C when the VDD voltage level supplied to the device is 4.0V and above, the maximum SMBus 2.0 voltage level for the ViL parameter is 0.8V. When VDD drops below 4.0V, the maximum SMBus voltage level for ViL drops to 0.7V. This issue applies to extended temperature devices only.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X	X						

5.3. Nonvolatile Memory

Nonvolatile memory (NVM) access on LF devices may not work when operating at temperatures between -40°C and +25°C and VDD levels below 2.0V.

Work around

None.

Affected Silicon Revisions

A3	A4	A6					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001799F):

Note: Corrections are shown in bold . Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev H Document (9/2019)

Updated Table 1: Silicon DEVREV Values. Removed items from Data Sheet Clarifications.

Rev G Document (01/2019)

Added two lines to Table 2. Added sections 4.2 and 5.3. Other minor corrections.

Data Sheet Clarifications: Added Table 35-6. Other minor corrections.

Rev F Document (01/2018)

Added Module 5.2: SMBus 2.0 VIL Level. Other minor corrections.

Rev E Document (07/2017)

Added Module 5: Electrical Specifications.

Data Sheet Clarifications: Removed Module 1: Comparator. Other minor corrections.

Rev D Document (01/2017)

Added Module 4: Nonvolatile Memory Control.

Data Sheet Clarifications:

Removed Module 1 through Module 7; Added new Module 1: Comparator.

Rev C Document (09/2016)

Data Sheet Clarifications:

Added new Module 6: Packaging Information.

Rev B Document (01/2016)

Added silicon revision A4 to Tables 1 and 2.

Rev A Document (10/2015)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Klear, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TempTrackr, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, Vite, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQR, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2015-2019, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-5094-8

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.



Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880-3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820