

PIC16(L)F178X Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16F1782 • PIC16LF1782
- PIC16F1783 • PIC16LF1783
- PIC16F1784 • PIC16LF1784
- PIC16F1786 • PIC16LF1786
- PIC16F1787 • PIC16LF1787
- PIC16F1788 • PIC16LF1788
- PIC16F1789 • PIC16LF1789

1.0 OVERVIEW

The device can be programmed using either the high-voltage In-Circuit Serial Programming™ (ICSP™) method or the low-voltage ICSP method.

1.1 Hardware Requirements

1.1.1 HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP mode, the device requires two programmable power supplies: one for VDD and one for the MCLR/VPP pin.

1.1.2 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP mode, the PIC16(L)F178X devices can be programmed using a single VDD source in the operating range. The MCLR/VPP pin does not have to be brought to a different voltage, but can instead be left at the normal operating voltage.

1.1.2.1 Single-Supply ICSP Programming

The LVP bit in Configuration Word 2 enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled) from the factory. The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the MCLR/VPP pin is raised to VIH. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

Note 1: The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying VIH to the MCLR/VPP pin.

2: While in Low-Voltage ICSP mode, MCLR is always enabled, regardless of the MCLRE bit, and the port pin can no longer be used as a general purpose input.

1.2 Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in Table 1-1.

TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING FOR PIC16(L)F178X

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
RE3/MCLR/VPP	Program/Verify mode	P(1)	Program Mode Select/Programming Power Supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to MCLR input. Since the MCLR is used for a level source, MCLR does not draw any significant current.

PIC16(L)F178X

2.0 DEVICE PINOUTS

The pin diagrams for the PIC16(L)F178X family are shown in [Figure 2-1](#) to [Figure 2-7](#). The pins that are required for programming are listed in [Table 1-1](#) and shown in bold lettering in the pin diagrams.

FIGURE 2-1: 28-PIN PDIP/SOIC/SSOP DIAGRAM FOR PIC16(L)F1782/3/6/8

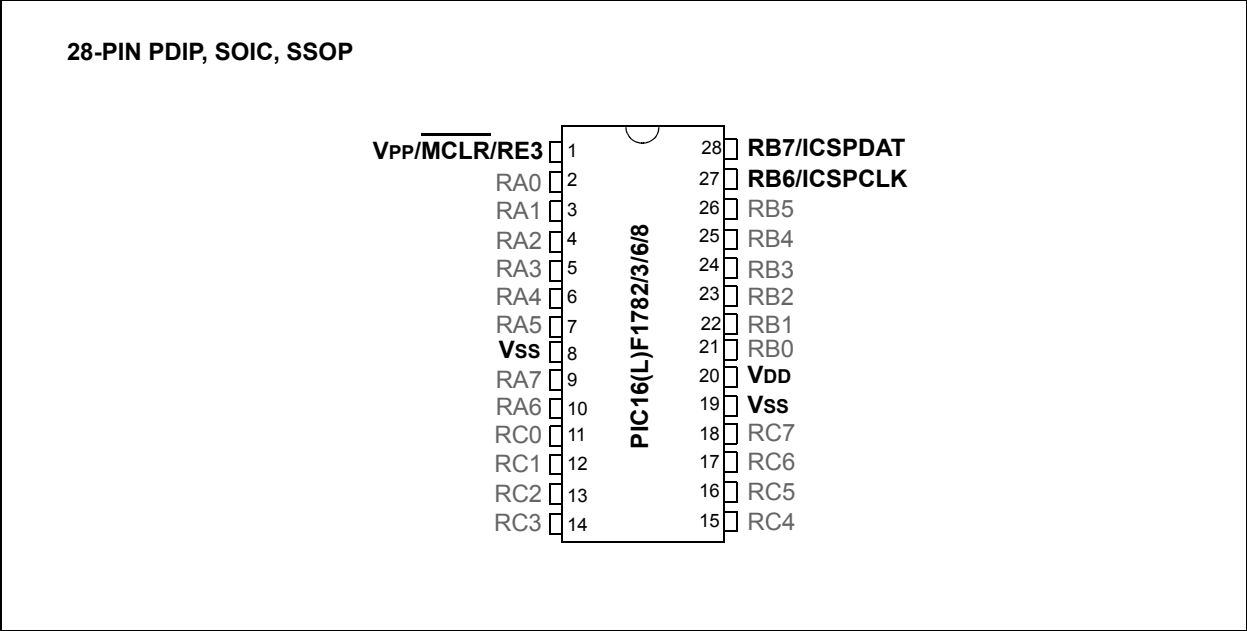


FIGURE 2-2: 28-PIN UQFN PACKAGE DIAGRAM FOR PIC16(L)F1782/1783

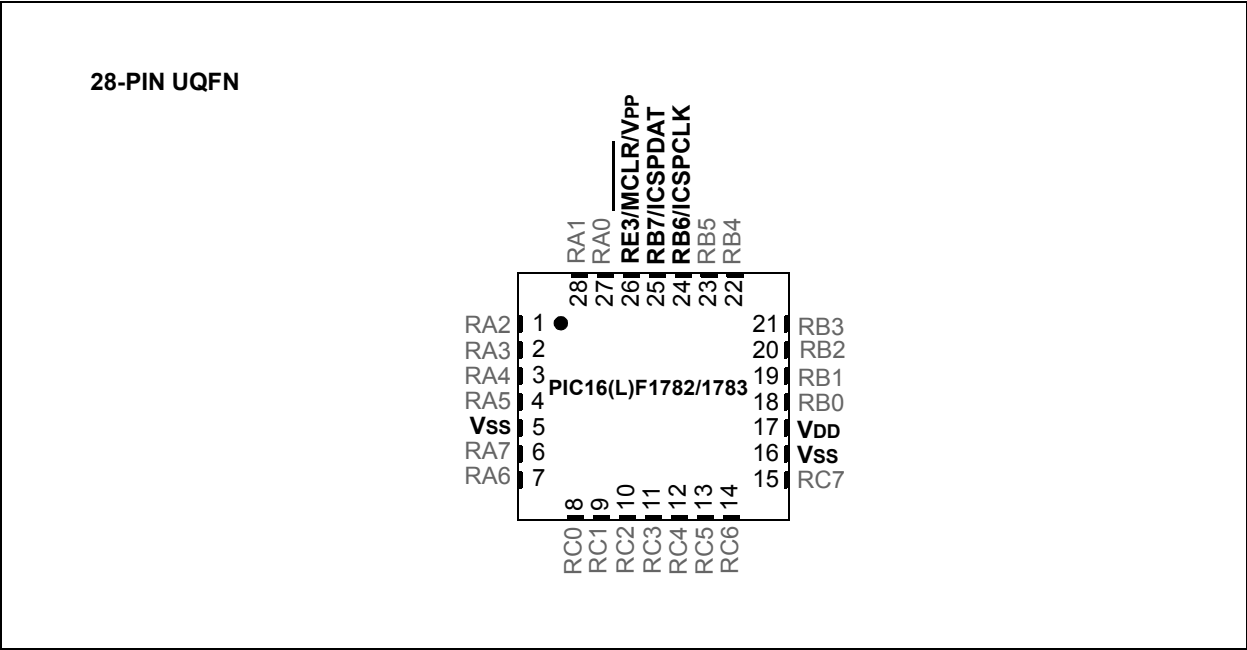


FIGURE 2-3: 28-PIN QFN PACKAGE DIAGRAM FOR PIC16(L)F1786/1788

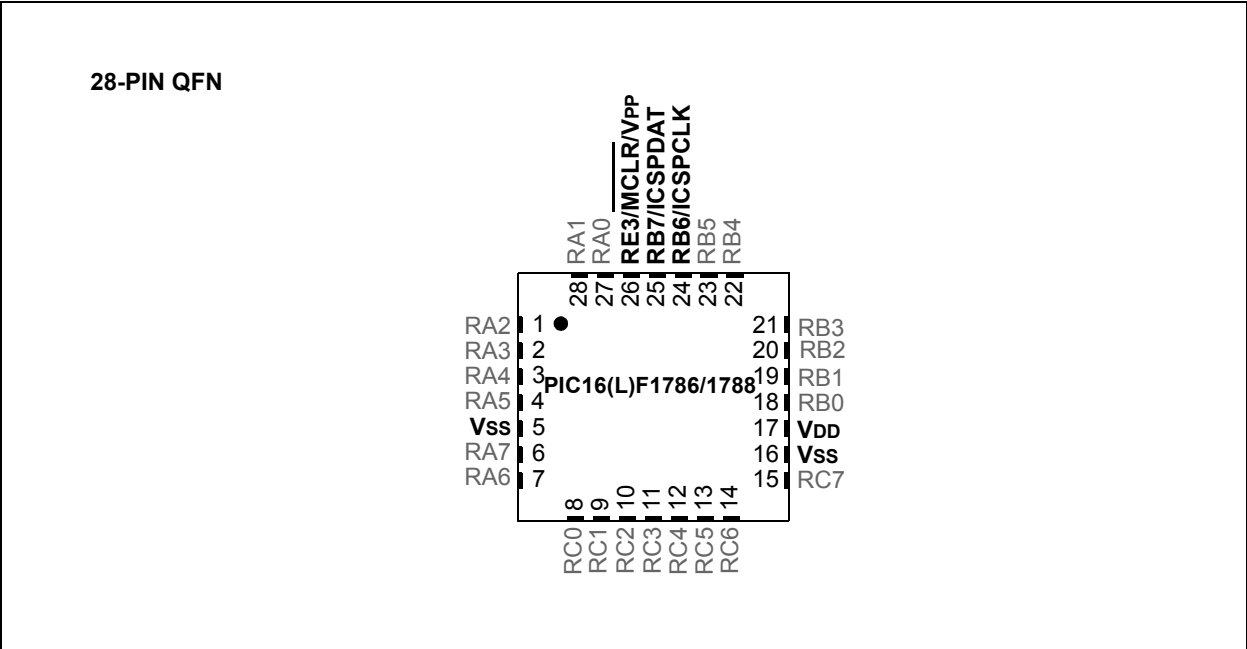
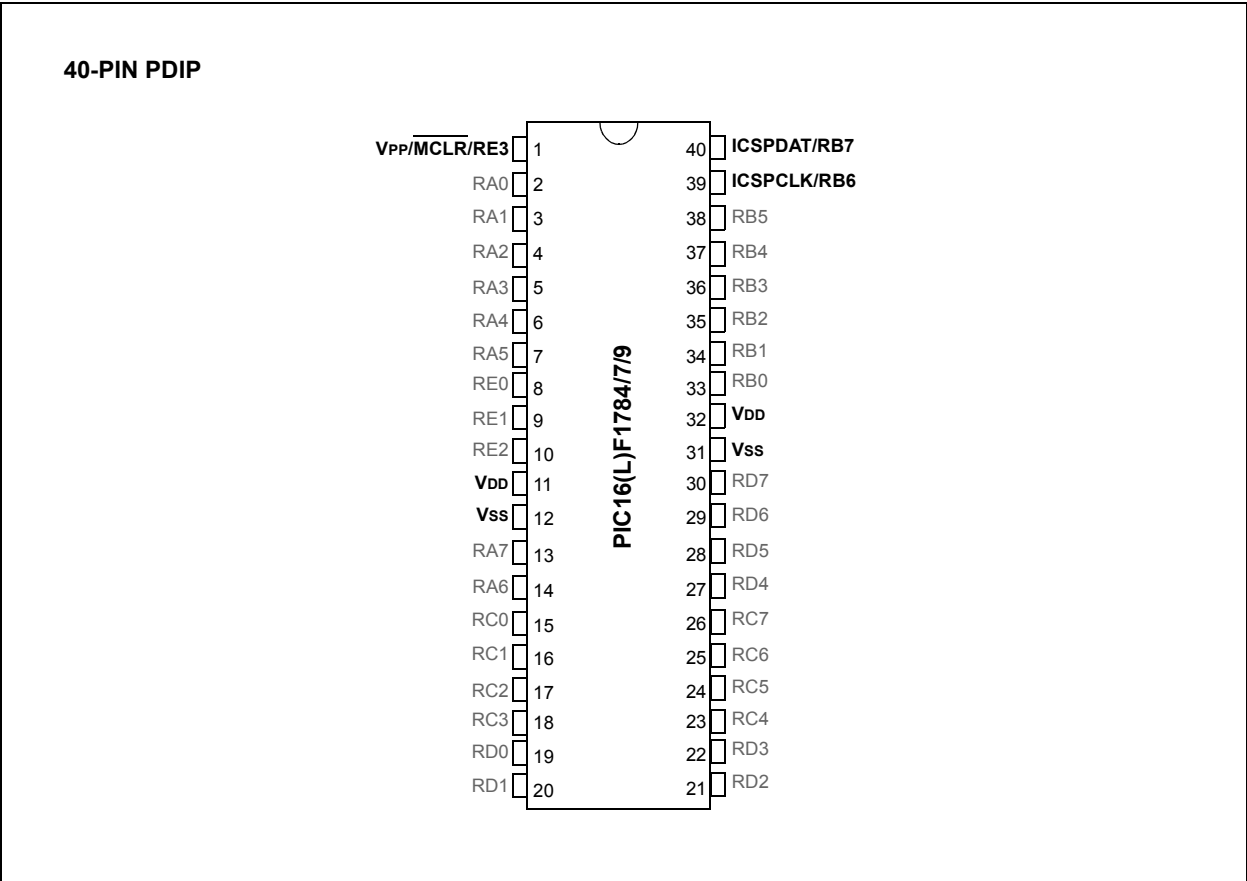


FIGURE 2-4: 40-PIN PDIP PACKAGE DIAGRAM FOR PIC16(L)F1784/7/9



PIC16(L)F178X

FIGURE 2-5: 40-PIN UQFN PACKAGE DIAGRAM FOR PIC16(L)F1784/7/9

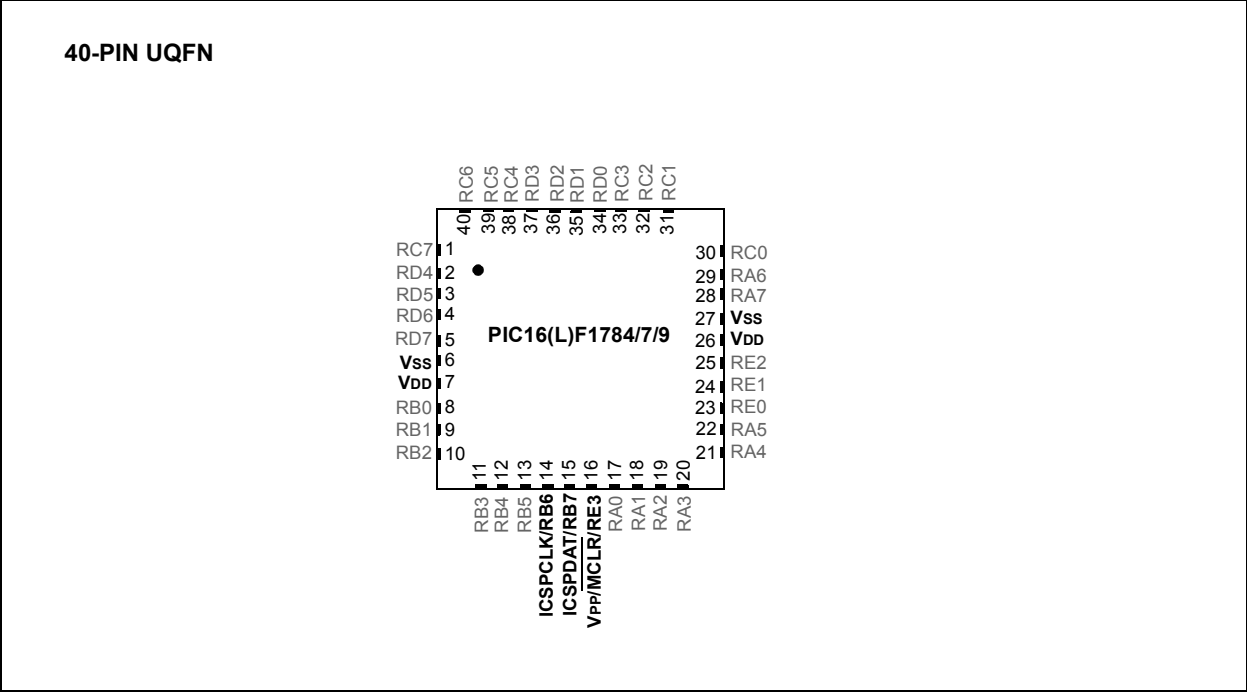


FIGURE 2-6: 44-PIN QFN PACKAGE DIAGRAM FOR PIC16(L)F1784/7/9

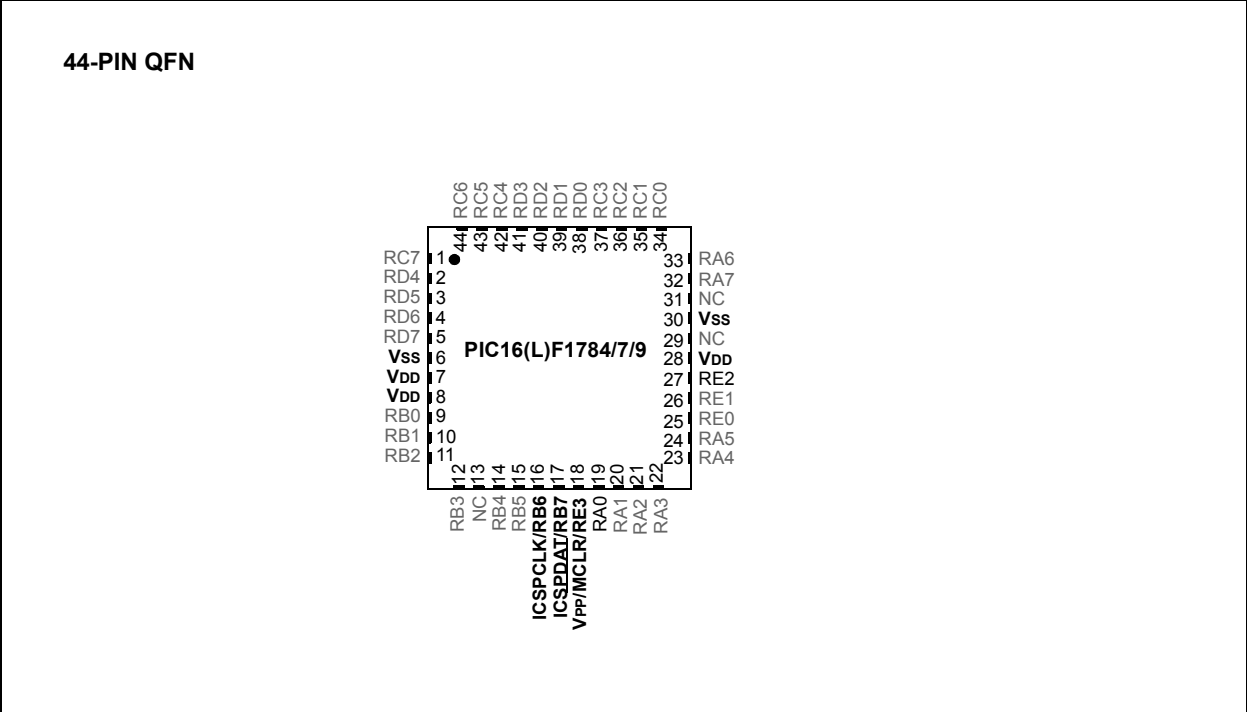
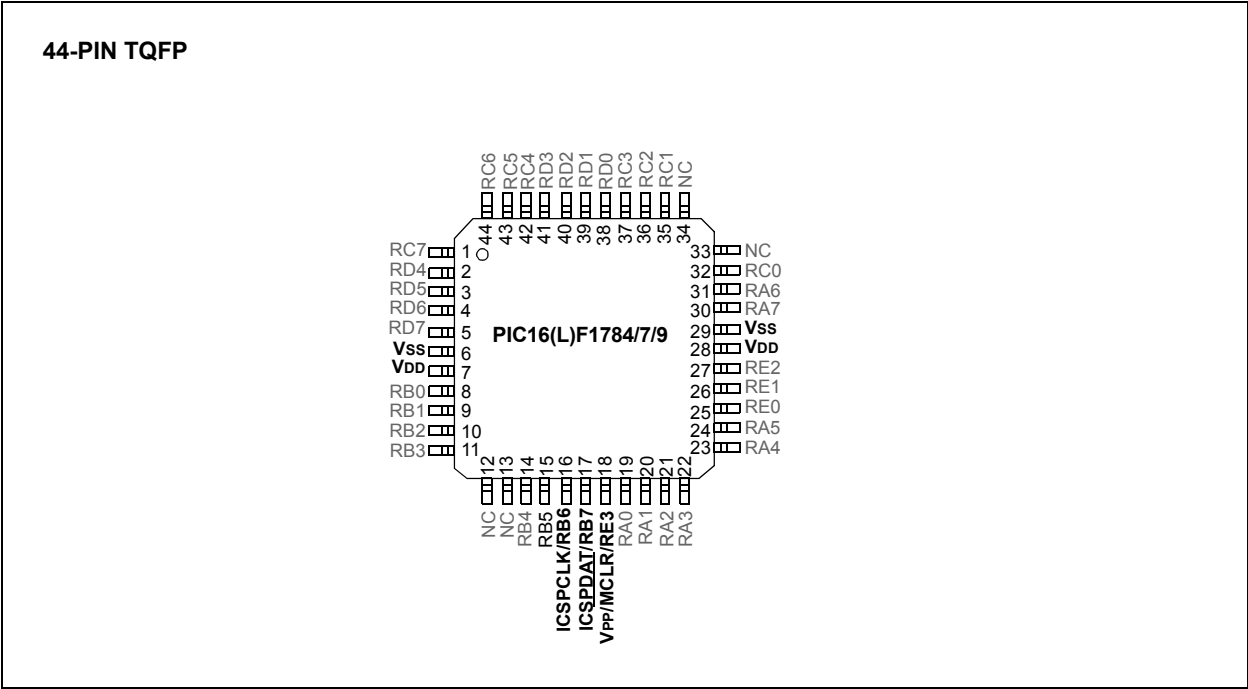


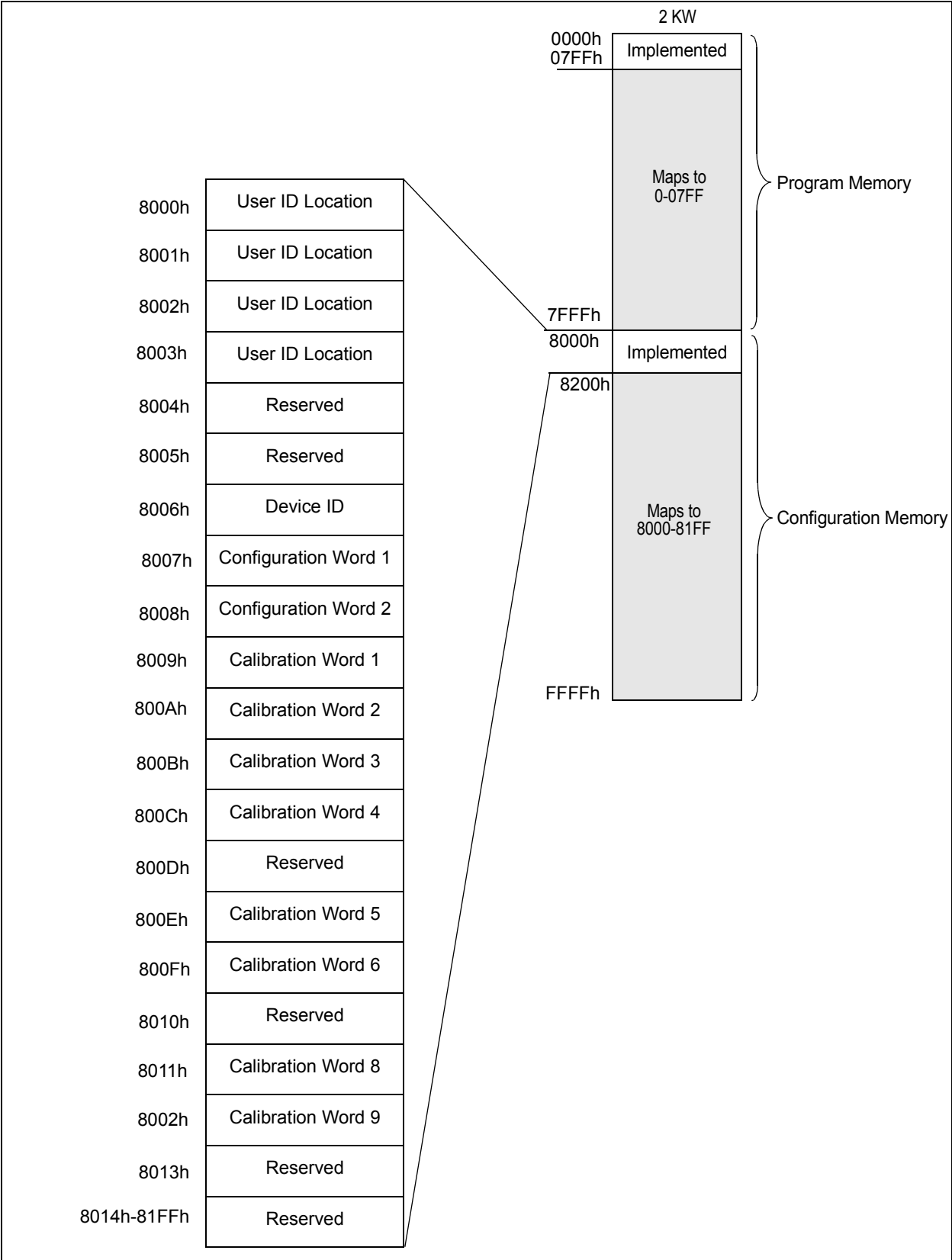
FIGURE 2-7: 44-PIN TQFP PACKAGE DIAGRAM FOR PIC16(L)F1784/7/9



3.0 MEMORY MAP

The memory is broken into two sections: program memory and configuration memory. Only the size of the program memory changes between devices, the configuration memory remains the same.

FIGURE 3-1: PIC16(L)F1782 PROGRAM MEMORY MAPPING



PIC16(L)F178X

FIGURE 3-2: PIC16(L)F1783/4 PROGRAM MEMORY MAPPING

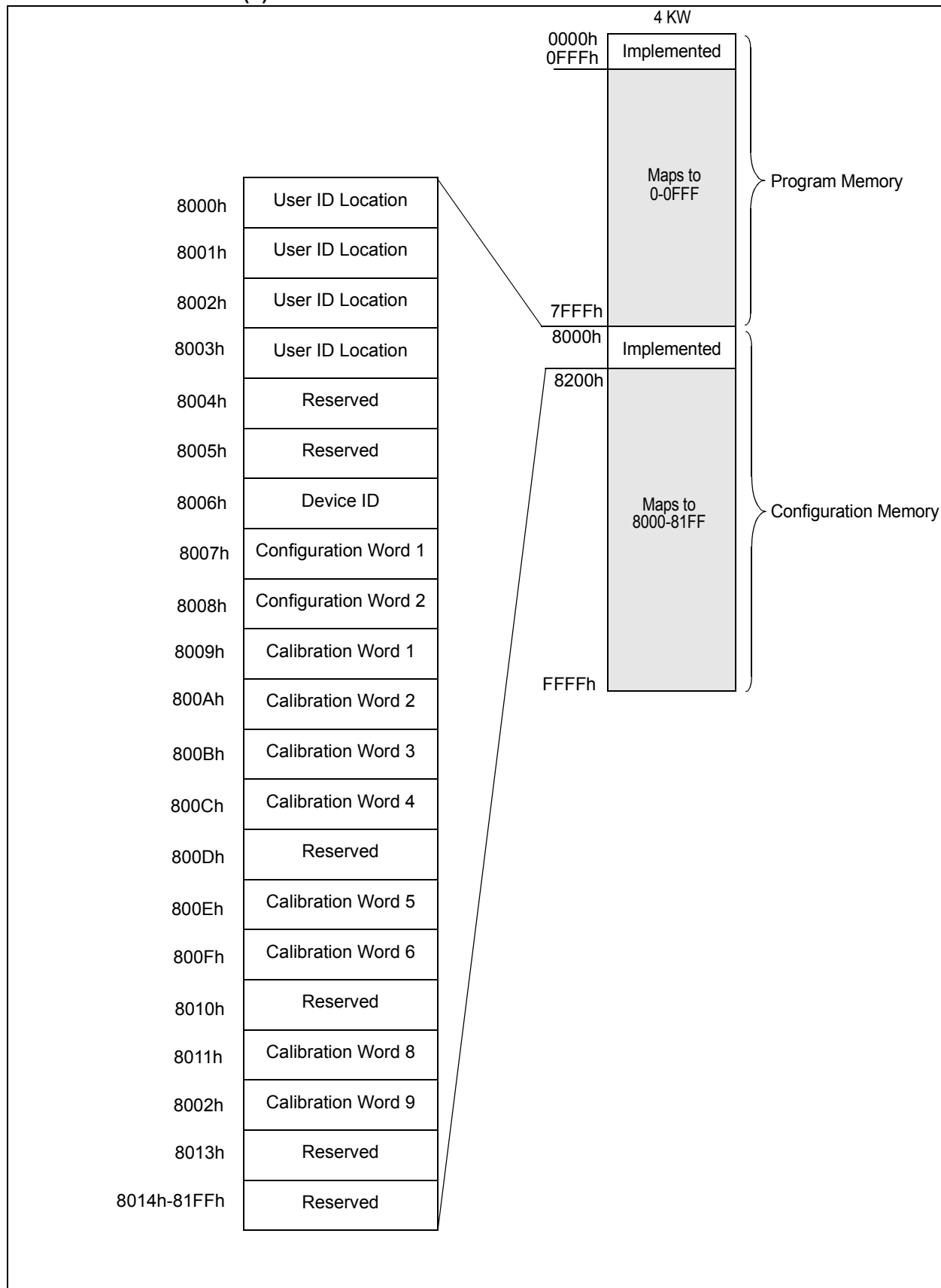
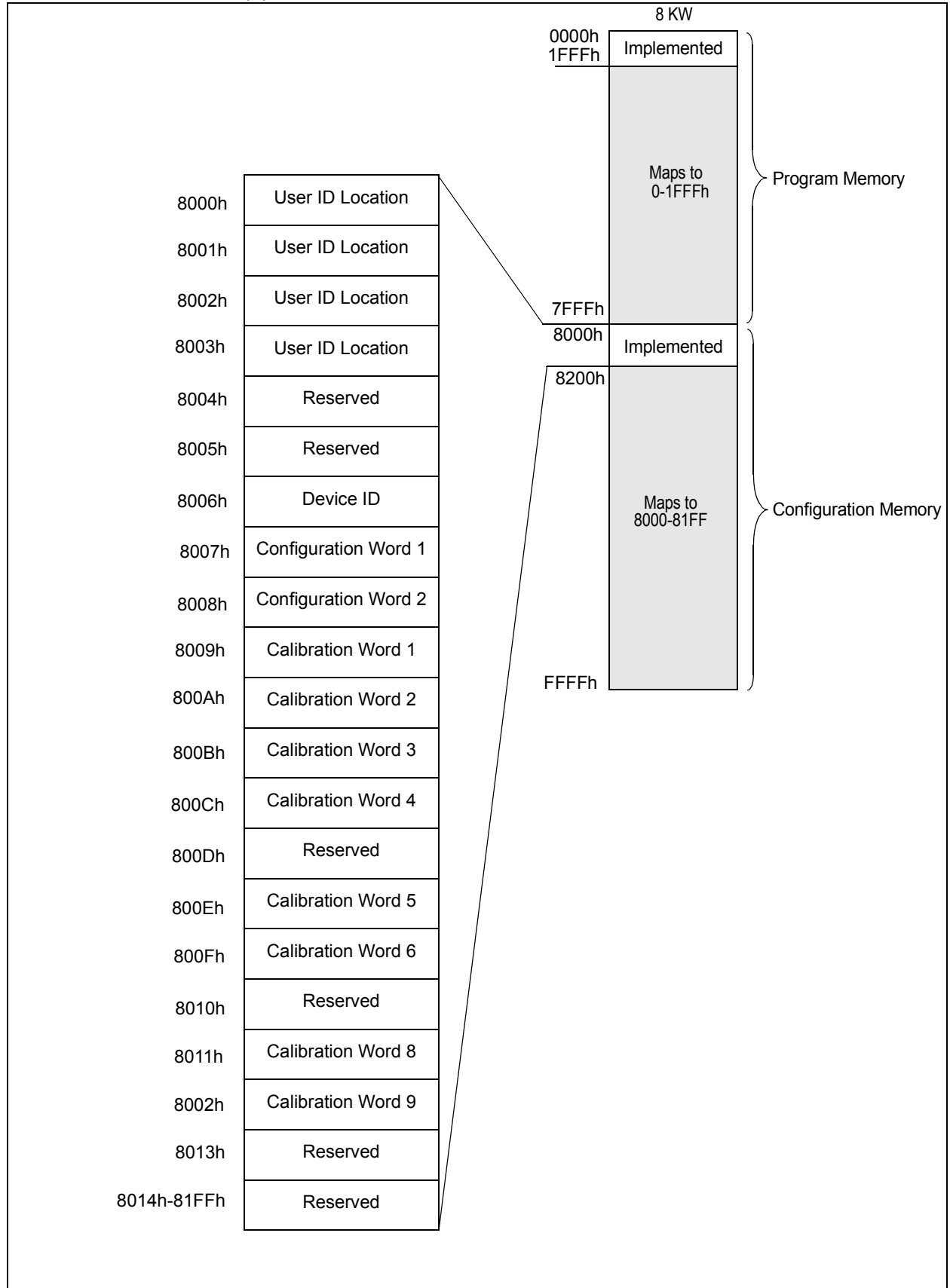
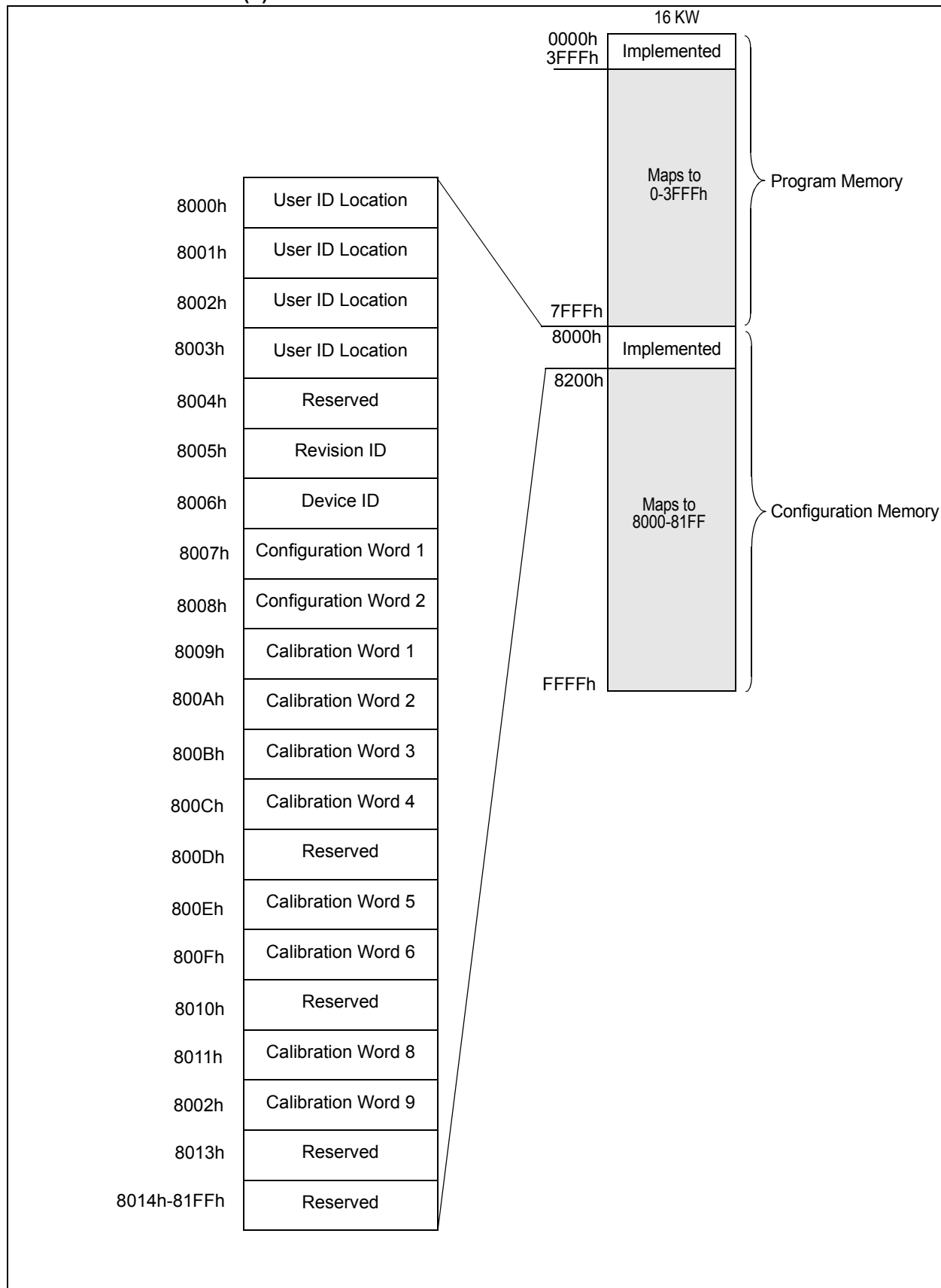


FIGURE 3-3: PIC16(L)F1786/7 PROGRAM MEMORY MAPPING



PIC16(L)F178X

FIGURE 3-4: PIC16(L)F1788/9 PROGRAM MEMORY MAPPING



PIC16(L)F178X

3.2.2 DEVICE/REVISION ID – PIC16(L)F1788/9 DEVICES

The 14-bit device ID word is located at 8006h and the 14-bit revision ID is located at 8005h. These locations are read-only and cannot be erased or modified.

REGISTER 3-2: **DEVICEID: DEVICE ID REGISTER**^{(1),(2)}

R	R	R	R	R	R
DEV<13:8>					
bit 13			bit 8		

R	R	R	R	R	R	R	R
DEV<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

'0' = Bit is cleared

'1' = Bit is set

x = Bit is unknown

bit 13-0 **DEV<13:0>**: Device ID bits

Refer to [Table 3-2](#) to determine what these bits will read on which device. A value of 3FFFh is invalid.

Note 1: This location cannot be written.

2: PIC16(L)F1788/9 devices only.

REGISTER 3-3: **REVISIONID: REVISION ID REGISTER**^{(1),(2)}

R	R	R	R	R	R
REV<13:8>					
bit 13			bit 8		

R	R	R	R	R	R	R	R
REV<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

'0' = Bit is cleared

'1' = Bit is set

x = Bit is unknown

bit 13-0 **REV<13:0>**: Revision ID bits

These bits are used to identify the device revision.

Note 1: This location cannot be written.

2: PIC16(L)F1788/9 devices only.

TABLE 3-2: DEVICE ID VALUES (PIC16(L)F1788/9)

DEVICE	Device ID	Revision ID
PIC16F1788	302Bh	2xxxh
PIC16LF1788	302Dh	2xxxh
PIC16F1789	302Ah	2xxxh
PIC16LF1789	302Ch	2xxxh

3.3 Configuration Words

The device has two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

The internal calibration values are factory calibrated and stored in the Calibration Word locations. See [Figure 3-1](#), [Figure 3-2](#), [Figure 3-3](#) and [Figure 3-4](#) for address information.

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

PIC16(L)F178X

REGISTER 3-4: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
FCMEN	IESO	CLKOUTEN	BOREN<1:0>	CPD	
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	MCLRE	PWRTEN	WDTE<1:0>		FOSC<2:0>		
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '1'
 '0' = Bit is cleared '1' = Bit is set n = Value when blank or after Bulk Erase

- bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
 1 = Fail-Safe Clock Monitor is enabled
 0 = Fail-Safe Clock Monitor is disabled
- bit 12 **IESO:** Internal External Switchover bit
 1 = Internal/External Switchover mode is enabled
 0 = Internal/External Switchover mode is disabled
- bit 11 **CLKOUTEN:** Clock Out Enable bit
 1 = CLKOUT function is disabled. I/O or oscillator function on RA6/CLKOUT
 0 = CLKOUT function is enabled on RA6/CLKOUT
- bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits⁽¹⁾
 11 = BOR enabled
 10 = BOR enabled during operation and disabled in Sleep
 01 = BOR controlled by SBOREN bit of the PCON register
 00 = BOR disabled
- bit 8 **CPD:** Data Code Protection bit⁽²⁾
 1 = Data memory code protection is disabled
 0 = Data memory code protection is enabled
- bit 7 **CP:** Code Protection bit⁽³⁾
 1 = Program memory code protection is disabled
 0 = Program memory code protection is enabled
- bit 6 **MCLRE:** MCLR/VPP Pin Function Select bit
 If LVP bit = 1:
 This bit is ignored.
 If LVP bit = 0:
 1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
 0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of port pin's WPU control bit.
- bit 5 **PWRTEN:** Power-up Timer Enable bit⁽¹⁾
 1 = PWRT disabled
 0 = PWRT enabled
- bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
 11 = WDT enabled
 10 = WDT enabled while running and disabled in Sleep
 01 = WDT controlled by the SWDTEN bit in the WDTCON register
 00 = WDT disabled

- Note 1:** Enabling Brown-out Reset does not automatically enable Power-up Timer.
Note 2: The entire data EEPROM will be erased when the code protection is turned off during an erase.
Note 3: The entire program memory will be erased when the code protection is turned off.

REGISTER 3-4: CONFIGURATION WORD 1 (CONTINUED)

bit 2-0 **FOSC<2:0>**: Oscillator Selection bits

111 = ECH: External Clock, High-Power mode: CLKIN on RA7/OSC1/CLKIN

110 = ECM: External Clock, Medium-Power mode: CLKIN on RA7/OSC1/CLKIN

101 = ECL: External Clock, Low-Power mode: CLKIN on RA7/OSC1/CLKIN

100 = INTOSC oscillator: I/O function on RA7/OSC1/CLKIN

011 = EXTRC oscillator: RC function on RA7/OSC1/CLKIN

010 = HS oscillator: High-speed crystal/resonator on RA6/OSC2/CLKOUT pin and RA7/OSC1/CLKIN

001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT pin and RA7/OSC1/CLKIN

000 = LP oscillator: Low-power crystal on RA6/OSC2/CLKOUT pin and RA7/OSC1/CLKIN

- Note 1:** Enabling Brown-out Reset does not automatically enable Power-up Timer.
- 2:** The entire data EEPROM will be erased when the code protection is turned off during an erase.
- 3:** The entire program memory will be erased when the code protection is turned off.

PIC16(L)F178X

REGISTER 3-5: CONFIGURATION WORD 2

R/P-1 ⁽¹⁾	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
LVP	DEBUG	LPBOR	BORV	STVREN	PLLEN
bit 13					bit 8

U-1	U-1	R/P-1	U-1	U-1	U-1	R/P-1	R/P-1
—	—	VCAPEN	—	—	—	WRT<1:0>	
bit 7							bit 0

Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '1'

'0' = Bit is cleared

'1' = Bit is set

n = Value when blank or after Bulk Erase

- bit 13 **LVP:** Low-Voltage Programming Enable bit⁽¹⁾
 1 = Low-voltage programming enabled
 0 = MCLR/VPP must be used for programming high voltage
- bit 12 **DEBUG:** In-Circuit Debugger Mode bit
 1 = In-Circuit Debugger disabled, RB6/ICSPCLK and RB7/ICSPDAT are general purpose I/O pins
 0 = In-Circuit Debugger enabled, RB6/ICSPCLK and RB7/ICSPDAT are dedicated to the debugger
- bit 11 **LPBOR:** Low-Power Brown-out Reset Enable bit
 1 = Low-Power Brown-out is disabled
 0 = Low-Power Brown-out is enabled
- bit 10 **BORV:** Brown-out Reset Voltage Selection bit
 1 = Brown-out Reset voltage, low trip point selected
 0 = Brown-out Reset voltage, high trip point selected
- bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
 1 = Stack Overflow or Underflow will cause a Reset
 0 = Stack Overflow or Underflow will not cause a Reset
- bit 8 **PLLEN:** PLL Enable bit
 1 = 4xPLL enabled
 0 = 4xPLL disabled
- bit 7-6 **Unimplemented:** Read as '1'
- bit 5 **VCAPEN:** Voltage Regulator Capacitor Enable for RA6 bits⁽²⁾
 1 = VCAP functionality is disabled on RA6. (VDDCORE is not connected to the pad)
 0 = VCAP functionality is enabled on RA6. (VDDCORE is connected to the pad)
- bit 4-2 **Unimplemented:** Read as '1'

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.

2: This bit is implemented on the LF devices only; otherwise, it is unimplemented and reads as '1'.

REGISTER 3-5: CONFIGURATION WORD 2 (CONTINUED)

bit 1-0

WRT<1:0>: Flash Memory Self-Write Protection bits

2 kW Flash memory: PIC16(L)F1782:

11 = Write protection off

10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control

01 = 000h to 3FFh write-protected, 400h to 7FFh may be modified by PMCON control

00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control

4 kW Flash memory: PIC16(L)F1783/1784:

11 = Write protection off

10 = 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control

01 = 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control

00 = 000h to FFFh write-protected, no addresses may be modified by PMCON control

8 kW Flash memory: PIC16(L)F1786/1787:

11 = Write protection off

10 = 000h to 1FFh write-protected, 200h to 1FFFh may be modified by PMCON control

01 = 000h to FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control

00 = 000h to 1FFFh write-protected, no addresses may be modified by PMCON control

16 kW Flash memory: PIC16(L)F1788/1789:

11 = Write protection off

10 = 000h to 1FFh write-protected, 200h to 3FFFh may be modified by PMCON control

01 = 000h to 1FFFh write-protected, 2000h to 3FFFh may be modified by PMCON control

00 = 000h to 3FFFh write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.

2: This bit is implemented on the LF devices only; otherwise, it is unimplemented and reads as '1'.

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to V_{IH} .
3. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Word has MCLR disabled ($\text{MCLRE} = 0$), the power-up time is disabled ($\text{PWRT} = 0$), the internal oscillator is selected ($\text{FOSC} = 100$), and RB6 and RB7 are driven by the user application, the device will execute code. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in [Figure 8-2](#).

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to V_{IH} .

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in [Figure 8-1](#).

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (V_{IL}). See [Figures 8-3](#) and [8-4](#).

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the PIC16(L)F178X devices to be programmed using VDD only, without high voltage. When the LVP bit of the Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to V_{IL} .
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see [Figures 8-8](#) and [8-9](#).

Exiting Program/Verify mode is done by no longer driving $\overline{\text{MCLR}}$ to V_{IL} . See [Figures 8-8](#) and [8-9](#).

Note: To enter LVP mode, the LSb of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

4.3 Program/Verify Commands

These devices implement 13 programming commands, each six bits in length. The commands are summarized in [Table 4-1](#).

Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING FOR PIC16(L)F178X

Command	Mapping							Data/Note
	Binary (MSb ... LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data For Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Load Data For Data Memory	x	0	0	0	1	1	03h	0, data (8), zero (6), 0
Read Data From Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Read Data From Data Memory	x	0	0	1	0	1	05h	0, data (8), zero (6), 0
Increment Address	x	0	0	1	1	0	06h	—
Reset Address	x	1	0	1	1	0	16h	—
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Externally Timed Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Bulk Erase Data Memory	x	0	1	0	1	1	0Bh	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

PIC16(L)F178X

4.3.1 LOAD CONFIGURATION

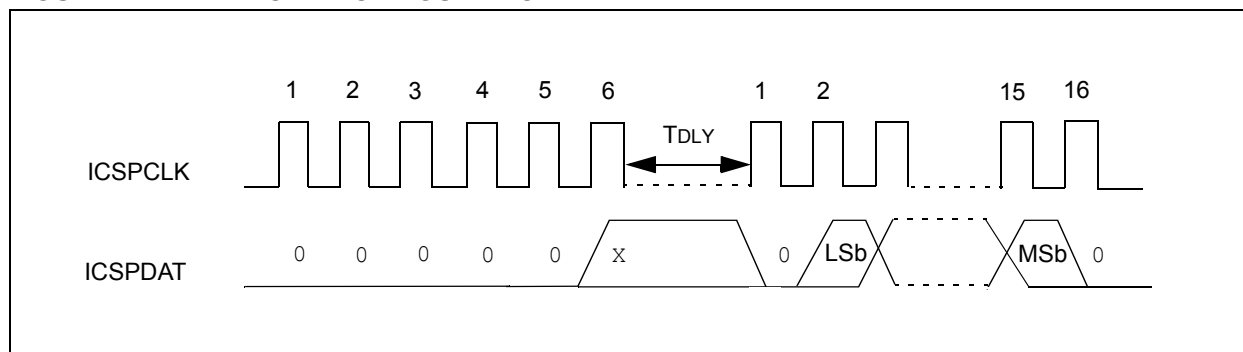
The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see [Figure 4-1](#)).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

Note: Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

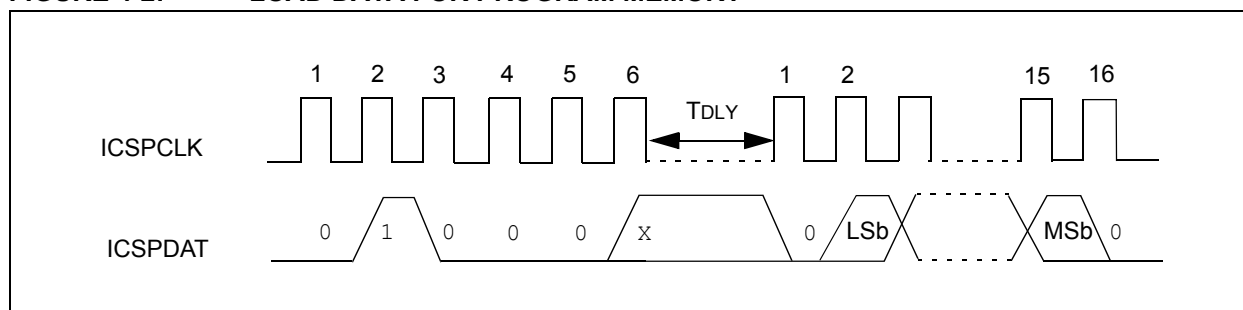
FIGURE 4-1: LOAD CONFIGURATION



4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see [Figure 4-2](#)).

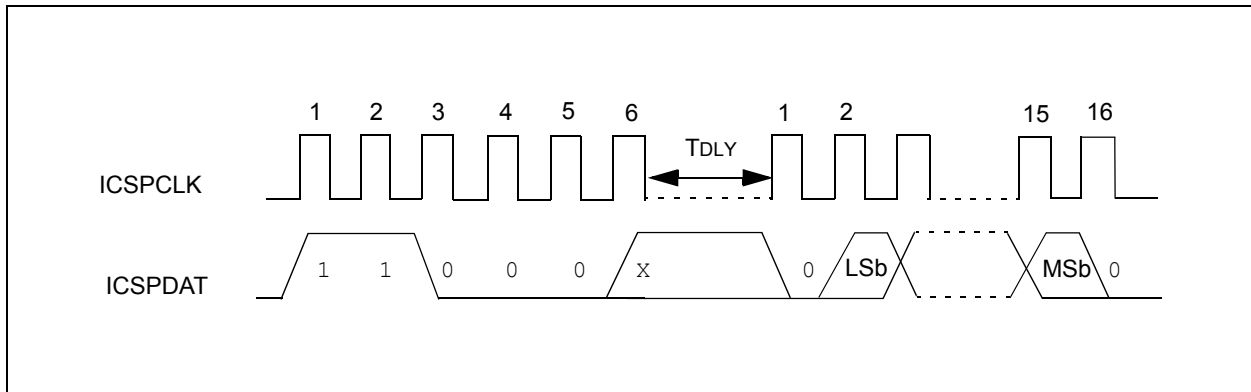
FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



4.3.3 LOAD DATA FOR DATA MEMORY

The Load Data for Data Memory command will load a 14-bit “data word” when 16 cycles are applied. However, the data memory is only eight bits wide and thus, only the first eight bits of data after the Start bit will be programmed into the data memory. It is still necessary to cycle the clock the full 16 cycles in order to allow the internal circuitry to reset properly (see [Figure 4-3](#)).

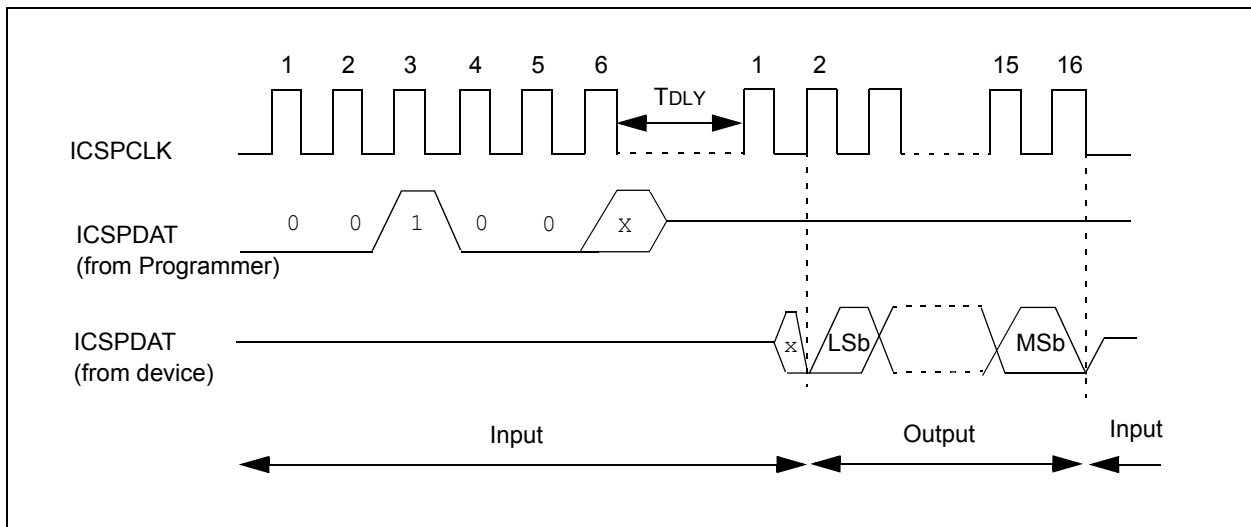
FIGURE 4-3: LOAD DATA FOR DATA MEMORY COMMAND



4.3.4 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see [Figure 4-4](#)).

FIGURE 4-4: READ DATA FROM PROGRAM MEMORY



The Read Data from Data Memory command will transmit data bits out of the data memory starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the second rising edge, and it will revert to Input mode (high-impedance) after the 16th rising edge. The data memory is eight bits wide, and therefore, only the first eight bits that are output are actual data. If the data memory is code-protected, the data is read as all zeros. A timing diagram of this command is shown in [Figure 4-5](#).

The diagram illustrates the timing relationship between the ICSPCLK, ICSPDAT (from Programmer), and ICSPDAT (from device) signals. The ICSPCLK signal is a periodic clock. The ICSPDAT (from Programmer) signal shows the data being sent to the device, with bits 1 through 6, followed by a delay (TDLY), and then bits 1 through 2, followed by a delay, and then bits 15 and 16. The ICSPDAT (from device) signal shows the data being received from the device, with bits 1 through 6, followed by a delay, and then bits 1 through 2, followed by a delay, and then bits 15 and 16. The diagram is divided into three sections: Input, Output, and Input, indicating the direction of data flow.

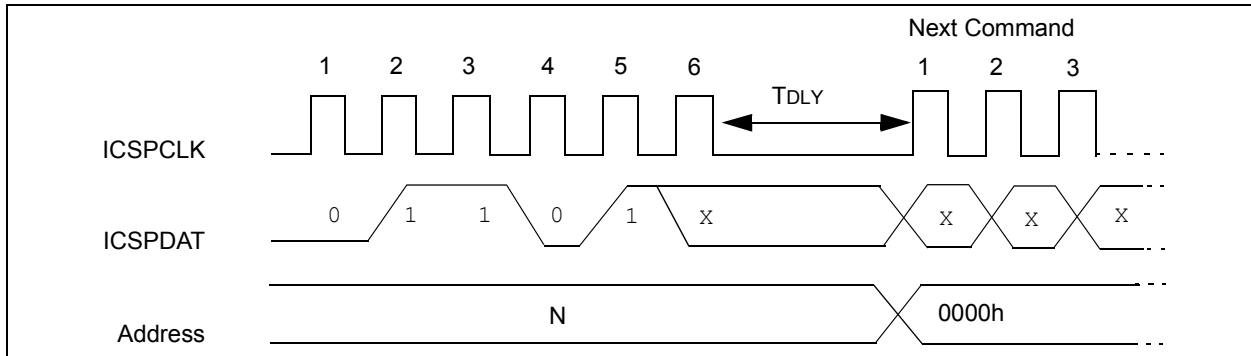
The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it.

The diagram illustrates the timing of three signals: ICSPCLK, ICSPDAT, and Address. The ICSPCLK signal is a periodic square wave. The ICSPDAT signal is a bus that carries data during the first six clock cycles (labeled 1 to 6) and then enters a high-impedance state (X) for the next three clock cycles (labeled 1 to 3). The Address signal is a bus that carries the address during the first six clock cycles and then increments by one (Address + 1) for the next three clock cycles. A delay period (TDLY) is indicated between the sixth and seventh clock cycles.

4.3.7 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory.

FIGURE 4-7: RESET ADDRESS



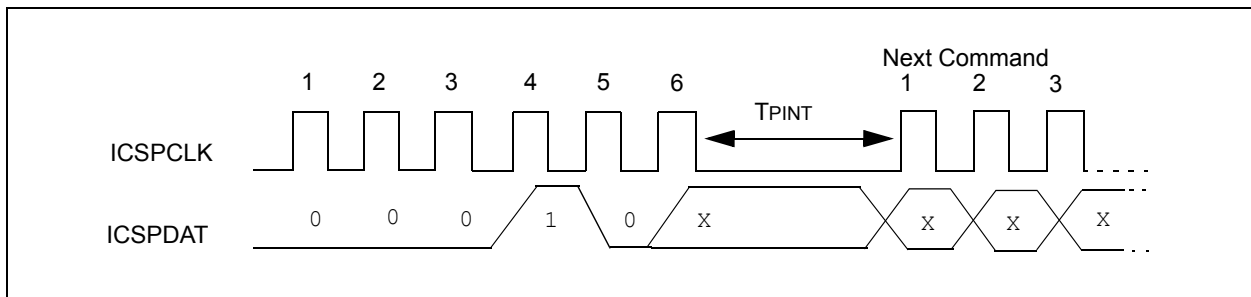
4.3.8 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, TPINT, for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed. However, the EEPROM memory address that is being programmed is erased prior to being programmed with internally timed programming.

FIGURE 4-8: BEGIN INTERNALLY TIMED PROGRAMMING



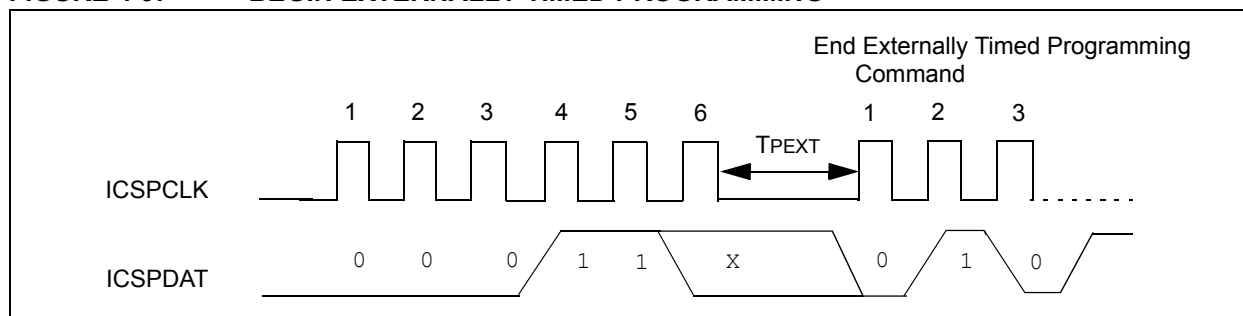
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4.3.9 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration, Load Data for Program Memory or Load Data for Data Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming, the End Externally Timed Programming command must be sent in the specified time window defined by T_{PEXT} . No internal erase is performed for the data EEPROM, therefore, the device should be erased prior to executing this command (see [Figure 4-9](#)).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 4-9: BEGIN EXTERNALLY TIMED PROGRAMMING

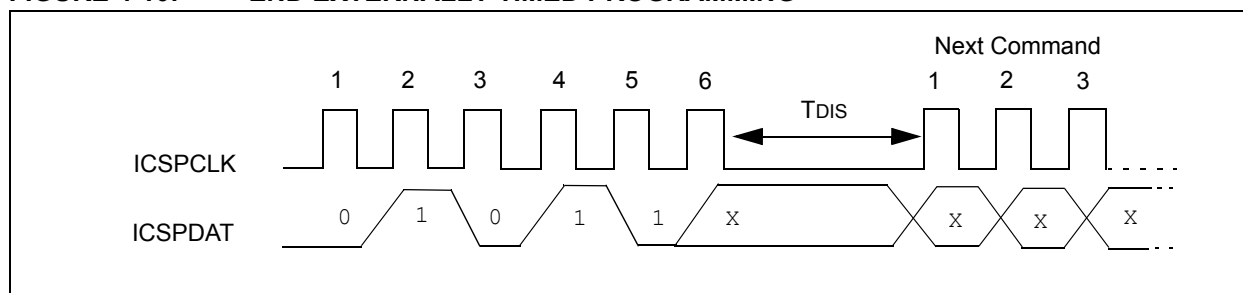


4.3.10 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by T_{PEXT} after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (T_{DIS}) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see [Figure 4-10](#)).

FIGURE 4-10: END EXTERNALLY TIMED PROGRAMMING



4.3.11 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:

- Program Memory is erased
- Configuration Words are erased
- If $\overline{\text{CPD}} = 0$, Data Memory is erased

Address 8000h-8008h:

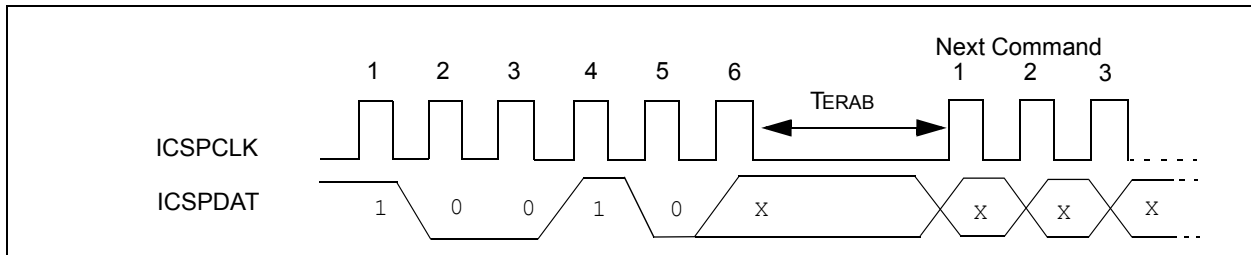
- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased
- If $\overline{\text{CPD}} = 0$, Data Memory is erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command the erase will not complete until the time interval, TERAB , has expired.

Note: The code protection Configuration bit (CP) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-11: BULK ERASE PROGRAM MEMORY



4.3.12 BULK ERASE DATA MEMORY

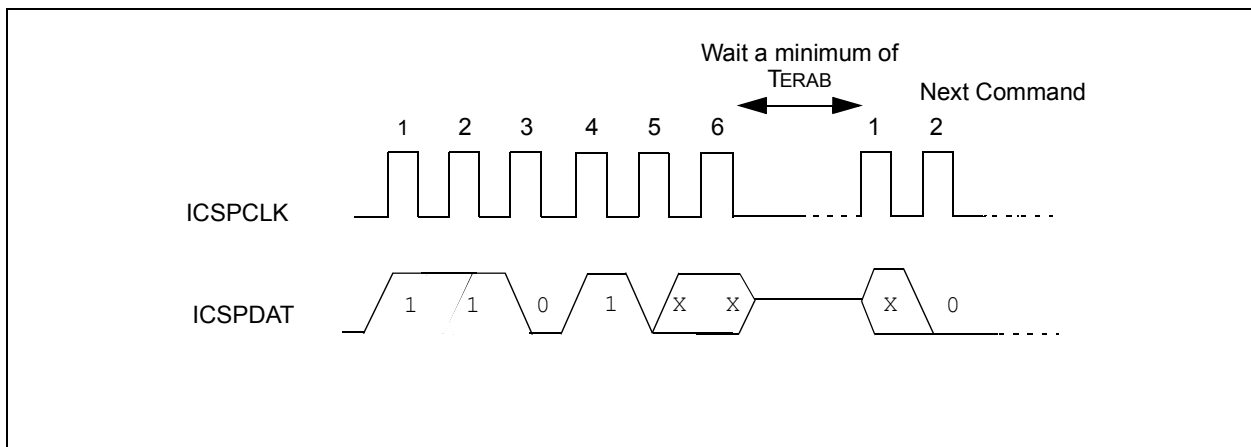
To perform an erase of the data memory, after a Bulk Erase Data Memory command, wait a minimum of TERAB to complete Bulk Erase.

To erase data memory when data code-protect is active ($\overline{\text{CPD}} = 0$), the Bulk Erase Program Memory command should be used.

After receiving the Bulk Erase Data Memory command, the erase will not complete until the time interval, TERAB , has expired.

Note: Data memory will not erase if code-protected ($\overline{\text{CPD}} = 0$).

FIGURE 4-12: BULK ERASE DATA MEMORY COMMAND



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4.3.13 ROW ERASE PROGRAM MEMORY

The Row Erase Program Memory command will erase an individual row. Refer to [Table 4-2](#) for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected, the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h the Row Erase Program Memory command will only erase the user ID locations regardless of the setting of the $\overline{CP}$ Configuration bit.

After receiving the Row Erase Program Memory command the erase will not complete until the time interval, T_{ERAR} , has expired.

FIGURE 4-13: ROW ERASE PROGRAM MEMORY

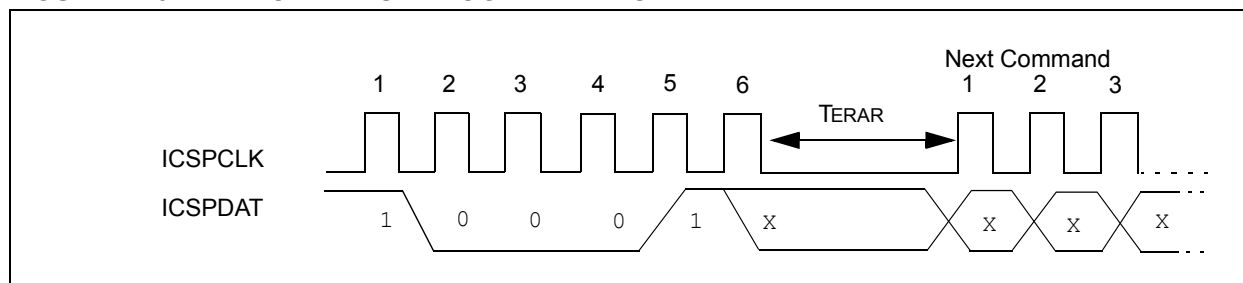


TABLE 4-2: PROGRAMMING ROW AND LATCH SIZES

Devices	PC	Erase Row Size (Number of 14-bit Memory Words)	Write Row Size (Number of 14-bit Latches)
PIC16F1782	<15:5>	32	32
PIC16F1783			
PIC16F1784			
PIC16F1786			
PIC16F1787			
PIC16F1788			
PIC16F1789			
PIC16LF1782			
PIC16LF1783			
PIC16LF1784			
PIC16LF1786			
PIC16LF1787			
PIC16LF1788			
PIC16LF1789			

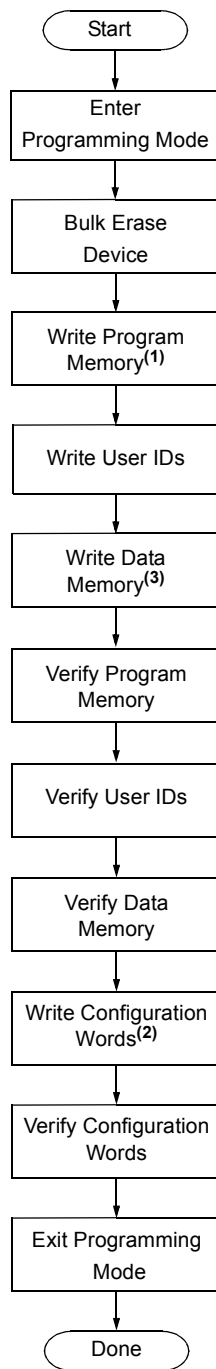
5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to [Table 4-2](#) for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PS address bits indicated in [Table 4-2](#) at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which memory row is written. Writes cannot cross a physical row boundary. For example, attempting to write from address 0002h-0021h in a 32-latch device will result in data being written to 0020h-003Fh.

If more than the maximum number of latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART

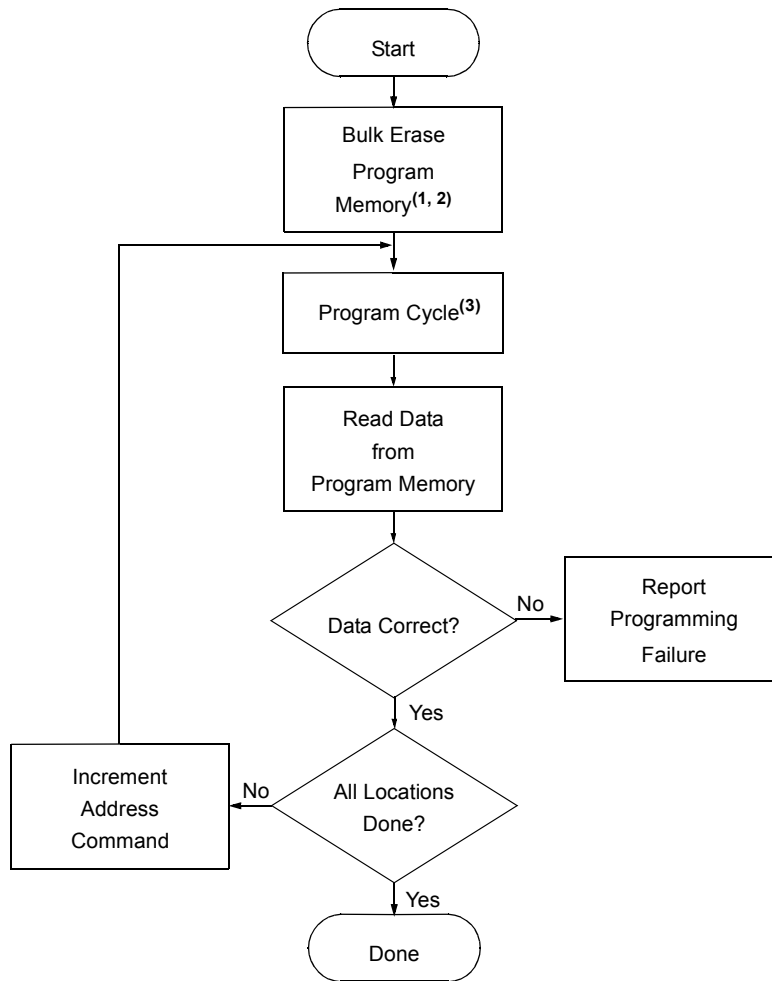


Note 1: See [Figure 5-2](#).

2: See [Figure 5-5](#).

3: See [Figure 5-6](#).

FIGURE 5-2: PROGRAM MEMORY FLOWCHART



- Note 1:** This step is optional if the device has already been erased or has not been previously programmed.
Note 2: If the device is code-protected or must be completely erased, then Bulk Erase the device per [Figure 5-8](#).
Note 3: See [Figure 5-3](#) or [Figure 5-4](#).

FIGURE 5-3: ONE-WORD PROGRAM CYCLE

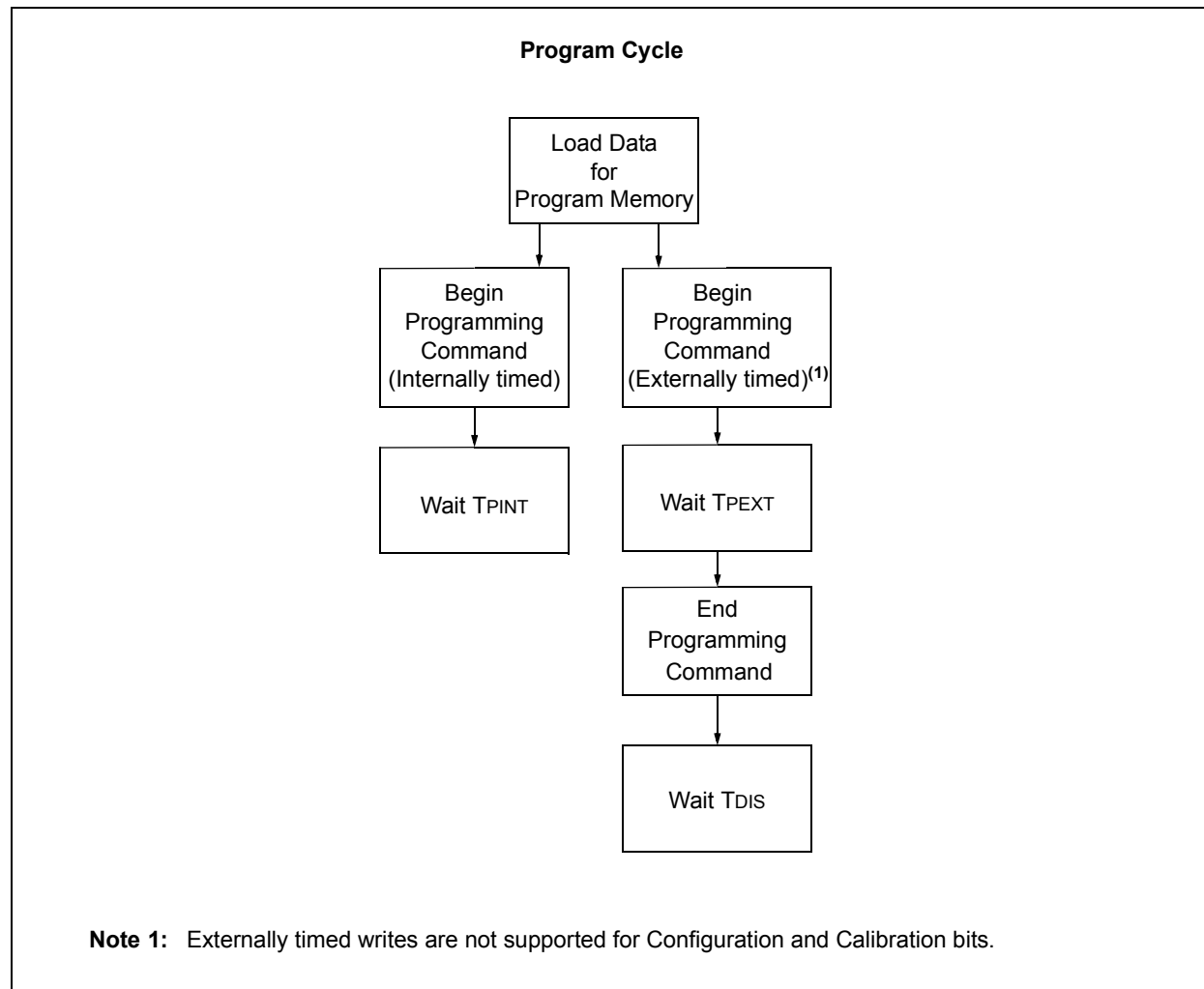


FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

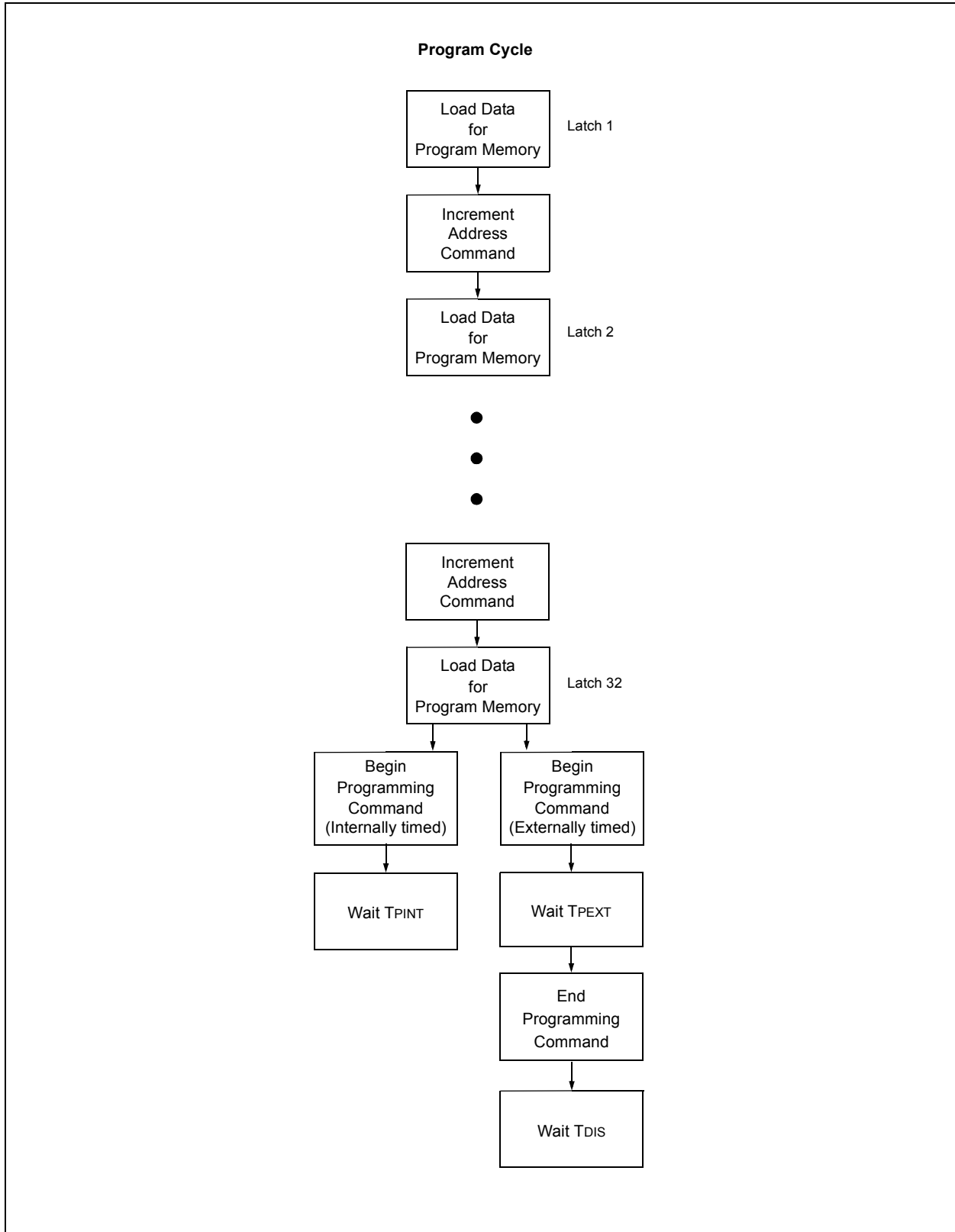


FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART

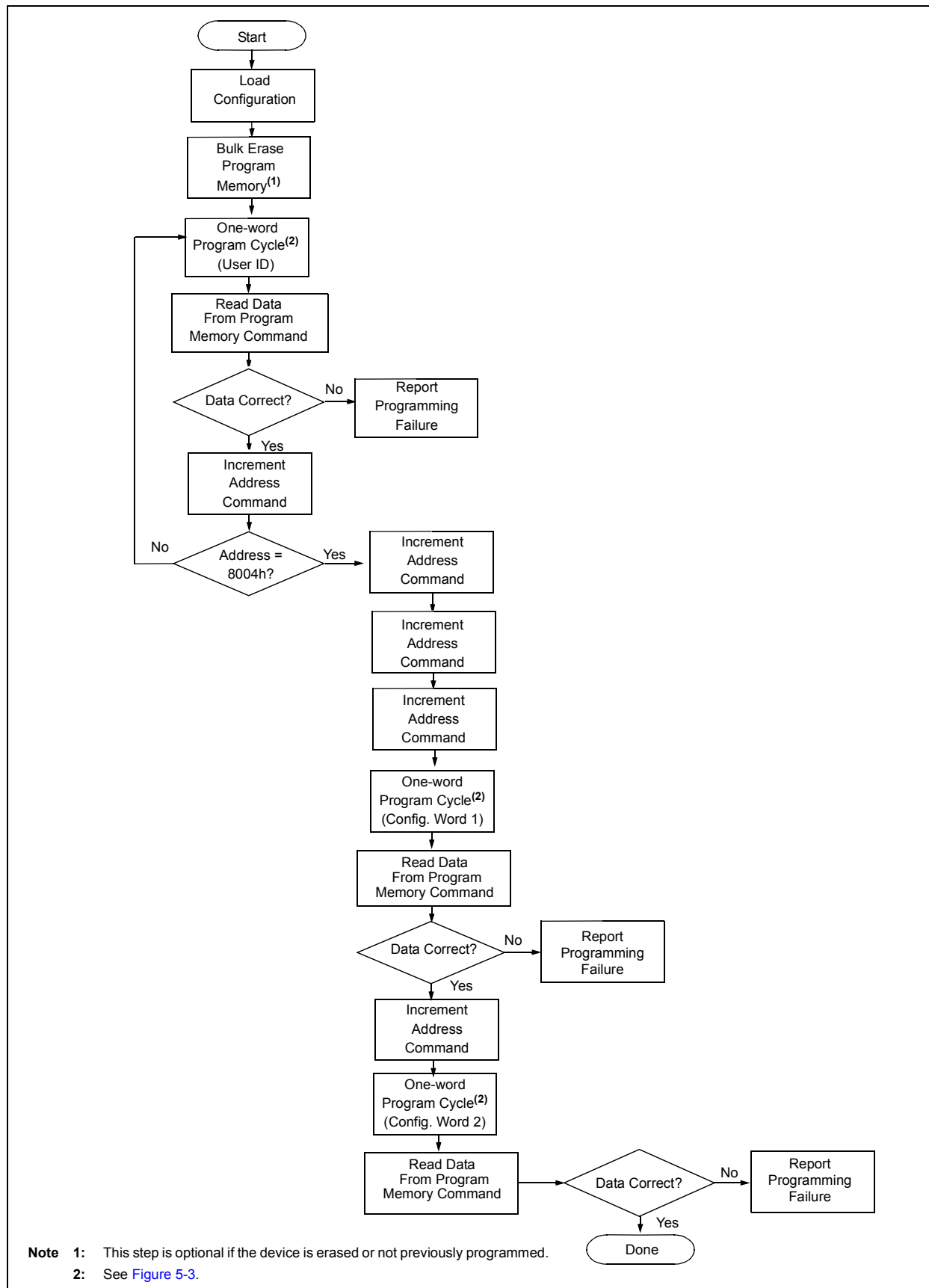
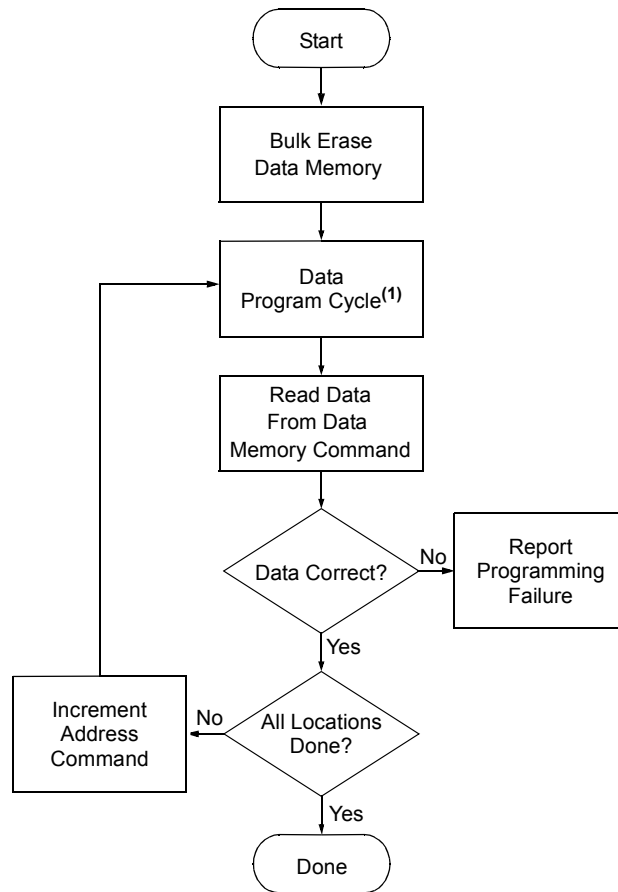


FIGURE 5-6: DATA MEMORY PROGRAM FLOWCHART



Note 1: See [Figure 5-7](#).

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FIGURE 5-7: DATA MEMORY PROGRAM CYCLE

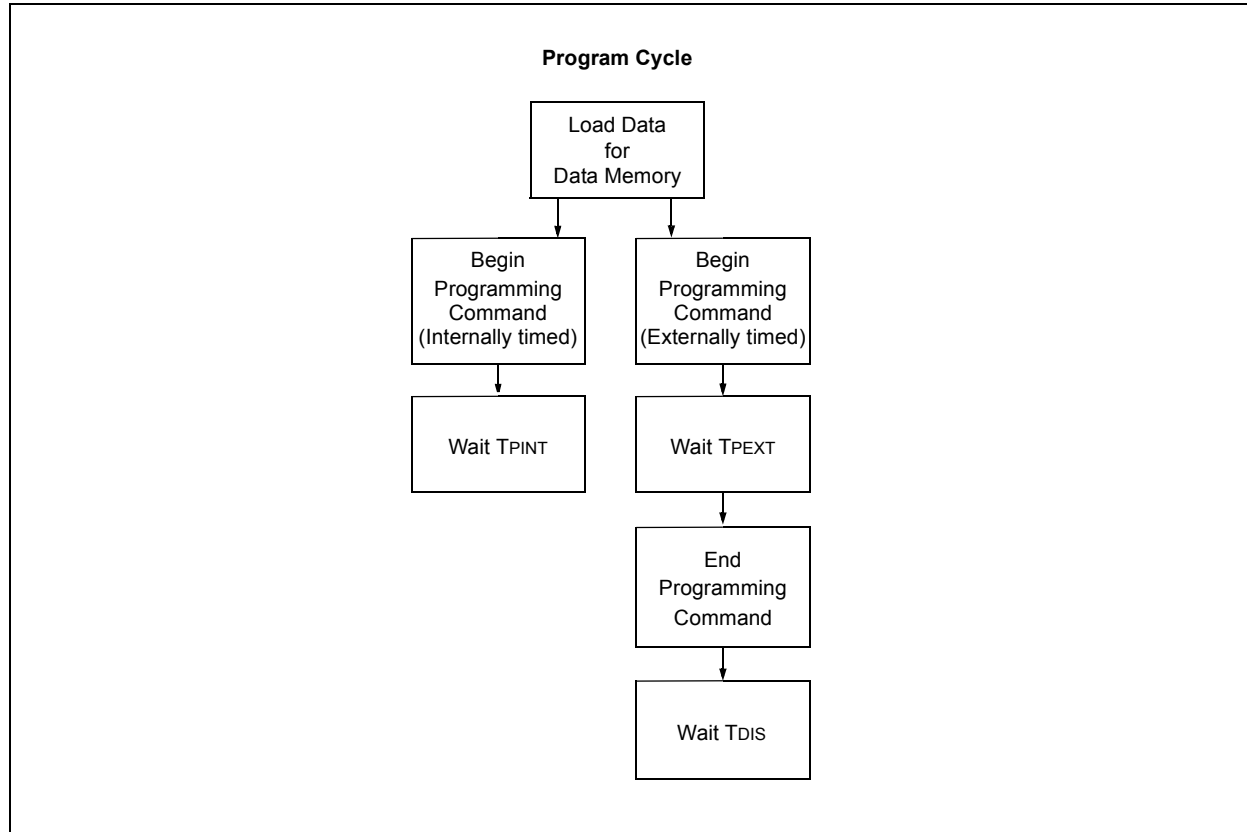
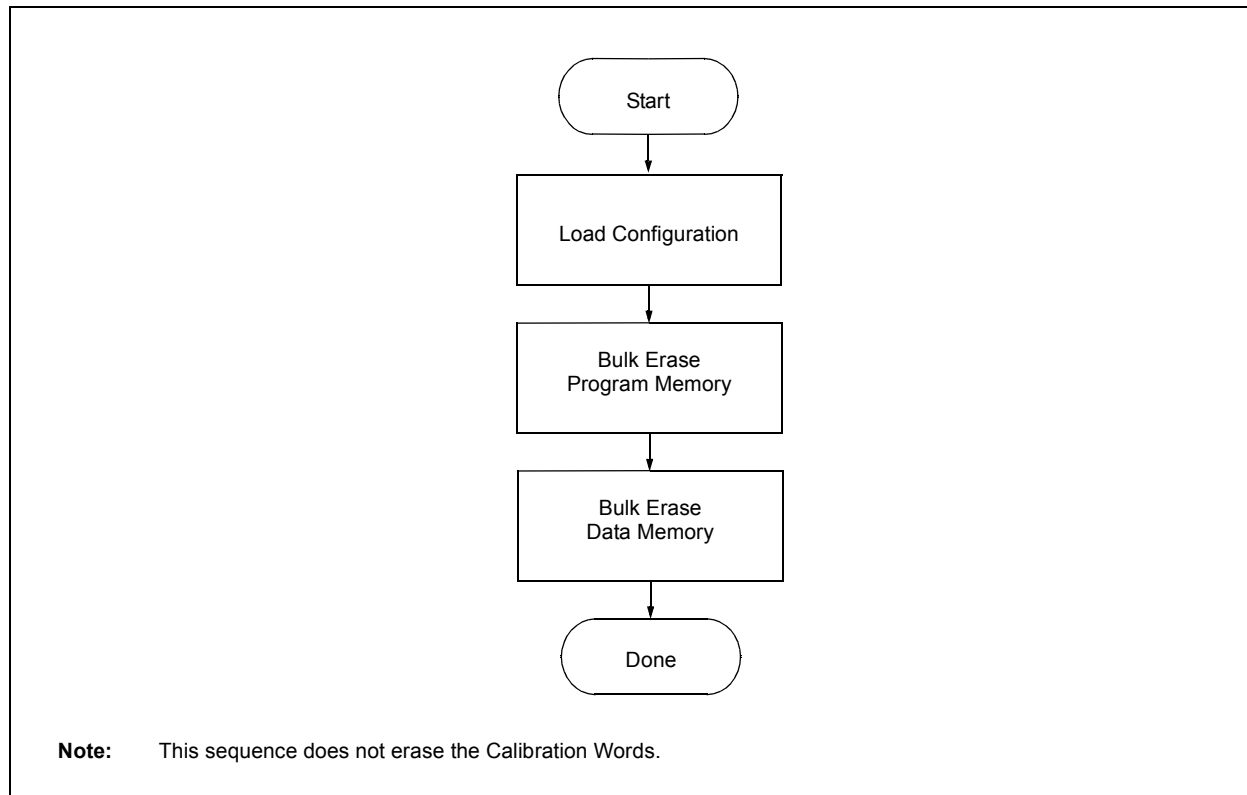


FIGURE 5-8: ERASE FLOWCHART



6.0 CODE PROTECTION

Code protection is controlled using the $\overline{\text{CP}}$ bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as '0'. Further programming is disabled for the program memory (0000h-7FFFh). Program memory can still be programmed and read during program execution.

Data memory is protected with its own Code-Protect bit ($\overline{\text{CPD}}$). When data code protection is enabled ($\overline{\text{CPD}} = 0$), all data memory locations read as '0'. Further programming is disabled for the data memory. Data memory can still be programmed and read during program execution.

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the $\overline{\text{CP}}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

6.2 Data Memory

Data memory protection is enabled by programming the $\overline{\text{CPD}}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

Note: To ensure system security, if $\overline{\text{CPD}}$ bit = 0, the Bulk Erase Program Memory command will also erase data memory.
--

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: The Configuration Word 1 is stored at 8007h. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID and Revision

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID (excluding the revision) against the value read from the part. On a mismatch condition the programmer should generate a warning message.

7.3 Data EEPROM

The programmer should be able to read data memory information from a hex file and write data memory contents to a hex file.

The physical address of the Data EEPROM memory (byte data), starts at address 0000h. However, these addresses are logically mapped above the Program Memory Space starting at Word address F000h. This provides a way of differentiating between the data and program memory locations in this range. The format for data memory storage is one data byte per 14-bit word address location, LSb aligned. The hex file format uses byte addressing, logically mapping Data EEPROM memory starting at byte address 1E000h.

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7.4 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the $\overline{CP}$ Configuration bit.

TABLE 7-1: CONFIGURATION WORD MASK VALUES

Device	Config. Word 1 Mask	Config. Word 2 Mask
PIC16F1782	3FFFh	3F23h
PIC16LF1782	3FFFh	3F03h
PIC16F1783	3FFFh	3F23h
PIC16LF1783	3FFFh	3F03h
PIC16F1784	3FFFh	3F23h
PIC16LF1784	3FFFh	3F03h
PIC16F1786	3FFFh	3F23h
PIC16LF1786	3FFFh	3F03h
PIC16F1787	3FFFh	3F23h
PIC16LF1787	3FFFh	3F03h
PIC16F1788	3FFFh	3F23h
PIC16LF1788	3FFFh	3F03h
PIC16F1789	3FFFh	3F23h
PIC16LF1789	3FFFh	3F03h

7.4.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the PIC16(L)F178X program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location (e.g., 7FFh for the PIC16F1782). Any Carry bits exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

Note: Data memory does not effect the checksum.
--

7.4.2 PROGRAM CODE PROTECTION ENABLED

When the MPLAB IDE check box for Configure->ID Memory...-> Use Unprotected Checksum is checked, then the 16-bit checksum of the equivalent unprotected device is computed and stored in the user ID. Each nibble of the unprotected checksum is stored in the Least Significant nibble of each of the four user ID locations. The Most Significant checksum nibble is stored in the user ID at location 8000h, the second Most Significant nibble is stored at location 8001h, and so forth for the remaining nibbles and ID locations. The protected checksums in [Table 7-2](#) assume that the Use Unprotected Checksum box is checked.

The checksum of a code-protected device is computed in the following manner: the Least Significant nibble of each user ID is used to create a 16-bit value. The Least Significant nibble of user ID location 8000h is the Most Significant nibble of the 16-bit value. The Least Significant nibble of user ID location 8001h is the second Most Significant nibble, and so forth for the remaining user IDs and 16-bit value nibbles. The thusly created 16-bit value is summed with the Configuration Words. All unimplemented Configuration bits are masked to '0'.

Note: Data memory does not affect the checksum.

TABLE 7-2: CHECKSUMS

Device	Config1			Config2		Checksum			
	Unprotected	Protected	Mask	Word	Mask	Unprotected		Code-protected	
						Blank	00AAh First and Last	Blank	00AAh First and Last
PIC16F1782	3FFFh	3F7Fh	3FFFh	3FFFh	3F23h	7722h	F878h	F5C4h	771Ah
PIC16F1783	3FFFh	3F7Fh	3FFFh	3FFFh	3F23h	6F22h	F078h	EDC4h	6F1Ah
PIC16F1784	3FFFh	3F7Fh	3FFFh	3FFFh	3F23h	6F22h	F078h	EDC4h	6F1Ah
PIC16F1786	3FFFh	3F7Fh	3FFFh	3FFFh	3F23h	5F22h	E078h	DDC4h	5F1Ah
PIC16F1787	3FFFh	3F7Fh	3FFFh	3FFFh	3F23h	5F22h	E078h	DDC4h	5F1Ah
PIC16F1788	3FFFh	3F7Fh	3FFFh	3FFFh	3F23h	3F22h	C078h	BDC4h	3F1Ah
PIC16F1789	3FFFh	3F7Fh	3FFFh	3FFFh	3F23h	3F22h	C078h	BDC4h	3F1Ah
PIC16LF1782	3FFFh	3F7Fh	3FFFh	3FFFh	3F03h	7702h	F858h	F584h	76DAh
PIC16LF1783	3FFFh	3F7Fh	3FFFh	3FFFh	3F03h	6F02h	F058h	ED84h	6EDAh
PIC16LF1784	3FFFh	3F7Fh	3FFFh	3FFFh	3F03h	6F02h	F058h	ED84h	6EDAh
PIC16LF1786	3FFFh	3F7Fh	3FFFh	3FFFh	3F03h	5F02h	E058h	DD84h	5EDAh
PIC16LF1787	3FFFh	3F7Fh	3FFFh	3FFFh	3F03h	5F02h	E058h	DD84h	5EDAh
PIC16LF1788	3FFFh	3F7Fh	3FFFh	3FFFh	3F03h	3F02h	C058h	BD84h	3EDAh
PIC16LF1789	3FFFh	3F7Fh	3FFFh	3FFFh	3F03h	3F02h	C058h	BD84h	3EDAh

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8.0 ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS			Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics		Min.	Typ.	Max.	Units	Conditions/Comments
Programming Supply Voltages and Currents							
VDD	Supply Voltage (VDDMIN ⁽²⁾ , VDDMAX)	PIC16LF178X	1.80	—	3.60	V	FOSC ≤ 16 MHz
			2.70	—	3.60	V	FOSC ≤ 32 MHz
		PIC16F178X	2.30	—	5.50	V	FOSC ≤ 16 MHz
			2.70	—	5.50	V	FOSC ≤ 32 MHz
VPEW	Read/Write and Row Erase operations		VDDMIN	—	VDDMAX	V	
VBE	Bulk Erase operations		2.7	—	VDDMAX	V	
IDDI	Current on VDD, Idle		—	—	1.0	mA	
IDDP	Current on VDD, Programming		—	—	3.0	mA	
IPP	VPP						
	Current on MCLR/VPP		—	—	600	μA	
VIHH	High voltage on MCLR/VPP for Program/Verify mode entry		8.0	—	9.0	V	
TVHHR	MCLR rise time (VIL to VIHH) for Program/Verify mode entry		—	—	1.0	μs	
	I/O pins						
VIH	(ICSPCLK, ICSPDAT, MCLR/VPP) input high level		0.8 VDD	—	—	V	
VIL	(ICSPCLK, ICSPDAT, MCLR/VPP) input low level		—	—	0.2 VDD	V	
VOH	ICSPDAT output high level		VDD-0.7 VDD-0.7 VDD-0.7	—	—	V	IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 2 mA, VDD = 1.8V
VOL	ICSPDAT output low level		—	—	VSS+0.6 VSS+0.6 VSS+0.6	V	IOH = 8 mA, VDD = 5V IOH = 6 mA, VDD = 3.3V IOH = 3 mA, VDD = 1.8V
VBOR	Brown-out Reset Voltage: BORV = 0 (high trip)		—	2.70	—	V	PIC16(L)F178X
	BORV = 1 (low trip)		—	2.40	—	V	PIC16F178X
			—	1.90	—	V	PIC16LF178X
Programming Mode Entry and Exit							
TENTS	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before VDD or MCLR↑		100	—	—	ns	
TENTH	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after VDD or MCLR↑		250	—	—	μs	
Serial Program/Verify							
TCKL	Clock Low Pulse Width		100	—	—	ns	
TCKH	Clock High Pulse Width		100	—	—	ns	
TDS	Data in setup time before clock↓		100	—	—	ns	
TDH	Data in hold time after clock↓		100	—	—	ns	
Tco	Clock↑ to data out valid (during a Read Data command)		0	—	80	ns	
TLZD	Clock↓ to data low-impedance (during a Read Data command)		0	—	80	ns	
THZD	Clock↓ to data high-impedance (during a Read Data command)		0	—	80	ns	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

Note 2: Bulk-erased devices default to Brown-out enabled. VDDMIN is 2.85 volts when performing low-voltage programming on a bulk-erased device, to ensure that the device is not held in Brown-out Reset.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
TDLY	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	μs	
TERAB	Bulk Erase cycle time	—	—	5	ms	
TERAR	Row Erase cycle time	—	—	2.5	ms	
TPINT	Internally timed programming operation time	—	—	2.5 5 5	ms	Program memory Configuration Words Data EEPROM
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	Note 1
TDIS	Time delay from program to compare (HV discharge time)	300	—	—	μs	
TEXT	Time delay when exiting Program/Verify mode	1	—	—	μs	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

2: Bulk-erased devices default to Brown-out enabled. VDDMIN is 2.85 volts when performing low-voltage programming on a bulk-erased device, to ensure that the device is not held in Brown-out Reset.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST

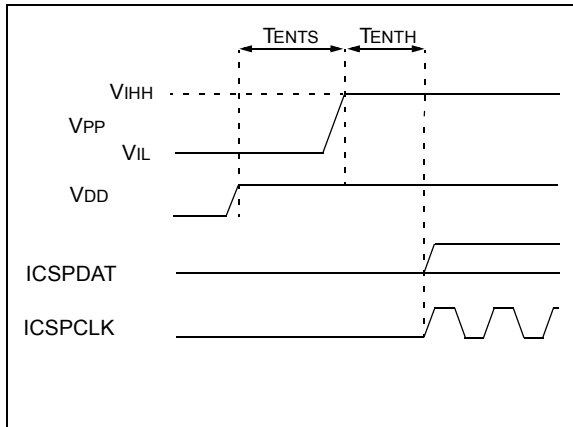


FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST

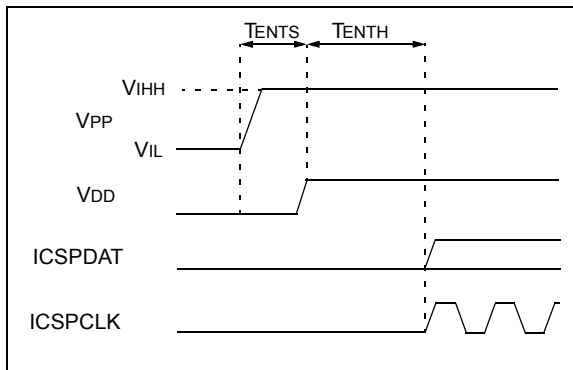


FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST

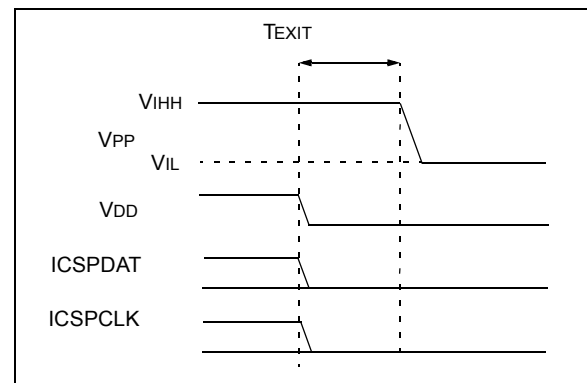
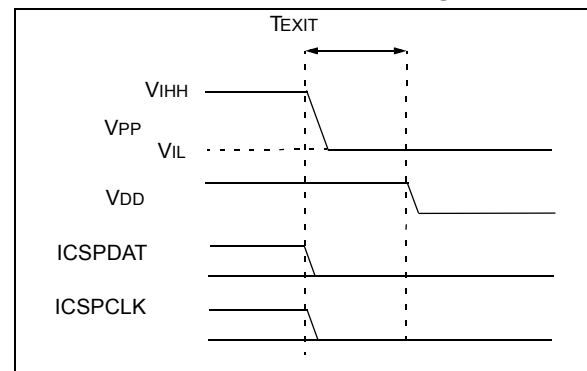


FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST



PIC16(L)F178X

FIGURE 8-5: CLOCK AND DATA TIMING

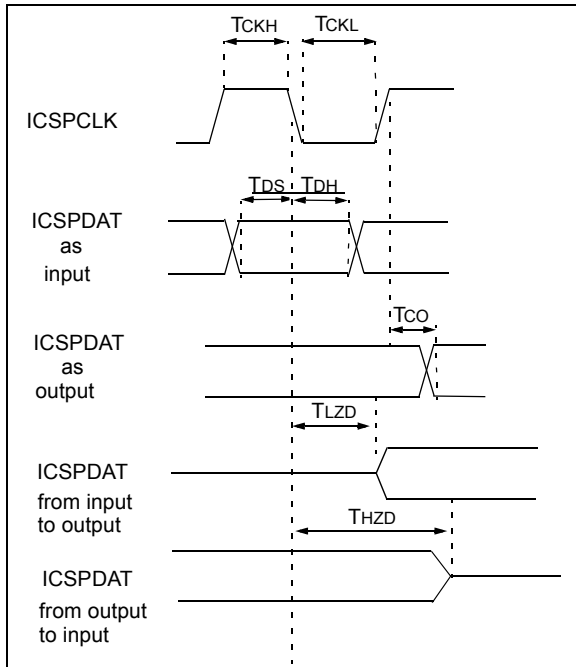


FIGURE 8-6: WRITE COMMAND-PAYLOAD TIMING

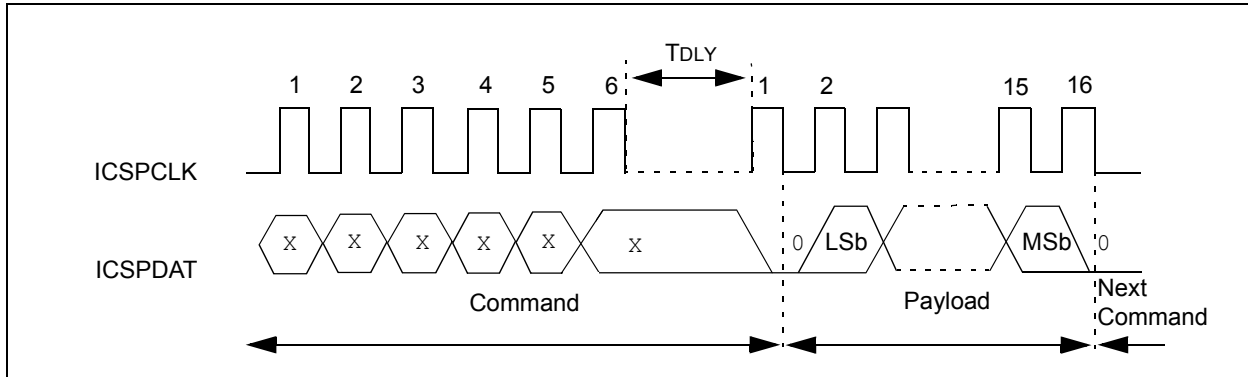


FIGURE 8-7: READ COMMAND-PAYLOAD TIMING

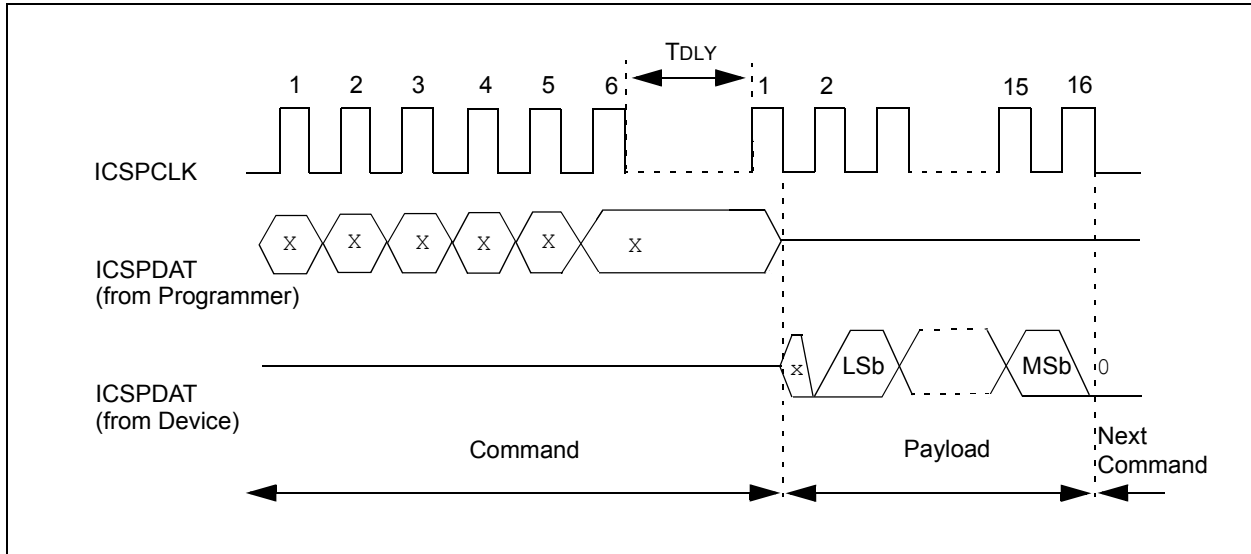


FIGURE 8-8: LVP ENTRY (POWERING UP)

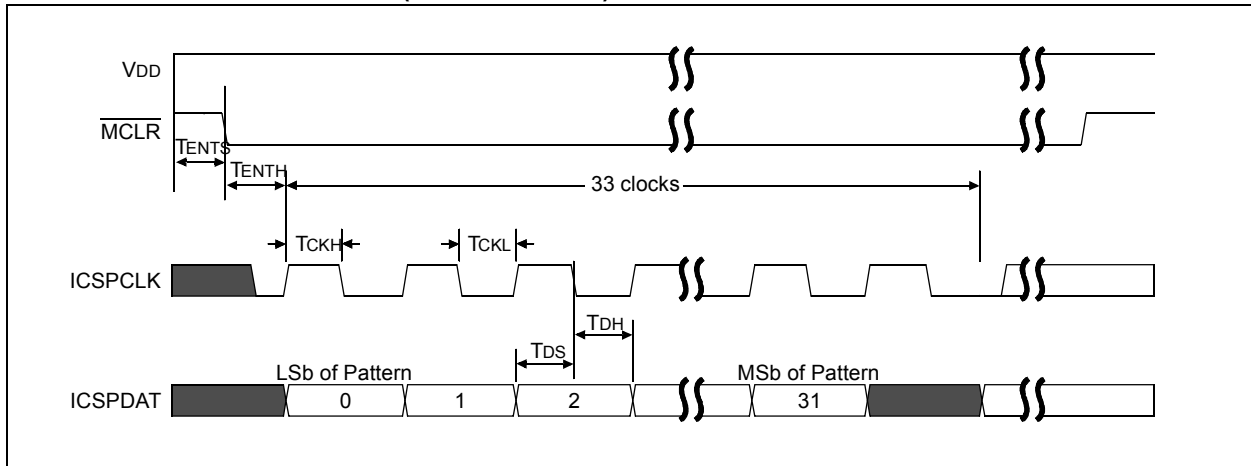
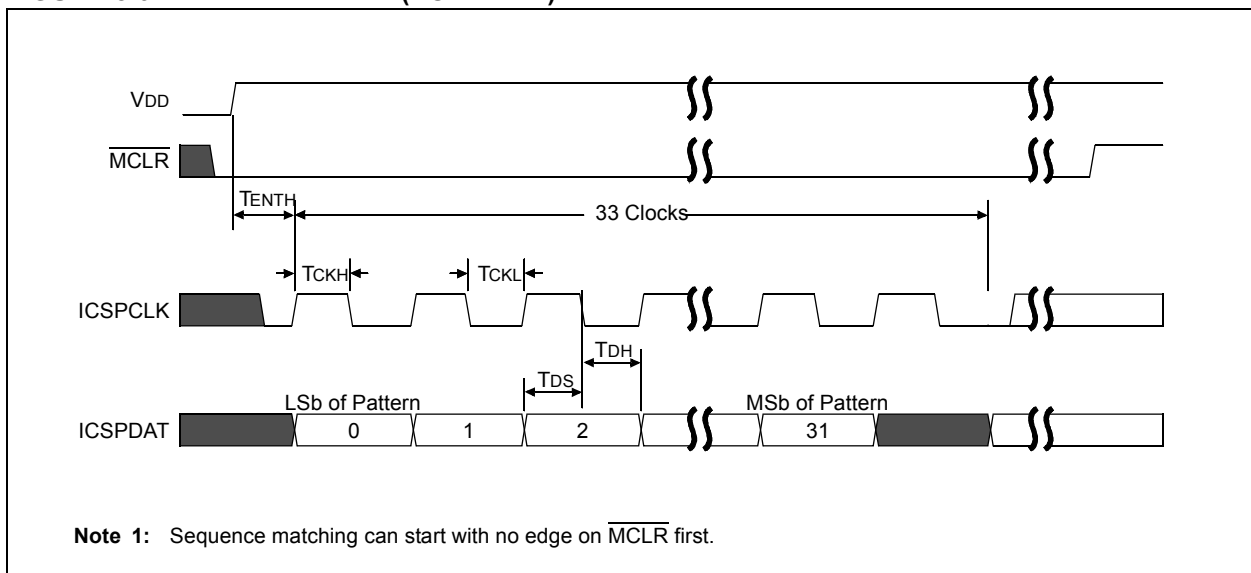


FIGURE 8-9: LVP ENTRY (POWERED)



PIC16(L)F178X

APPENDIX A: REVISION HISTORY

Revision A (01/2011)

Original release of this document.

Revision B (02/2011)

Revised section 4.3.13; Added Table 4-2; Revised section 5.0; Changed the Min. value for VDD in Table 8-1.

Revision C (02/2012)

Added PIC16(L)F1784/6/7 devices; Added Figures 2-3, 2-4, 2-5, 2-6 and 3-3; Updated Registers 3-1, 3-2 and 3-3; Updated Table 3-1 and 4-2 with the PIC16(L)F1784/6/7 devices; Updated section 7.3, Data EEPROM; Updated Table 7-1 with the PIC16(L)F1784/6/7 devices; Removed Examples 7-1 to 7-4; Added Table 7-2, Checksums; Updated section 7.4.2, Program Code Protection Enabled; Updated Table 8-1; Other minor corrections.

Revision D (03/2012)

Updated Register 3-3, Table 7-1 and Table 7-2.

Revision E (09/2012)

Added PIC16(L)F1788/1789 devices; Updated Figure 2-1 to add PIC16(L)F1788 devices; Updated Figures 2-4, 2-5, 2-6 and 2-7 to add PIC16(L)F1789 devices; Added new Figure 2-3; Updated Section 3.2, Device ID; Updated Figure 3-3; Added Figure 3-4; Added Note 2 to Register 3-1; Added Register 3-2 and Register 3-3; Updated Register 3-5; Added Table 3-2; Updated Table 4-2, Table 7-1 and Table 7-2 to include PIC16(L)F1788/9 devices; Updated Table 8-1; Other minor corrections.

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ISBN: 9781620765678

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