PIC16(L)F1713/1716 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1713/1716 family devices that you have received conform functionally to the current Device Data Sheet (DS40001726**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1713/1716 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision **(A2)**.

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1713/1716 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID (Silicon Revision)(2)	
		A1	A2
PIC16F1713	3049h	2001h	2002h
PIC16LF1713	3048h	2001h	2002h
PIC16F1716	304Bh	2001h	2002h
PIC16LF1716	304Ah	2001h	2002h

Note 1: The Revision ID and Device ID are located in the Configuration memory at addresses 8005h and 8006h, respectively.

2: Refer to the *"PIC16(L)F1713/6 Memory Programming Specification"* (DS40001714) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revision(1)	
				A1	A2
PORTS	Pin Input Impedance	1.1	Pin leakage of RA3 may be high.	X	X
Comparator	Low-Power Mode	2.1	Unexpected Low-Power mode performance.	X	X
Fixed Voltage Reference (FVR)	4x Gain Amplifier	3.1	The output of the 4x gain amplifier is 4.25V.	X	X
COG	Blanking	4.1	Blanking may fail to release.	X	
EUSART	Transmit	5.1	Duplicate Transmission.	X	
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	6.1	Slave select release during Sleep corrupts data.	X	
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	6.2	Receive data lost when Slave select enable occurs just before Sleep execution.	X	
Master Synchronous Serial Port (MSSP)	SPI Slave Mode	6.3	WCOL improperly set in Sleep.	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision **(A2)**.

1. Module: PORTS

1.1 Pin Input Impedance

The pin leakage of RA3 may be as high as 25 μA.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

2. Module: Comparator

2.1 Low-Power Mode

Unexpected performance may result when operating the comparator in Low-Power, Low-Speed mode (CxSP = 0).

Work around

Use the comparator in High-Speed, High-Power mode (CxSP = 1).

Affected Silicon Revisions

A1	A2						
X	X						

3. Module: Fixed Voltage Reference (FVR)

3.1 4x Gain Amplifier

The output of the 4x gain amplifier is 4.25V ±6%.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

4. Module: COG

4.1 Input Blanking May Not Release

When level mode input sensitivity is selected, input blanking is not zero, and a rising event occurs simultaneously with a falling event, then the blanking circuit that inhibits falling events will remain in the blanking state and the COG output will remain in the active state until a shutdown event or COG module Reset.

Work around

Use edge sensitivity or set blanking times to zero.

Affected Silicon Revisions

A1	A2						
X							

5. Module: EUSART

5.1 Duplicate Transmission

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

1. Monitor the Transmit Interrupt Flag bit (TXIF). Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty.
2. Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty.

Affected Silicon Revisions

A1	A2						
X							

6. Module: Master Synchronous Serial Port (MSSP)

6.1 SPI Slave Data Corruption During Sleep

When the MSSP module is configured in SPI Slave mode with SS pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master releases the SS line (SS goes high) before the device wakes from Sleep and updates SSPBUF, the received data will be lost.

Work around

Method 1: The SPI master must wait a minimum of parameter SP83 (1.5TCY + 40nS) after the last SCK edge AND the additional wake-up time from Sleep (device dependent) before releasing the SS line.

Method 2: If both the Master and Slave devices have an available pin, once the Slave has completed the transaction and BF or SSPIF is set, the slave could toggle an output to inform the Master that the transaction is complete and that it is safe to release the SS line.

Affected Silicon Revisions

A1	A2						
X							

6.2 SPI Slave Data Lost Before Sleep Execution

When the MSSP module is configured in SPI Slave mode with SS pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI Master enables SS (SS goes low) within 1 TCY before Sleep is executed, the data written into the SSPBUF by the slave for transmission will remain in the SSPBUF, and the byte received by the slave will be completely discarded. The MSb of the data byte that is currently loaded into SSPBUF will be transmitted on each of the eight SCK clocks, resulting in either a 0x00 or 0xFF to be incorrectly transmitted. This issue typically occurs when the device wakes up from Sleep to process data and immediately goes back to Sleep during the next transmission.

Work around

The SPI Slave must wait a minimum of 2.25 * TCY from the time the SS line becomes active (SS goes low) before executing the Sleep command.

Affected Silicon Revisions

A1	A2						
X							

6.3 WCOL Bit Improperly Set During Sleep

When the MSSP module is configured with either of the Slave modes listed below and Sleep is executed during transmission, the WCOL bit is erroneously set. Although the WCOL bit is set, it does not cause a break in transmission or reception.

Mode 1: SPI Slave mode with SS disabled (SSPM = 0101) and CKE = 0.

Mode 2: SPI Slave mode with SS enabled (SSPM = 0100) and SS in not set and then cleared before each consecutive transmission. This typically occurs during multiple byte transmissions in which the Master does not release the SS line until all transmission has completed.

Work around

Method 1: The WCOL bit can be ignored since the issue does not interfere with MSSP hardware.

Method 2: Clear the SSPEN after each transaction, then set SSPEN before the next transaction.

Affected Silicon Revisions

A1	A2						
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001726**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (01/2014)

Initial release of this document.

Rev B Document (12/2014)

Added Module 3, FVR.

Rev C Document (04/2015)

Added Module 4, COG. Added Module 5, EUSART. Added Module 6, MSSP.

Rev D Document (01/2017)

Added silicon revision A2.

Rev D Document (06/2017)

Updated the Work around section of Module 5, EUSART.

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