

PIC16(L)F15356/75/76/85/86 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F15356/75/76/85/86 family devices that you have received conform functionally to the current Device Data Sheet (DS40001866B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC16(L)F15356/75/76/85/86 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on [page 4](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select **Programmer > Reconnect**.
 - b) For MPLAB X IDE, select **Window > Dashboard** and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F15356/75/76/85/86 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾	
		A1	A2
PIC16F15356	30B0h	2001h	2002h
PIC16LF15356	30B1h	2001h	2002h
PIC16F15375	30B2h	2001h	2002h
PIC16LF15375	30B3h	2001h	2002h
PIC16F15376	30B4h	2001h	2002h
PIC16LF15376	30B5h	2001h	2002h
PIC16F15385	30B6h	2001h	2002h
PIC16LF15385	30B7h	2001h	2002h
PIC16F15386	30B8h	2001h	2002h
PIC16LF15386	30B9h	2001h	2002h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the "PIC16(L)F153XX Memory Programming Specification" (DS40001838) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions	
				A1	A2
Analog-to-Digital Converter (ADC)	ADC Positive Voltage Reference	1.1	Using FVR as the positive voltage reference to the ADC can cause missing codes in the conversion result.	X	X
Development Support	Data Breakpoints	2.1	Data breakpoints are not available on Banks 32 through 63.	X	X
Windowed Watchdog Timer (WWDT)	Watchdog Timer Clock Source	3.1	WWDT does not work with SOSC as the clock source.	X	X
Electrical Specifications	Min. VDD Specification	4.1	VDDMIN specifications are changed for LF devices only.	X	X
Electrical Specifications	Fixed Voltage Reference (FVR) Accuracy	4.2	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A2).

1. Module: Analog-to-Digital Converter (ADC)

1.1 ADC Positive Voltage Reference

Using the FVR as the positive voltage reference to the ADC can cause an increase in missing codes.

Work around

1. Increase the bit conversion time, known as TAD, to 8 us.
2. Use VDD as the positive voltage reference to the ADC.

Affected Silicon Revisions

A1	A2						
X	X						

2. Module: Development Support

2.1 Data Breakpoints

Data breakpoints are not available on Banks 32 through 63. Any breakpoints that are placed in Banks 32 through 63 will fail to be recognized.

Work around

None.

Affected Silicon Revisions

A1	A2						
X							

3. Module: Windowed Watchdog Timer (WWDT)

3.1 WWDT Clock Source Selection

When the WDTCS <2:0> bits of the WDTCON1 register are set to 'b010', selecting the Secondary Oscillator SOSC 32 kHz as the clock source, the WWDT does not operate.

Work around

Use the LFINTOSC or MFINTOSC clock sources for the WWDT.

Affected Silicon Revisions

A1	A2						
X							

4. Module: Electrical Specifications

4.1 Min VDD Specification

VDDMIN specifications are changes for LF devices only. VDDMIN at -40°C to 25°C = 2.0V.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

4.2 Fixed Voltage References (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001866B):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Interrupt-On-Change (PORTE)

Bits <2:0> are unimplemented in registers IOCEP, IOCEN, and IOCEF, as indicated in the following register tables.

REGISTER 17-10: IOCEP: INTERRUPT-ON-CHANGE PORTE POSITIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	U-0	U-0	U-0
—	—	—	—	IOCEP3 ⁽¹⁾	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **IOCEP3:** Interrupt-on-Change PORTE Positive Edge Enable bit
 1 = Interrupt-on-Change enabled on the pin for a positive-going edge. IOCCF_x bit and IOCIF flag will be set upon detecting an edge.
 0 = Interrupt-on-Change disabled for the associated pin

bit 2-0 **Unimplemented:** Read as '0'

Note 1: IF MCLRE = 1 or LVP = 1, port functionality is disabled and IOC on that pin is not available.

REGISTER 17-11: IOCEN: INTERRUPT-ON-CHANGE PORTE NEGATIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	U-0	U-0	U-0
—	—	—	—	IOCEN3 ⁽¹⁾	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **IOCEN3:** Interrupt-on-Change PORTE Negative Edge Enable bit
 1 = Interrupt-on-Change enabled on the pin for a negative-going edge. IOCCF_x bit and IOCIF flag will be set upon detecting an edge.
 0 = Interrupt-on-Change disabled for the associated pin

bit 2-0 **Unimplemented:** Read as '0'

Note 1: IF MCLRE = 1 or LVP = 1, port functionality is disabled and IOC on that pin is not available.

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REGISTER 17-12: IOCEF: INTERRUPT-ON-CHANGE PORTE FLAG REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	U-0	U-0	U-0
—	—	—	—	IOCEP3 ⁽¹⁾	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

HS - Bit is set in hardware

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **IOCEF:** Interrupt-on-Change PORTE Flag bit

1 = An enabled change was detected on the associated pin

Set when IOCCPx = 1 and a rising edge was detected on RCx, or when IOCCNx = 1 and a falling edge was detected on RCx.

0 = No change was detected, or the user cleared the detected change

bit 2-0 **Unimplemented:** Read as '0'

Note 1: IF MCLRE = 1 or LVP = 1, port functionality is disabled and IOC on that pin is not available.

2. Module: Section 4.2.3 Boot Block

If **BBEN** = 0, the Boot Block is enabled and a specific address range is allotted as the Boot Block based on the value of the BBSIZE bits of Configuration Word ([Register 5-4](#)) and the sizes provided in [Table 5-1](#).

APPENDIX A: DOCUMENT REVISION HISTORY

Rev B Document (11/2018)

Added Module 4: Electrical Specifications, 4.1 and 4.2.
Data Sheet Clarifications: Removed Modules 1 and 2.
Added Module 1: Interrupt-on-Change (PORTE); Added
Module 2: Section 4.2.3 Boot Block.

Rev A Document (1/2017)

Initial release of this document.

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