

PIC16(L)F15354/55 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F15354/55 family devices that you have received conform functionally to the current Device Data Sheet (DS40001853C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC16(L)F15354/55 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on [page 4](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F15354/55 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾
		A2
PIC16F15354	30ACh	2002h
PIC16LF15354	30ADh	2002h
PIC16F15355	30AEh	2002h
PIC16LF15355	30AFh	2002h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the "PIC16(L)F153XX Memory Programming Specification" (DS40001838) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A2
Analog-to-Digital Converter (ADC)	ADC Positive Voltage Reference	1.1	Using FVR as the positive voltage reference to the ADC can cause missing codes in the conversion result.	X
Development Support	Data Breakpoints	2.1	Data breakpoints are not available on Banks 32 through 63.	X
Windowed Watchdog Timer (WWDT)	Watchdog Timer Clock Source	3.1	WWDT does not work with SOSC as the clock source.	X
Electrical Specifications	Min. V _{DD} Specification	4.1	V _{DDMIN} specifications are changed for LF devices only.	X
	Fixed Voltage Reference (FVR) Accuracy	4.2	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A2).

1. Module: Analog-to-Digital Converter (ADC)

1.1 ADC Positive Voltage Reference

Using the FVR as the positive voltage reference to the ADC can cause an increase in missing codes.

Work around

1. Increase the bit conversion time, known as TAD, to 8 us.
2. Use VDD as the positive voltage reference to the ADC.

Affected Silicon Revisions

A2							
X							

2. Module: Development Support

2.1 Data Breakpoints

Data breakpoints are not available on Banks 32 through 63. Any breakpoints that are placed in Banks 32 through 63 will fail to be recognized.

Work around

None.

Affected Silicon Revisions

A2							
X							

3. Module: Windowed Watchdog Timer (WWDT)

3.1 WWDT Clock Source Selection

When the WDTCS <2:0> bits of the WDTCON1 register are set to 'b010', selecting the Secondary Oscillator SOSC 32 kHz, as the clock source, the WWDT does not operate.

Work around

Use the LFINTOSC or MFINTOSC clock sources for the WWDT.

Affected Silicon Revisions

A2							
X							

4. Module: Electrical Specifications

4.1 Min. VDD Specifications

VDDMIN specifications are changed for LF devices only. VDDMIN at -40°C to 25°C = 2.0V.

Work around

None

Affected Silicon Revisions

A2							
X							

4.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

None

Affected Silicon Revisions

A2							
X							

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001853C):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

1. Module: Analog-to-Digital Converter

Added RA6 bit description to bit 7-2 from register 20-1 from ADC chapter.

20.4 Register Definitions: ADC Control

REGISTER 20-1: ADCON0: ADC CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CHS<5:0>						GO/DONE	ADON
bit 7						bit 0	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2 **CHS<5:0>**: Analog Channel Select bits
111111 =FVR Buffer 2 reference voltage⁽²⁾
111110 =FVR 1Buffer 1 reference voltage⁽²⁾
111101 =DAC1 output voltage⁽¹⁾
111100 =Temperature sensor output⁽³⁾
111011 =AVss (Analog Ground)
111010 - 011000 = Reserved. No channel connected
.
.
010111 = RC7
010110 = RC6
010101 = RC5
010100 = RC4
010011 = RC3
010010 = RC2
010001 = RC1
010000 = RC0
001111 = RB7
001110 = RB6
001101 = RB5
001100 = RB4
001011 = RB3
001010 = RB2
001001 = RB1
001000 = RB0
000111 = RA7⁽⁴⁾
000110 = RA6⁽⁴⁾
000101 = RA5
000100 = RA4
000011 = RA3
000010 = RA2
000001 = RA1
000000 = RA0

bit 1 **GO/DONE**: ADC Conversion Status bit
1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle.
This bit is automatically cleared by hardware when the ADC conversion has completed.
0 = ADC conversion completed/not in progress

REGISTER 20-1: ADCON0: ADC CONTROL REGISTER 0 (CONTINUED)

bit 0 **ADON:** ADC Enable bit
 1 = ADC is enabled
 0 = ADC is disabled and consumes no operating current

- Note**
- 1: See [Section 21.0 “5-Bit Digital-to-Analog Converter \(DAC1\) Module”](#) for more information
 - 2: See [Section 18.0 “Fixed Voltage Reference \(FVR\)”](#) for more information.
 - 3: See [Section 19.0 “Temperature Indicator Module”](#)
 - 4: The analog channel functionality on these pins is disabled when the system clock source is selected is external.

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APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2016)

Initial release of this document.

Rev B Document (01/2017)

Removed Module 1: Oscillators. Added Module 3: Windowed Watchdog Timer (WWDT). Other minor corrections.

Rev C Document (08/2017)

Added Module 4: Electrical Specifications

Data Sheet Clarifications: Added Modules 1 and 2. Other minor corrections.

Rev D Document (03/2018)

Data Sheet Clarifications: Added Module 1: Analog-to-Digital Converter.

Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

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