



MICROCHIP PIC16(L)F1516/1517/1518/1519

PIC16(L)F1516/1517/1518/1519 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1516/1517/1518/1519 family devices that you have received conform functionally to the current Device Data Sheet (DS40001452F), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC16(L)F1516/1517/1518/1519 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (A7).

Data Sheet clarifications and corrections start on [page 7](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select **Programmer > Reconnect**.
 - b) For MPLAB X IDE, select **Window > Dashboard** and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1516/1517/1518/1519 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0> ^{(1),(2)}					
	DEV<8:0>	REV<4:0> Silicon Revision				
		A2	A3	A4	A6	A7
PIC16F1516	01 0110 100	—	0 0011	0 0100	0 0110	0 0111
PIC16LF1516	01 0111 100	0 0010	0 0011	0 0100	0 0110	0 0111
PIC16F1517	01 0110 101	—	0 0011	0 0100	0 0110	0 0111
PIC16LF1517	01 0111 101	0 0010	0 0011	0 0100	0 0110	0 0111
PIC16F1518	01 0110 110	—	0 0011	0 0100	0 0110	0 0111
PIC16LF1518	01 0111 110	0 0010	0 0011	0 0100	0 0110	0 0111
PIC16F1519	01 0110 111	—	0 0011	0 0100	0 0110	0 0111
PIC16LF1519	01 0111 111	0 0010	0 0011	0 0100	0 0110	0 0111

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the “PIC16(L)F151X/152X Memory Programming Specification” (DS41442) for detailed information on Device and Revision IDs for your specific device.

PIC16(L)F1516/1517/1518/1519

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾				
				A2	A3	A4	A6	A7
High-Frequency Internal Oscillator (HFINTOSC)	HFINTOSC Operation	1.1	HFINTOSC is not stable when $V_{DD} < 2.3V$.	X				
High-Frequency Internal Oscillator (HFINTOSC)	HFINTOSC Operation	1.2	HFINTOSC Max. V_{DD} at $-40^{\circ}C$.		X			
FVR	FVR Ready Bit (FVRRDY)	2.1	FVRRDY bit may not get set at low V_{DD} and low operating temperature.	X				
Oscillator	HFINTOSC Ready/Stable bit	3.1	Bits remained set to '1' after initial trigger.	X	X	X		
Oscillator	Clock Switching	3.2	Clock switching can cause a single corrupted instruction.	X	X	X		
Oscillator	Oscillator Start-up Timer (OST) bit	3.3	OST bit remains set.	X	X	X		
Configuration Word	Configuration Word 1, Bit 8	4.1	Writing the unimplemented Configuration Word bit 8 affects bit 7.	X	X			
Low-Dropout (LDO) Voltage Regulator	Low-Power Sleep mode	5.1	Unexpected Resets may occur at ambient temperatures below $0^{\circ}C$.	X	X	X	X	
MSSP (Master Synchronous Serial Port)	SPI Master mode	6.1	Buffer Full (BF) bit or MSSP Interrupt Flag (SSPIF) bit becomes set half SCK cycle too early.	X	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Slave mode	6.2	SPI Master releasing Slave Select during Slave Sleep mode corrupts data.	X	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Slave mode	6.3	SPI Master enabling Slave Select too early could lose received data in Slave.	X	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Slave mode	6.4	WCOL is erroneously set in SPI Slave mode during Sleep.	X	X	X	X	X
Enhanced Universal Synchronous Receiver Transmitter (EUSART)	Transmit mode	7.1	Possible duplicate byte transmitted	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A7).

1. Module: High-Frequency Internal Oscillator (HFINTOSC)

1.1 Internal Oscillator min. VDD

The High-Frequency Internal Oscillator requires a minimum voltage of 2.3V to operate.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X							

1.2 HFINTOSC Max. VDD at -40°C

For the LF devices only, the High-Frequency Internal Oscillator may stop working at -40°C when VDD is 3.6V.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
	X						

2. Module: FVR

2.1 FVR Ready Bit (FVRRDY)

After the FVR is stabilized, the FVR Ready bit may not be set when the temperature is -40°C and VDD = 1.8V.

Work around

Operate above -30°C or with VDD >2.0V.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X							

3. Module: Oscillator

3.1 OSCSTAT bits: HFIOFR and HFIOFS

When HFINTOSC is selected, the HFIOFR and HFIOFS bits will become set when the oscillator becomes ready and stable. Once these bits are set, they become “stuck”, indicating that HFINTOSC is always ready and stable. If the HFINTOSC is disabled, the bits fail to be cleared.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X					

3.2 Clock Switching

When switching clock sources between INTOSC clock source and an external clock source, one corrupted instruction may be executed after the switch occurs.

This issue affects Two-Speed Start-up and Fail-Safe Clock Monitor operation.

Work around

When switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired internal oscillator frequency.

When switching from an internal oscillator (INTOSC) to an external oscillator clock source, first switch to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X					

3.3 Oscillator Start-up Timer (OST) bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- MCLR Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X					

4. Module: Configuration Word

4.1 Configuration Word 1, Bit 8

If an attempt is made to clear bit 8, bit 7 will be cleared instead. A cleared bit 7 enables code-protect on the device.

Work around

Do not write Configuration Word 1, bit 8 to '0'.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X						

5. Module: Low-Dropout (LDO) Voltage Regulator

5.1 Low-Power Sleep mode at Ambient Temperatures Below 0°C

Under the following conditions:

- ambient temperatures below 0°C
- while in Sleep mode
- VREGCON configured for Low-Power Sleep mode (VREGPM = 1)

On very rare occasions, the LDO voltage will drop below the minimum VDD, causing unexpected device Resets.

Work around

For applications that operate at ambient temperatures below 0°C, use the LDO voltage regulator in Normal-Power mode (VREGPM = 0).

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X				

6. Module: MSSP (Master Synchronous Serial Port)

6.1 SPI Master mode

When the MSSP is used in SPI Master mode and the CKE bit is clear (CKE = 0), the Buffer Full (BF) bit and the MSSP Interrupt Flag (SSPIF) bit becomes set half an SCK cycle early. If the user software immediately reacts to either of the bits being set, a write collision may occur as indicated by the WCOL bit being set.

Work around

To avoid a write collision one of the following methods should be used:

Method 1: Add a software delay of one SCK period after detecting the completed transfer (the BF bit or SSPIF bit becomes set) and prior to writing to the SSPBUF register. Verify the WCOL bit is clear after writing to SSPBUF. If the WCOL bit is set, clear the bit in software and rewrite the SSPBUF register.

Method 2: As part of the MSSP initialization procedure, set the CKE bit (CKE = 1).

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X	X			

6.2 SPI Slave mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during the SPI activity, if the SPI master releases the $\overline{SS}$ line ($\overline{SS}$ goes high) before the device wakes from Sleep and updates SSPBUF, the received data will be lost.

Work around

1. The SPI master must wait a minimum of parameter SP83 ($1.5T_{CY} + 40\text{ ns}$) after the last SCK edge and the additional wake-up time from Sleep (device dependent) before releasing the $\overline{SS}$ line.
2. If both the Master and Slave devices have an available pin, once the Slave has completed the transaction and BF or SSPIF is set, the slave could toggle an output to inform the Master that the transaction is complete and that it is safe to release the $\overline{SS}$ line.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X	X			

6.3 SPI Slave mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI Master enables $\overline{SS}$ ($\overline{SS}$ goes low) within $1 T_{CY}$ before Sleep is executed, the data written into the SSPBUF by the slave for transmission will remain in the SSPBUF, and the byte received by the slave will be completely discarded. The MSb of the data byte that is currently loaded into SSPBUF will be transmitted on each of the eight SCK clocks, resulting in either a 0x00 or 0xFF to be incorrectly transmitted. This issue typically occurs when the device wakes up from Sleep to process data and immediately goes back to Sleep during the next transmission.

Work around

The SPI Slave must wait a minimum of $2.25 * T_{CY}$ from the time the $\overline{SS}$ line becomes active ($\overline{SS}$ goes low) before executing the Sleep command.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X	X			

6.4 SPI Slave mode

When the MSSP module is configured with either of the Slave modes listed below and Sleep is executed during transmission, the WCOL bit is erroneously set. Although the WCOL is set, it does not cause a break in transmission or reception.

Modes:

1. SPI Slave mode with $\overline{SS}$ disabled (SSPM = 0101) and CKE = 0, or
2. SPI Slave mode with $\overline{SS}$ enabled (SSPM = 0100) and $\overline{SS}$ is not set and then cleared before each consecutive transmission. This typically occurs during multiple byte transmissions in which the Master does not release the $\overline{SS}$ line until all transmission has completed.

Work around

1. The WCOL bit can be ignored since the issue does not interfere with MSSP hardware, or
2. Clear the SSPEN after each transaction then set SSPEN before next transaction.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X	X			

7. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

7.1 Transmit mode

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

1. Monitor the Transmit Interrupt Flag bit (TXIF). Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty.
2. Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty.

Affected Silicon Revisions

A2	A3	A4	A6	A7			
X	X	X	X	X			

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001452F):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: MSSP(SPI)

The electrical specification parameter number 70 from [Table 25-12](#) has been modified as follows:

TABLE 25-12: SPI MODE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
70*	TssL2sCH, TssL2sCL	$\overline{SS}\downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ input	2.25 *T _{CY}	—	—	ns	

PIC16(L)F1516/1517/1518/1519

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2010)

Initial release of this document.

Rev B Document (03/2011)

Added Silicon Revision A3; Added PIC16F1516, PIC16F1517, PIC16F1518 and PIC16F1519 devices; Added Module 1.2.

Rev C Document (03/2012)

Added Silicon Revision A4; Added Module 3 Oscillator; Added Module 4 Configuration Word; Other minor corrections.

Data Sheet Clarifications: Added Module 1, Oscillator.

Rev D Document (07/2012)

Added MPLAB X IDE; Added Module 5, Low-Dropout (LDO) Voltage Regulator.

Data Sheet Clarifications: Added Module 2, Memory, High-Endurance Flash.

Rev E Document (12/2012)

Added Silicon Revision A6.

Data Sheet Clarifications removed for DS41452C.

Rev F Document (10/2013)

Added Silicon Revision A7; Other minor corrections.

Rev G Document (11/2014)

Added module 6, MSSP; Other minor corrections.

Rev H Document (02/2015)

Added Modules 6.2, 6.3, 6.4 and 7 (EUSART); Other minor corrections.

Data Sheet Clarifications: Added Module 1 (MSSP Module).

Rev I Document (06/2017)

Changed the text in Module 7, Work around section. Other minor corrections.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KEELOQ, KEELOQ logo, Klear, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2010-2017, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-1842-9

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-3326-8000
Fax: 86-21-3326-8021

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

France - Saint Cloud
Tel: 33-1-30-60-70-00

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820