PIC12F629/675

PIC12F629/675 Family
Silicon Errata and Data Sheet Clarification

The PIC12F629/675 family of devices that you have received conform functionally to the current Device Data Sheet (DS41190**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC12F629/675 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B0**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC12F629/675 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A9	B0
PIC12F629	1111110 xxxxx	0F90h	0F8Bh
PIC12F675	1111100 xxxxx	0FD0h	0FCBh

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC12F629/675 Flash Programming Specification"* (DS41191) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A9	B0
Data EEPROM Memory	Interrupt Flag	1.	Inadvertently clears.	X	X
Power-on Reset	—	2.	Low V_{DD} Level may fail to release the Reset.	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B0**).

1. Module: Data EEPROM Memory

The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register, simultaneously with the completion of an EEPROM write. This condition occurs when the EEPROM write timer completes at the same moment that the PIR1 register operation is executed. Register operations are those that have the PIR1 register as the destination and include, but are not limited to, BSF, BCF, ANDWF, IORWF and XORWF.

Work around

1. Avoid operations on the PIR1 register when writing to the EEPROM memory.
2. Poll the WR bit (EECON1<1>) to determine when the write is complete.
3. Use a timer interrupt to catch any instances when the EEIF flag is inadvertently cleared. The timer interrupt should be set longer than 8 ms. If EEIF fails, then the timer interrupt occurs as a default time out. The WR and WRERR flags are checked as part of the timer Interrupt Service Routine to verify the EEPROM write success.
4. If periodic interrupts are occurring in addition to the EEIF interrupts, then use a secondary flag to sense write completion. The secondary flag is set whenever EEPROM writes are active. An EEPROM write completion is indicated when the secondary flag is set and the WR flag is clear.

Affected Silicon Revisions

A9	B0						
X	X						

2. Module: Power-on Reset (Rising VDD Detect)

The PIC12F629/675 Power-on Reset (POR) circuitry is sensitive to a low VDD level and may fail to release the Reset if VDD returns to an operational voltage after dropping to a very low level.

The sensitive VDD condition occurs when VDD drops into an out-of-specification voltage region below the Brown-out Detect threshold and then recovers to a normal operating condition. The voltage region that can cause the problem is dependant upon temperature with the region growing as the temperature drops. A typical region is between 0.5 and 0.7V at -25°C. Below the region, the POR operates correctly. Above the region, the POR is inactive per the data sheet. Inside the region, the POR will assert Reset and will not release Reset until power is removed and VDD reaches VSS. Because the POR is independent of other Reset circuits (see Figure 9-4 of the data sheet), activating BOR or using the MCLR input will not eliminate the problem.

Work around

To resolve this problem, the application must be designed to assure that VDD reaches VSS. This is described as D003 VPOR in **Section 12.0 "Electrical Specifications"** of the Device Data Sheet (DS41190**F**).

Affected Silicon Revisions

A9	B0						
X							

Data Sheet Clarification

None.

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APPENDIX A: DOCUMENT REVISION HISTORY

Rev. A Document (3/2002)

First revision of this document. Revised Table 12.3

Rev. B Document (9/2002)

Added Module 1: “In-Circuit Serial Programming™”, changes made to the Typical In-Circuit Serial Programming Connection, Figure 9-18.

Rev. C Document (04/02/04)

Removed Table 12.3 and Figure 9-18 due to Data Sheet revisions.
Added Module 1: “GPIO Port”, changes made to the TRISIO – GPIO Tri-state Register.

Rev. D Document (11/2004)

Added Module 1: “Data EEPROM Memory” for PIC12F629/675 silicon.

Rev. E Document (07/2005)

Data Sheet Clarifications/Corrections Section: Added Module 2: New 4x4 DFN Package added.

Rev. F Document (10/2005)

Data Sheet Clarifications/Corrections Section: Replaced 8-Lead Plastic Dual Flat No Lead Package 4x4 (DFN).

Rev. G Document (8/2006)

Added Module 2: “Power-on Reset (Rising V_{DD} Detect)” for PIC12F629/675 silicon.

Rev. H Document (6/2009)

Updated the document with new format. Deleted Module 1 and 2 from the Data Sheet Clarification section. Updated Table 1 and 2. Other minor edits.

NOTES:

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