

Errata Sheet for Rev. A PIC12CE67X Engineering Sample Silicon

The PIC12CE67X (Rev A) engineering sample parts conform functionally to the PIC12CE67X data sheet (DS40181A), except for the anomalies described below. These problems will be addressed in the next revision of the PIC12CE67X silicon.

- Determine if you have Rev. A silicon. If you have an 8 lead PDIP part with Rev. A silicon, the part will be marked like the following example:

Example



- A/D

If bits PCFG2:PCFG0 of ADCON1 register are configured in 111 mode (all digital inputs), then VREF = VSS. Performing an analog read will give erroneous results.

- The OSCCAL Register in Rev. A silicon does not function per the datasheet (DS40181A). Use the following definitions of OSCCAL below:

OSCCAL REGISTER (ADDRESS 8Fh)

R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	U-0	U-0
CAL3	CAL2	CAL1	CAL0	CALFST	CALSLW	—	—
bit7						bit0	

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7-4: **CAL<3:0>**: Fine calibration

bit 3: **CALFST**: Calibration Fast
1 = Increase frequency
0 = No change

bit 2: **CALSLW**: Calibration Slow
1 = Decrease frequency
0 = No change

bit 1-0: **Unimplemented**: Read as '0'

Note: If CALFST = 1 and CALSLW = 1, CALFST has precedence.

Clarifications/Corrections to the Data Sheet:

Reference 12.1 DC Characteristics, page 81 of the PIC12CE67X Data Sheet (DS40181A). The following information should replace Parm No. D028 in the "Typ" column and the "Max" column:

Typ = 0.1
Max = 0.2

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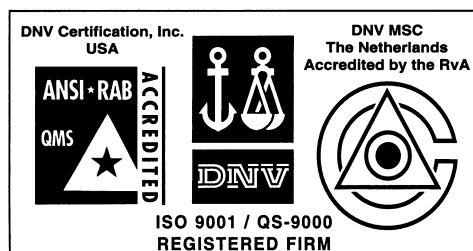
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