



PIC12F609/615/12HV609/615

PIC12F609/615/12HV609/615 Rev. A Silicon/Data Sheet Errata

The PIC12F609/615/12HV609/615 parts you have received conform functionally to the Device Data Sheet (DS41302A), except for the anomalies described below.

None.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41302A), the following clarifications and corrections should be noted.

1. **Module: 8-Pin Diagram, PIC12F609/HV609 (PDIP, SOIC, TSSOP, DFN)**

Diagram title – replace TSSOP package with **MSOP** package as shown.

(PDIP, SOIC, **MSOP**, DFN)

2. **Module: Table 2: PIC12F615/HV615 Pin Summary (PDIP, SOIC, TSSOP, DFN)**

Table title – replace TSSOP package with **MSOP** package as shown.

(PDIP, SOIC, **MSOP**, DFN)

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3. Module: REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER

Bit 1 should read as shown in bold.

bit 1 **TMR1CS**: Timer1 Clock Source Select bit
1 = External clock from T1CKI pin (on the rising edge)
0 = If **T1ACS** = 1 **system clock (Fosc)**
 = 0 **internal clock (Fosc/4)**

4. Module: REGISTER 8-1: CMCON0: COMPARATOR CONTROL REGISTER 0

Bit 0 should read as shown in bold.

bit 0 **CMCH**: Comparator C1 Channel Select bit
0 = CMV_{IN}- pin of the Comparator connects to CIN0-
1 = CMV_{IN}- pin of the Comparator connects to CIN1-

5. Module: Comparator Voltage Reference

Under "Section 8.10.3 Output Clamped to V_{ss}":

Change from:

- VREN = 0
- VRR = 1
- VR<3:0> = 0000

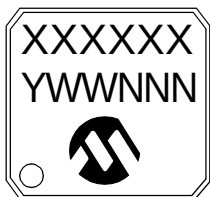
To:

- FVREN = 0

6. Module: 17.0 PACKAGING INFORMATION

Replace TSSOP package with **MSOP** package as shown.

8-Lead MSOP



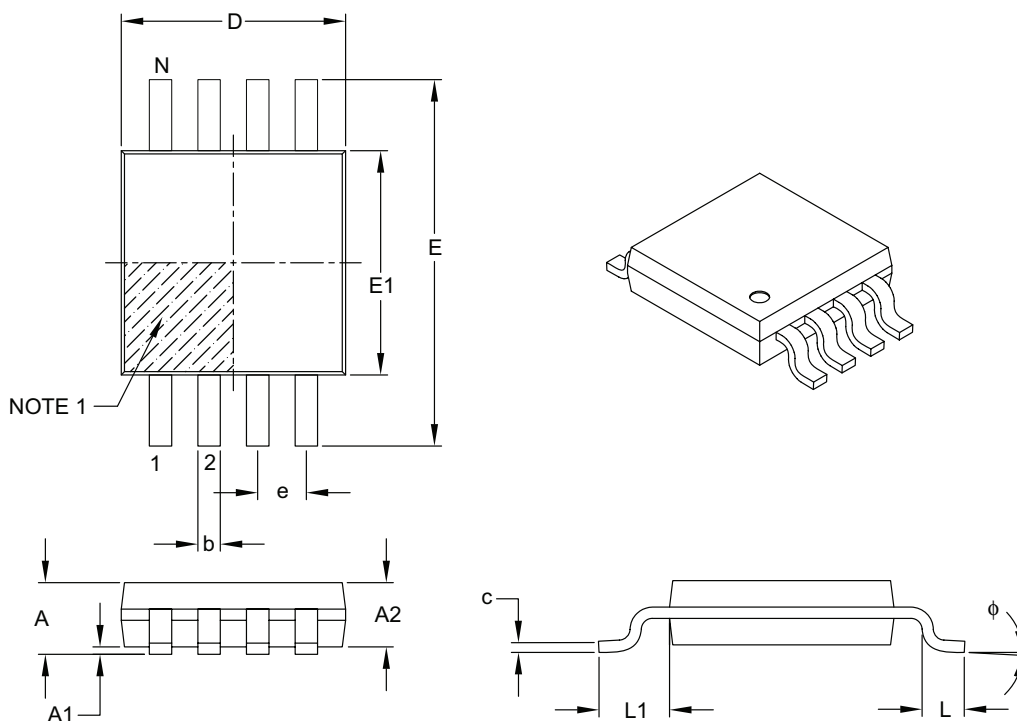
Example



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8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

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7. Module: 8-Pin Diagram, PIC12F615/HV615 (PDIP, SOIC, TSSOP, DFN)

Diagram title – replace TSSOP package with
MSOP package as shown.

(PDIP, SOIC, **MSOP**, DFN)

8. Module: Table 1: PIC12F609/HV609 Pin Summary (PDIP, SOIC, TSSOP, DFN)

Table title – replace TSSOP package with **MSOP**
package as shown.

(PDIP, SOIC, **MSOP**, DFN)

9. Module: Figure 2-1: Program Memory Map and Stack for the PIC12F609/615/12HV609/615

Wraps to 0000h-07FFh should be:

Wraps to 0000h-03FFh

10. Module: Section 10.4.3 Enhanced PWM Auto-Shutdown Mode

Last paragraph before Figure 10-10, the part has
no P1C or P1D. The paragraph should read:

The enabled PWM pins are asynchronously
placed in their shutdown states. The state of each
PWM output pin is determined by the PSSAC and
PSSBD bits of the ECCPAS register. Each pin may
be placed into one of three states:

11. Module: Register 10-2: ECCPAS: Enhanced Capture/Compare/PWM Auto-Shutdown Control Register

Unimplemented bits are Readable/Writable bits.

U-0 should be R/W-0 for bits 6 and 7.

REGISTER 10-2: ECCPAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0
bit 7							bit 0

REVISION HISTORY

Rev A Document (10/2006)

First revision of this document.

Clarifications/Corrections to the Data Sheet:

Added Modules 1 through 6.

Rev B Document (03/2007)

Clarifications/Corrections to the Data Sheet:

Added Modules 7 through 11; Module 6: Replaced

MSOP Package Drawing.

PIC12F609/615/12HV609/615

NOTES:

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